Qualification of the Front End Cards for the CMS ECAL

Project Team:

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Introduction

CMS ECAL trigger and data acquisition system changed in 2002
⇒ Same functionality
⇒ Readout and trigger primitives generation

CCS: Clock and Control System
TCC: Trigger Concentrator Card
DCC: Data Concentrator Card

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New electronics modules
⇒ VFE, FE, LVR…
⇒ Focus on FE card
Introduction

2 models of FE Cards
⇒ Fe card for barrel
⇒ Fe card for End Cap
Introduction

Focus: FE Cards
⇒ 4,000 cards to be produced
⇒ Need for a qualification system

Front end Automatic Tester

Beyond a test system, a valuable simulation tool…
Outline

General Description

• Hardware
• System Control
• On-board ICs

Data Flow

• Standard Operations

Design Details

• Digital Design
• Typical Test
• Simulation Tool
Hardware

New cards:

⇒ FAT card: 300mm × 550mm 12 Layers → 4 units
⇒ FATI card: 300mm × 250mm 6 Layers → 15 units

Why FATI?
• Boundary scan implemented
• Limit aging of FAT
System Control

VME vs. TINI

For debugging purposes:
+ Rack and rack controller available
+ Widely used environment
  - Handling difficult
  - Space consuming

For production tests:
+ Ethernet controlled
+ Easier handling
+ Compact set-up
  - Limited memory resources
Dual Port Random Access Memories

33 16-bit\(\times\)64k DPRAMs on board:

- **25 Data DPRAMs** ⇒
  To simulate 5 VFE cards of 5 16-bit channels each

- **7 REC DPRAMs** ⇒
  Record FE card response
  From 6 17-bit optical links (end cap version)
  16-bit data + 1 bit handshake

- **1 RT DPRAM** ⇒
  Generate a trigger
Programmable Logic

3 Xilinx xc2s200-6fg456 FPGAs on board:

• FPGA1 ⇒
  - Local Bus
  - VME/TINI

• FPGA2 ⇒
  - Local Bus
  - FPGA1
  - Address Port DPRAMs

• FPGA3 ⇒
  - Local Bus
  - Slow Ctrl FE
  - Data from RT DPRAM
Data Flow (1)

Writing to, Reading from DPRAMs

Software request
VME command
Decoding → FPGA1
Data broadcasting on local bus
Data Flow (2)

Configuration of the FE card

Software request
VME command
Decoding → FPGA1
Data broadcasting on local bus
Decoding → FPGA3
Token Ring Communication
Stimulus sending

- Software request
- VME command
- Decoding → FPGA1
- Data broadcasting on local bus
- Decoding → FPGA2
- Data sending to FE
- Data recording from FE
- When trigger from RT DPRAM
  - L1 Missing pulse to FE
- Read back response from FE
- Comparison with model
Digital design

FPGA1: Board management

- VME & TINI interface
  - R/W operations
- FPGAs communication interface
  - Use of Local Bus + handshake signals
- Local bus management
  - Buffers management to avoid collision

FPGA2: Pattern Generation

- Load start address of stimulus
- Set length of broadcasting sequence
- Start broadcasting sequence
Digital design

FPGA3: FE Configuration
Re-use of block from CCS system

Additional edge removal functionality
FE Cards Tests

Production test:

Goals: Checking crucial connections
       Operate board at 40 MHz

Time Budget: ~2 minutes

Typical test cycle:

(-1 boundary scan check) Option
-1 I²C test (check presence of FENIX)
-1 set of data loading in the DATA DPRAMs and 100 triggers in the RT DPRAM.
-1 set-up of the FE card using the slow control
-1 stimulus sending and data recording
Suitable test patterns:
  – Re-use of the FENIX simulation test vectors
  – Appropriate replica of a VFE data flow

FAT: A simulation tool
  – Copy of the real life environment of the FE card
  – Any VFE data flow can be reproduced
  – Slow Control logic identical to real life system

⇒ Useful to understand potential unexpected behaviour
⇒ Can be used to investigate problems during runs
Conclusion

• **FAT:** Flexible system reproducing real life environment of FE cards

• **Multiple applications:**
  - Production tests
  - Simulations
  - Radiation tests (backup)

• **Status:**
  - First system debugging run
  - First production run to start in November
Thank You For Your Attention

Questions?