Irradiation tests of ROHM 0.35µm ASIC and Actel Anti-fuse FPGA for the ATLAS Muon Endcap Level-1 Trigger System

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Abstract

In order to implement a level-1 trigger logic in an efficient manner from timing and space consumption point of view, application specific IC chips (ASIC) as well as FPGA ones are vitally used in the ATLAS muon end-cap level-1 trigger system. Various subsidiary logics are implemented in FPGAs while the core trigger logic is implemented in ASICs. These components will suffer for ten years the radiation of approximately 100Gy of total ionizing dose (TID) and a hadron fluence of $2x10^{10}$hadrons/cm^2, which will cause single event upset (SEU) or single event latch up (SEL). We intend to use Rohm 0.35µm gate width CMOS technology for ASIC and Actel anti-fuse based FPGA. In this presentation we report the result of irradiation test of devices made with these technologies and discuss validity of them to use in the system.

I. Introduction

Three types of ASIC chips are extensively used in the ATLAS end-cap muon level-1 system [1]. In these chips we implement a bunch crossing identification, low- and hi- pT coincidence matrices, readout pipe-line buffer and derandomizer, which are all important ingredients for the level-1 trigger system and for the data acquisition system. The on-detector electronics system also needs two ancillary logics, which will be realized ideally if these are configured in FPGA chips. The ASIC and FPGA chips are mounted in boards, which are just behind an end-cap muon chamber disc (Thin Gap Chamber; TGC) or the outer rim of the disc.

The region where these electronics are mounted will be exposed to the radiation of 100Gy (including a safety factor) and a hadron integrated intensity of $2.1x10^{10}$ hadrons/cm^2 for ten year in the normal operation [2]. We must clarify all the devices (of ASIC and FPGA) to survive in this radiation environment with no degradation in performance in terms of total ionizing dose (TID) and single event effects (SEE). We must also devise the design of the circuits to overcome the SEU (single event upset) even if the device is tolerant of the hadron fluence.

We intend to use four technologies for the chip production, 0.35µm standard full custom CMOS of Rohm, 0.35µm Gate Array CMOS of Hitachi for ASIC production and Actel anti-fuse based FPGA. In order to validate the devices made with these technologies are applicable in our system, we have made the irradiation measurements of them using γ-ray from Cobalt 60 for TID and 70MeV proton beam for SEE.

In this paper we report the results of the radiation tests for chips fabricated with technologies listed above. In section II we briefly outline the on-detector system of the ATLAS endcap muon level-1 trigger system with focusing the functionality of various ASICs and FPGAs. The results for TID and SEE tests for various chips are listed in section III and IV respectively. Finally in the section V we summarize the results and discuss the validity to mount them in vicinity of the ATLAS endcap muon detector.

II. Overview of the On-Detector System

Overall functionality including the off-detector part of the ATLAS level-1 muon endcap trigger system will be found in [3]. In this section we briefly summarize functionality of the on-detector part. Figure 1 shows a schematic diagram of the on-detector part. The on-detector part is physically divided into two parts; PS board (part1) and a VME crate (part2) that mounts High (Hi)-pT boards, Star Switches (SSW) and an HSC (remote crate controller)[4]. A PS board will be mounted just behind the TGC while the VME will be mounted at the outer edge of the TGC discal structure in the ATLAS endcap.

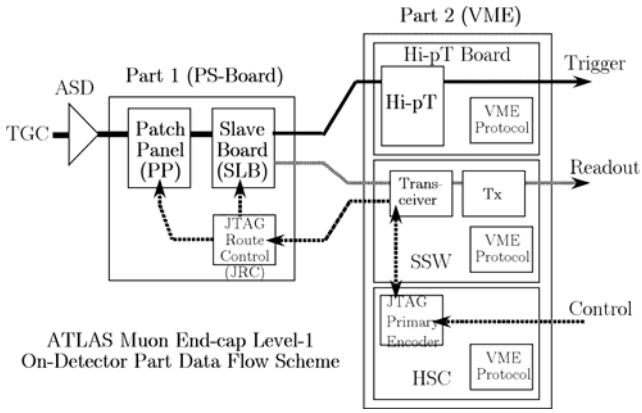

Figure 1: Figure 1: On-detector part of the ATLAS Muon Endcap Level-1 System

We have three data streams. While the trigger and readout data stream go down from the on-detector part to off-detector one, the control data stream comes from the off-detector part towards each IC mounted in the on-detector part to access various registers embedded in the chips with JTAG protocol.

Two kinds of the ASIC chips (Patch Panel; PP, Slave Board; SLB) and an Actel FPGA chip are mounted on a PS board. On a Hi-pT board in the VME crate, the third ASIC of so-called Hi-pT ASIC and an Actel FPGA are mounted. In these boards most of their functionalities are built into the chips in order to reduce the number of COTS (commercial-off-the-shelf) components. PP and SLB ASICs are fabricated with Rohm 0.35μm CMOS full-custom technology, and Hi-pT ASIC is fabricated with Hitachi 0.35μm CMOS gate array.

The PP ASIC has 32 identical channels. Each channel receives a binary data (hit on/off) with LVDS level from a front-end TGC channel (wire group or strip) through an ASD (Amplifier-, Shaper and Discriminator) [5]. Each channel has a variable delay circuit to adjust the delay of input data with 25ns/32 steps (32 delay cells) after conversion of the LVDS signal to a single ended TTL. In order to keep 25ns delay after 32 delay cells, a PLL circuit (phase detector, charge pump and another 32 delay cells with a loop back) is used commonly for all the 32 channels to adjust the delay. The SLB ASIC is a digital CMOS circuit, which contains Low-pT coincidence matrices for the TGC Level-1 trigger and read-out function (a level-1 buffer, a de-randomizer buffer and parallel to serial converter for data output) with JTAG control. The Hi-pT ASIC is a digital CMOS circuit, which receives track/hit information from SLB ASICs and reconstructs tracks using High-pT coincidence matrix logic for the TGC Level-1 trigger (no read-out function).

Beside these three kind of ASIC chips, two different series of Actel anti-fuse FPGA (A54SX-A and Axcelerator) [6] are used to implement various ancillary logic circuits for each board. Medium scale FPGA A54SX-A is used for a JTAG routing controller on the PS-board and a VME driver, which is commonly used for modules mounted in the part2 VME crate. The chip is also used for a JTAG encoder in an HSC module. The Axcelerator chip is a large scale FPGA with embedded memory. This chip is used for both transceiver and transmitter in an SSW module.

All in all, eight different kinds of ASIC and FPGA chips fabricated with four different technologies are used in the ATLAS muon endcap level-1 trigger system. We have followed the ATLAS standard radiation test [2] for these chips. For the fabrication of the chips, we have done no special process to deal with the radiation tolerance. Beside we have done the tests to check their radiation tolerance, however, the registers to keep parameters necessary to drive chips are all constructed with majority logic in order to reduce degradation due to SEE. This logic keeps a bit value with three flip-flops, and keeps checking consistency of data stored in all the flip-flops. The schematic of this logic circuit is shown in Fig. 2.

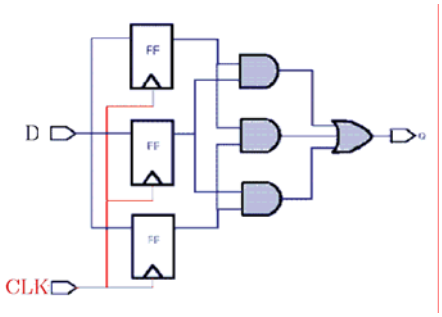

Figure 2: Voting logic to keep one bit data with three FFs

III. TEST FOR TOTAL IONIZATION DOSE (TID)

A. TID Test Procedure

The γ-ray irradiation facility is two-story structure; an irradiation room on the downstairs and a store with a lead container for the irradiation sources on the upstairs. 48 pencil type rods as radiation sources are filled in a cylindrical vessel, which moves between the upstairs and the downstairs via remote control system. The maximum strength of the sources and the maximum dose rate are 22 TBq and 1000Gy/hr in H_2O. The irradiation rate can be controlled by changing the radiation source and the location of the DUT (we call hereafter a target chip as DUT; Device Under Test). We used ^{60}Co as the source and the irradiation rate was set at 500Gy/hr. The irradiation facility of RCNST is widely being utilized in University of Tokyo; the dose rate is periodically calibrated using a Fricke Radiation Meter. The irradiation and the annealing were done at room temperature, around $25^{O}C$. During the irradiation and the annealing, DUTs were biased without clock and the current were monitored. The functionality was checked before and after the irradiation and the annealing.

B. Results of TID test

1) CMOS ASIC

We have tested four PP ASIC chips. Three chips were irradiated up to 300Gy, and the other one was irradiated to 850Gy. Until 300Gy, we have observed no increase of the static current for all the chips while the current of the fourth one was increased from 49nA to 81nA monotonically as the irradiation level increased from 500Gy to 850Gy.

The PLL in a PP ASIC adjusts a voltage (vcon) to hold 25nsec delay for the variable delay circuit of 32 delay cells. The PLL tried to increase vcon if the response of the delay circuit becomes slower. Otherwise it tried to decrease vcon to keep delay value constant as 25nsec. In Fig. 3(a), we plot this vcon as the irradiation level. The vcon was decreased once and it turned up at around 600Gy.

In the mean time in order to observe any characteristic change of a circuit in a Rohm 0.35μm chip caused by the

irradiation, we have processed a ring-oscillator circuit in an independent chip with the same technology. The circuit is connected with 501 NAND logics to form a ring to observe the oscillation frequency. We have also irradiated this chip as the same condition as the one for PP ASIC. Fig. 3(b) shows the frequency change with the irradiation. We can find the frequency was increased till 600Gy, then it was decreased, namely the circuit response became once faster owing to the irradiation, and then it became slower. Comparing with this figure with Fig. 3(a), we found correlation. This means that the PLL worked correctly to adjust vcon in order to compensate the variation of the circuit response time due to the irradiation up to 850 Gy where we quitted the test.

The functions of the ICs were measured before, after the irradiation, after the annealing and at the breaks during the irradiations. We could not find any failure in the tests.

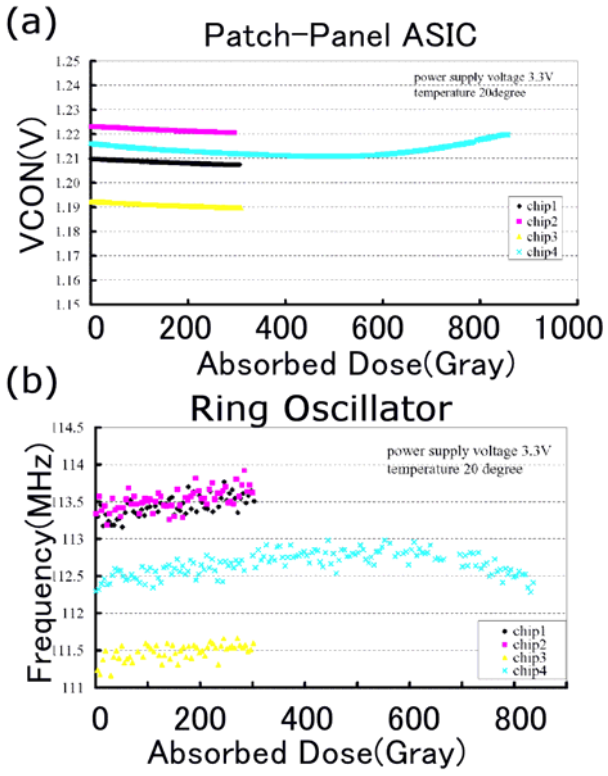

Figure 3: PP ASIC TID test results

Three SLB ASIC chips (0.35µm Rohm full custom) were sampled in the TID test. Static currents were measured during irradiation.

In the SLB ASIC, the current increased from 2.1mA to 14.5mA at the start of the irradiation. The increase of the current due to the integrated dose can be observed at around 150Gy. At the integrated dose of 200Gy, we interrupted the irradiation for the function measurement. After the inspection of the chip, the irradiation was resumed up to 430Gy, where the current monotonously increased to 44mA. The current went down to 33 mA at the termination of the irradiation. In the annealing of three days, the current gradually decreased to 2mA. Other two chips were irradiated up to 200Gy. Behaviours of the current increase were exactly same as the chip mentioned above.

For two Hi-pT ASIC chips, one was irradiated up to 750Gy. During the irradiation we took two breaks at 200Gy and 400Gy for the function inspection of the chip. The increase of the current gradually starts at around 200Gy and is rapid beyond 300Gy. Another chip was irradiated up to 200Gy and showed similar behaviour.

The functions of the ICs of SLB and Hi-pT were measured before, after the irradiation, after the annealing and at the breaks during the irradiations. The functions of the Low-pT trigger logic in the SLB ASIC and the Hi-pT trigger logic in the H-pT ASIC were tested. Five test input patterns were fed to the ICs at 40 MHz and the outputs were compared with the simulation. We could not find any failure in the tests.

2) Actel Anti-fuse FPGA

In on-detector part of the system, two series A54SX-A and Axcelerator of Actel anti-fuse FPGA chips are used. A54SX-A will be used in PS-board and also in the boards installed in the part2 VME crate while the Axcelerator chips will be used only in SSW board mounted in the part2 VME crate. Axcelerator chip is a large scale FPGA and has an embedded memory.

In a chip of A54SX-A series, we have built in a ring-oscillator circuit and measured its characteristic behavior in the radiation environment while a four-bit shift register circuit in R-cell and a ring oscillator circuit in C-cell have been built in a chip of Axecelerator chip.

Fig. 4(a) shows static currents versus absorbed dose (irradiation) level for four A54SX-A series FPGA chips. The full (dotted) curves indicate the current with (without) the operation of the ring oscillator circuit. Fig. 4(b) indicates frequency dependence on the absorbed dose. From both figures, we found that no significant degradation due to the irradiation was observed up to 600Gy in A54SX-A chips. Note that we will use them in at most 100Gy radiation environment.

The static current for four Axcelerator series FPGA chips versus the absorbed dose is shown in Fig. 5(a). In the measurement, the operation of the built-in circuit (a ring oscillator) has been paused for 10 seconds in every one minute regularly. This makes saw-toothed structure in the graph. The frequency of the ring oscillator versus the dose is shown in Fig. 5(b). In the current measurement, we observed two different currents per chip, one is one observed in the I/O cell which needs 3.3V power, and the other one is for the core logic part which is operated with 1.5V. From both figures, we found that neither significant current increase nor frequency change has been observed for all the four chips tested. Dynamic range of the change for both the leak current and the frequency in the Axcelerator series chips were smaller than one in the SX-A series ones. This may be due to that the Axcelerator chips were processed with more advanced technology of 0.15µm CMOS anti-fuse than SX-A ones.

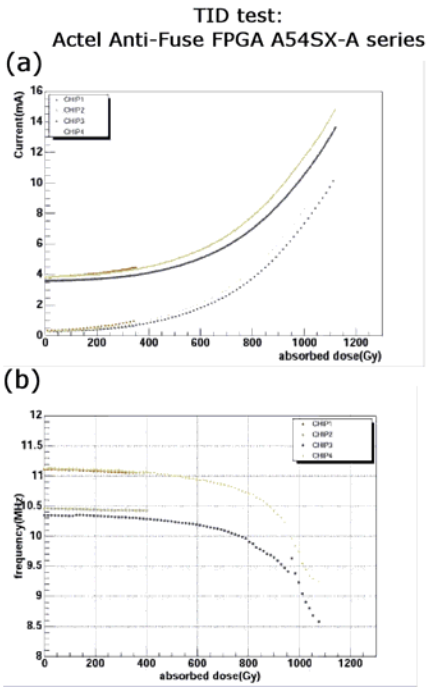

Figure 4: Results of TID test for Actel Anti-Fuse FPGA A45SX-A series

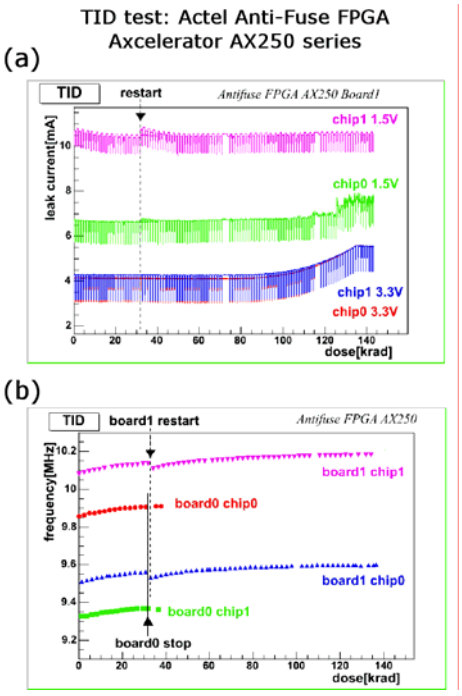

Figure 5: Results of TID test for Actel Anti-fuse FPGA Axcelerator series

IV. TEST FOR SINGLE EVENT EFFECT

A Soft SEE (Single Event Effect) is phenomenon of radiation induced bit flip (non-permanent). A Hard SEE is also the same as the soft SEE but a destructive SEE produces permanent short circuits in a chip, like a latch-up. Whatever effect is concerned, any SEE rate for a chip can be determined from the SEE test as follows;

$$SEE\ rate = (\sigma_{SEE}) \times Nbits \times SRLsee \times SFsim$$

where σ_{SEE} is the cross section of either soft or hard SEE for a chip in the location it will be installed (cm^2/bit), *Nbits* is the number of bits affected by SEE, *SRLsee* is the simulated Radiation Level at the location in a second (hadrons/cm^2/s), and *SFsim* is the safety factor of the simulation, and is set as '5'.

The maximum value of the *SRLsee* of the PP ASIC or SLB ASIC is seen on the electronics module at the most inner part of the ATLAS endcap (r=775mm, and z= 1250mm) and is estimated as 2.11×10^2 hadrons/cm^2/s (for hadrons energy > 20MeV). The *SRLsee* for the position where Hi-pT ASICs are placed is estimated to be 1.42×10^2 h/cm^2/s. These values are taken from a simulation done by the ATLAS radiation hardness assurance group [2].

To estimate the SEE rate for any particular chip in a test, we must count occurrence of soft (hard = latch up) SEEs for certain amount of time, estimate integrated proton intensity into the chip, and derive soft (hard) σ_{SEE} from them.

For the estimation of the proton intensity for a chip in a test, we made dosimetry measurement for a cu foil. Thickness of the Cu foil is 0.1 mm and its purity is 99.99+%.

The size of the Cu foil is 25 mm by 25 mm and attached on top of the chip just being tested. After one hour of a run of the SEE test, g-ray spectrum from activated radioisotopes was measured for 1,000 sec with a Ge detector.

We can estimate the number of nucleus generated (N) in the irradiation for period Tr seconds from the number of γs observed (C_γ) in the dosimetry measurement. Then if we know the effective cross section of proton and cu and number of cu atoms in the target, we can deduce the proton intensity (number of protons/cm^2/s). Then we calculated the integrated proton intensity (F) actually injected in the die of a chip in the irradiation period taking into account the beam profile information. For the beam profile measurement, we exposed the γ-rays emitted from a cu foil on an imaging plate, and scan the intensity of the exposed imaging plate with a commercial imaging plate reader. The unit of F is given as protons/cm^2. Then σ_{SEE} is given with a following relation,

$$\sigma_{SEE} = (\text{number of SEE counted}) / F / Nbits.$$

A. Test Procedure

For the SEE test, we have used an experimental facility of Tohoku University Proton cyclotron (CYRIC). 70MeV Proton beam was extracted through a Ti foil of 20mmϕ and 100μm thickness into air and was impinged to a DUT. The block diagram of a measurement setup is shown in Fig. 6. A target board and a ZnS fluorescence screen were mounted on an X-Y stage. The beam position was first monitored by the fluorescence screen and then the target board was moved to the beam position (The beam was stopped with a beam stopper during the X-Y stage was moving.). Actual beam

profile and beam intensity were measured, individually for each chip with dosimetry of a 100μm thick Cu foil placed in front of the DUT. The beam intensity at the final beam stopper was around 2 - 4nA. The beam was intentionally broadened up to the size of around 20mmϕ.

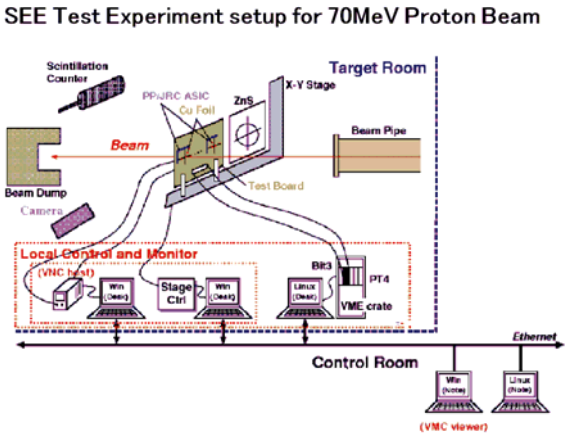

Figure 6: SEE test experiment setup for 70MeV proton beam of Tohoku University Cyclotron

B. SEE cross sections for individual chips

1) CMOS ASIC

We have processed a 4 bit 256 stage shift register into an independent ASIC chip in order to evaluate σ_{SEE} for Rohm 0.35μm CMOS chips. We have produced four chips of this shift register ASIC for σ_{SEE} estimation. We then took the value as σ_{SEE} for PP and SLB ASIC chips commonly. In the SEE test of this special ASIC, we have observed total 185 times of soft SEE for four chips with $6.3x10^{12}$ protons/cm^2 of the total integrated proton intensity injected (fluence). Thus the σ_{SEE} is estimated as $2.8x10^{-14}$ cm^2/bit.

In the Hi-pT ASIC, because all the registers are implemented by the voting logic circuit, only Boundary-Scan Registers (BSR) were examined by writing arbitrary data and reading/verifying via the JTAG protocol. The number of bits in the BSR observed was 92. The speed of the JTAG clock (TCK) was around 100 kHz. No SEE has been observed with the fluence of $5.6x10^{12}$protons/cm^2. Then σ_{SEE} is estimated for Hi-pT ASIC as $< 4.7x10^{-15}$cm^2/bit with 90% confidence level. Even one single event latch-up has been observed neither in Rohm CMOS devices nor Hitachi gate array devices.

2) Actel Anti-fuse FPGA

SX-A Series

We have installed a four bit shift register of 256 stages (1024 bit), and read and verified the data outputted. No SEE has been observed with the fluence of $2.6x10^{12}$ protons/cm^2. σ_{SEE} is estimated, therefore, as $< 1.5x10^{15}$cm^2/bit with 90% confidence level.

Axcelerator Series

We have installed a four bit shift register of 345 stages (total 1380 bit). We have applied the SEE test also to the embedded memory whose size is 54Kbit. Since the memory is configured as dual port memory, regularly we inputted a bit pattern to the memory, and compared it with the output bit pattern from the memory for verification. We have observed 32 SEE in the R-cell FF and 3869 in the embedded memory with $1.4x10^{12}$ protons/cm^2 of the proton fluence. σ_{SEE} for R-cell (Flip flop cells in FPGA) is estimated as $1.6x10^{-14}$cm^2/bit, and σ_{SEE} for Memory is $4.9x10^{-14}$cm^2/bit.

No single event latch-up has been observed in Actel anti-fuse FPGA chips.

V. CONCLUSIONS

From the TID tests, we could conclude that Rohm CMOS 0.35μm ASIC chips will work fine for Total absorbed dose of 800Gy, and Hitachi Gate Array will be fine till 300Gy where we stopped the irradiation. The series SX-A chips (Axcelerator) of Actel Anti-fuse FPGA will work fine till 600 (1000)Gy.

The SEE test results can be summarized in Table 1.

Table 1: Compilation of the SEE test results

Technology	Proton fluence (protons/cm^2)	σ_{SEE} (1/cm^2/bit)
Rohm CMOS 0.35μm	$6.3x10^{12}$	$2.8x10^{-14}$
Hitachi CMOS 0.35μm Gate Array	$5.6x10^{12}$	$<4.7x10^{-15}$
Actel FPGA SX-A	$2.6x10^{12}$	$<1.5x10^{-15}$
Actel FPGA Axcelerator (R-cell)	$1.4x10^{12}$	$1.6x10^{-14}$
Actel FPGA Axcelerator (Memory)	$1.4x10^{12}$	$4.9x10^{-14}$

VI. REFERENCES

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