Irradiation Tests of ROHM 0.35μm ASIC and Actel Anti-fuse FPGA for the ATLAS Muon Endcap Level-1 Trigger System

Chikara Fukunaga *(Tokyo Metropolitan University)*
and ATLAS muon-endcap level-1 trigger group

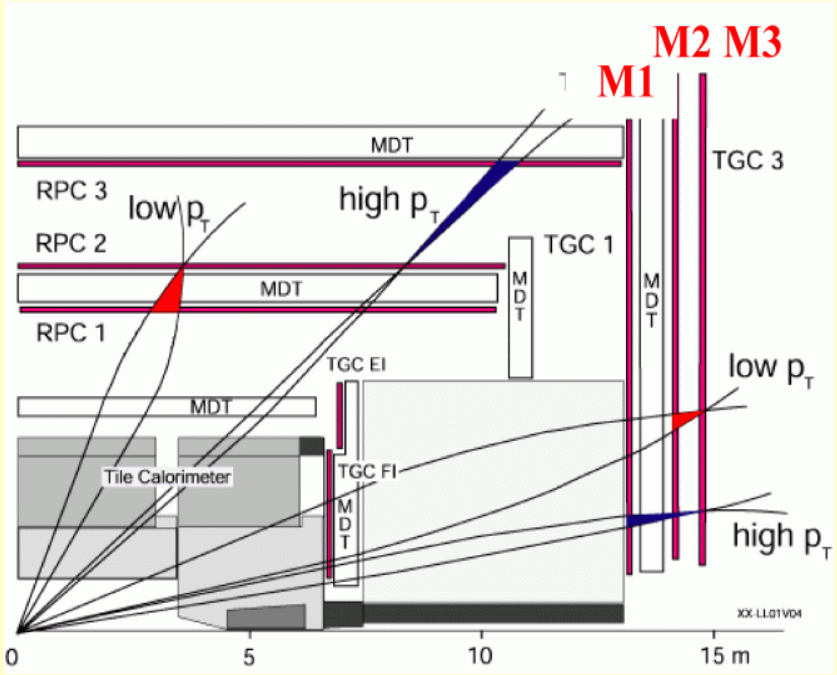
- TID (γ-ray) and SEE (proton) tests and results for
  - ROHM and HITACHI 0.35um CMOS
  - Actel Anti-fuse FPGA series (SX-A, Axcelerator)
  - LVDS and G-link ser./deser. (Poster)

Introduction

- Most of the ATLAS Endcap Muon Level-1 system will be installed in the detector (On-detector part).
- **Various trigger and readout circuits have been realized with (Three) ASIC chips.**
- **Subsidiary circuits are implemented in FPGA chips.**
- The devices must be hard or tolerant for irradiation of 10 years. This must be confirmed with tests of
  - the ionizing damage (Total Ionizing Dose; TID) with γ-ray
  - the Single Event Effects (SEE) with proton beam (> 60MeV)

ATLAS Muon Endcap Level-1 System

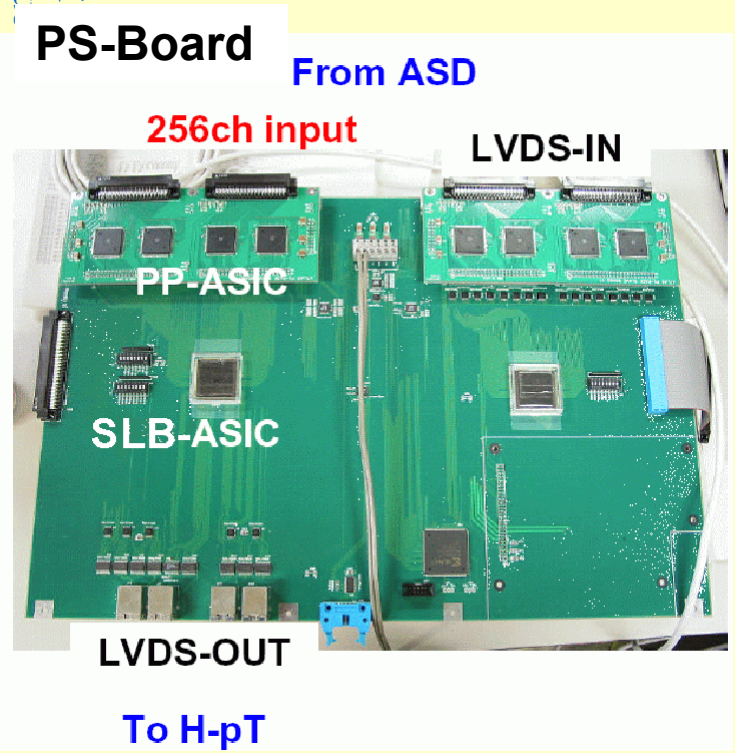
- Thin Gap chambers (TGC) are used to detect muons in the endcap regions (1.05 ≤η≤ 2.70)
- Hit (on/off) signals of Total 300k channels are processed in the vicinity of the chambers

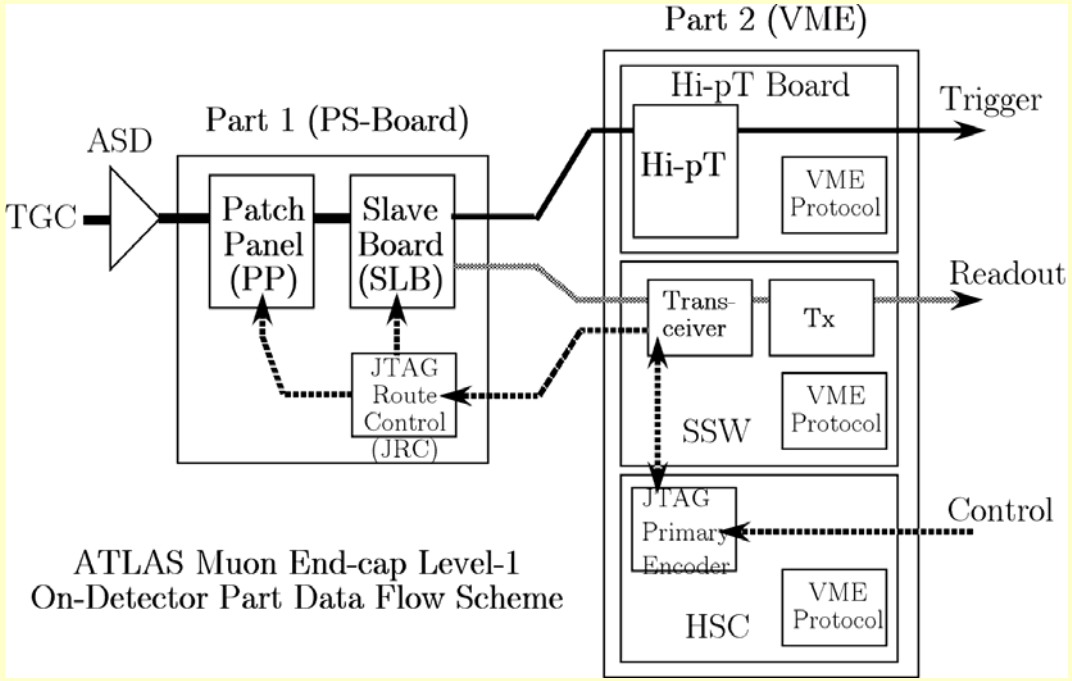


Level-1 Trigger/Readout System

- Two on-detector parts and off-detector part
- On-detector parts
  - PS-board
  - Hi-pt and Star Switch (SSW) (VME) Crate

nd FPGA for
ystem





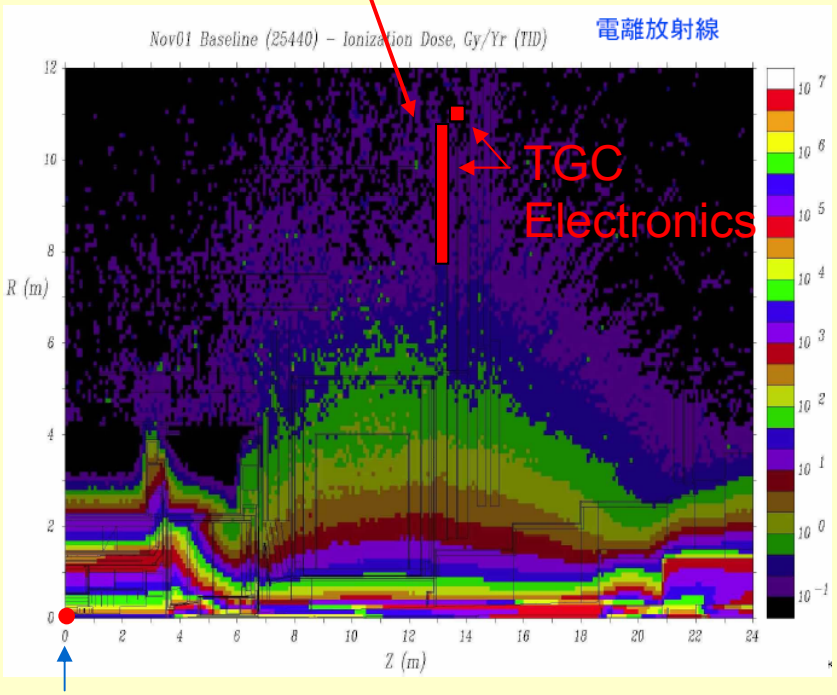
Devices under Test

- Custom ICs (8 types with 4 technologies)
  - **PP (Patch Panel) ASIC** 0.35um CMOS ROHM
    - Variable Delay with PLL, LVDS to CMOS, BCID, Test pulse Gen.
  - **SLB (SLave Board) ASIC** 0.35um CMOS ROHM
    - Low-pT coincidence matrices, Level-1 buffer+ Derandomizer
  - **High-pT (Hi-pT) ASIC** 0.35um HITACHI GA
    - Hi-pT coincidence matrices
  - **Simple FPGA** Actel Anti-fuse SX-A
    - JRC (PS board), HSC, VME protocol
  - **FPGA with embeddded memory** Actel Anti-fuse Axcelerator
    - SSW Transmitter/Receiver
  - *Serial Link IC (LVDS and G-link serdeser)*

Radiation Environment

Ionizing Dose: Gy/year

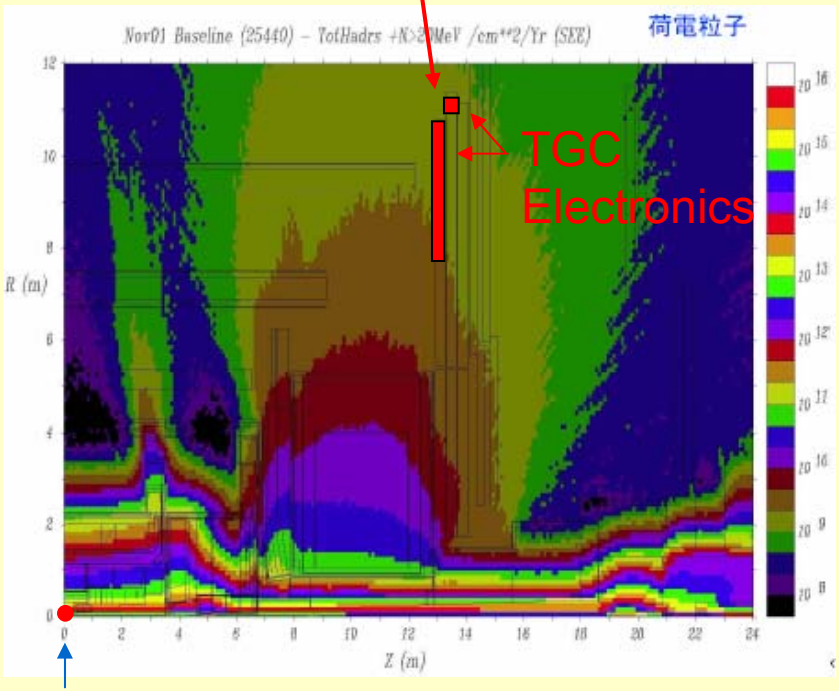
2-3Gy/10year → 140-210Gy/10year
(with Safety Factor:70)



Interaction Point

Total Hadron (>20MeV) :/cm^2/year

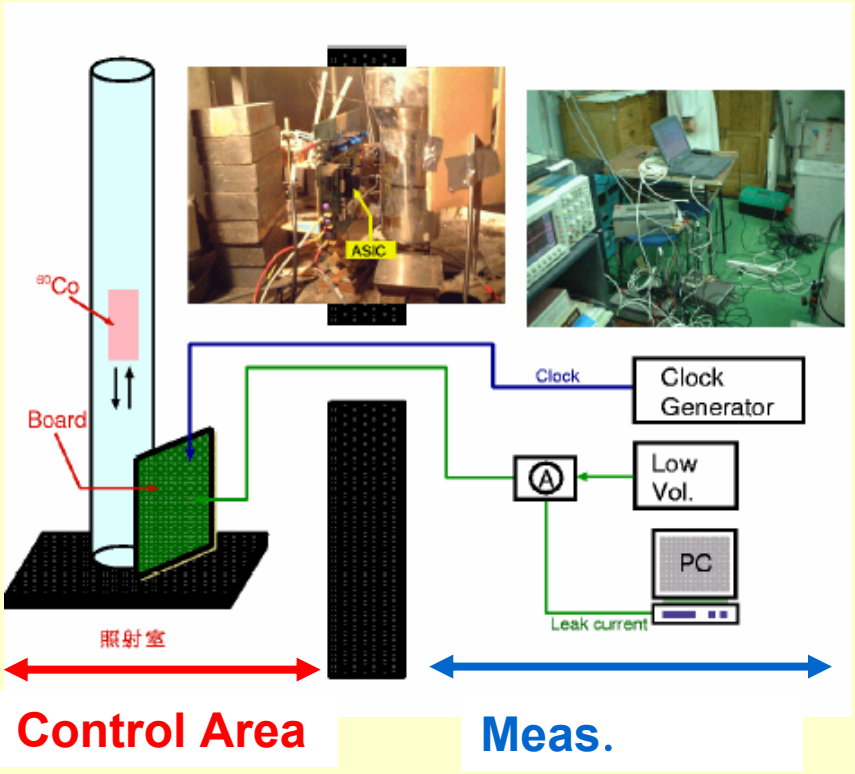
1.4-2.8x10^{10} hadrons/cm^2/10year



Interaction Point

TID test (γ-ray irradiation)

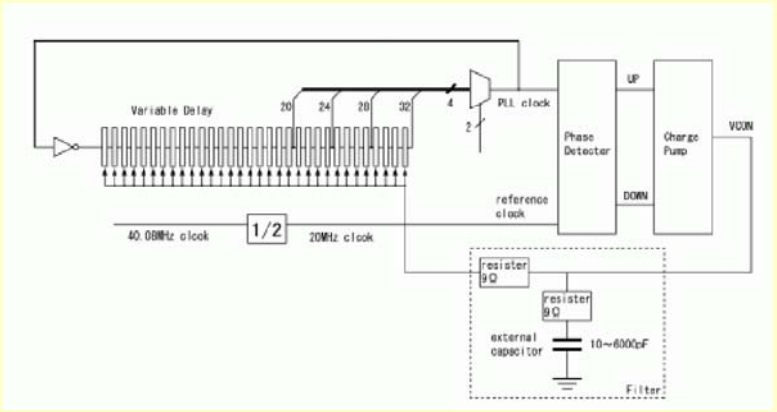
- Evaluation of Total Ionization Dose using γ-ray from ^{60}Co
  - A DUT (chip) is mounted on a PC board.
  - The board is applied with voltage and input signals
  - Irradiated 300Gy and more
  - Typically 4 samples/DUT
  - Icc or Frequency versus Abosrbed dose (time) has been evaluated



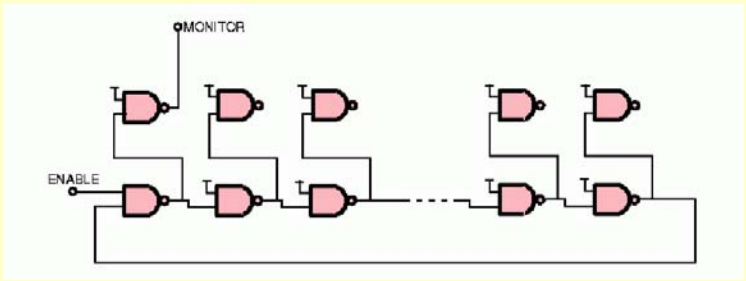
RCNST lab. At Univ. of Tokyo

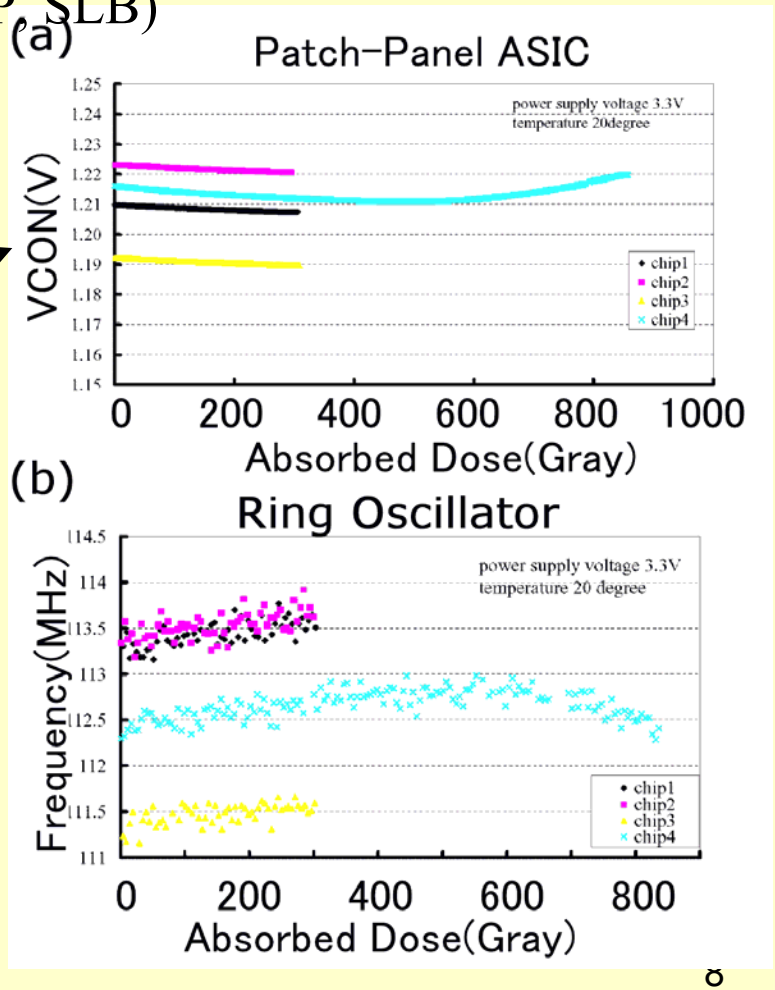
TID test results CMOS ROHM 0.35µm

- 0.35µm ROHM CMOS full custom chip (PP, SLB)
  - PP ASIC VCON(V) of PLL circuit for variable delay



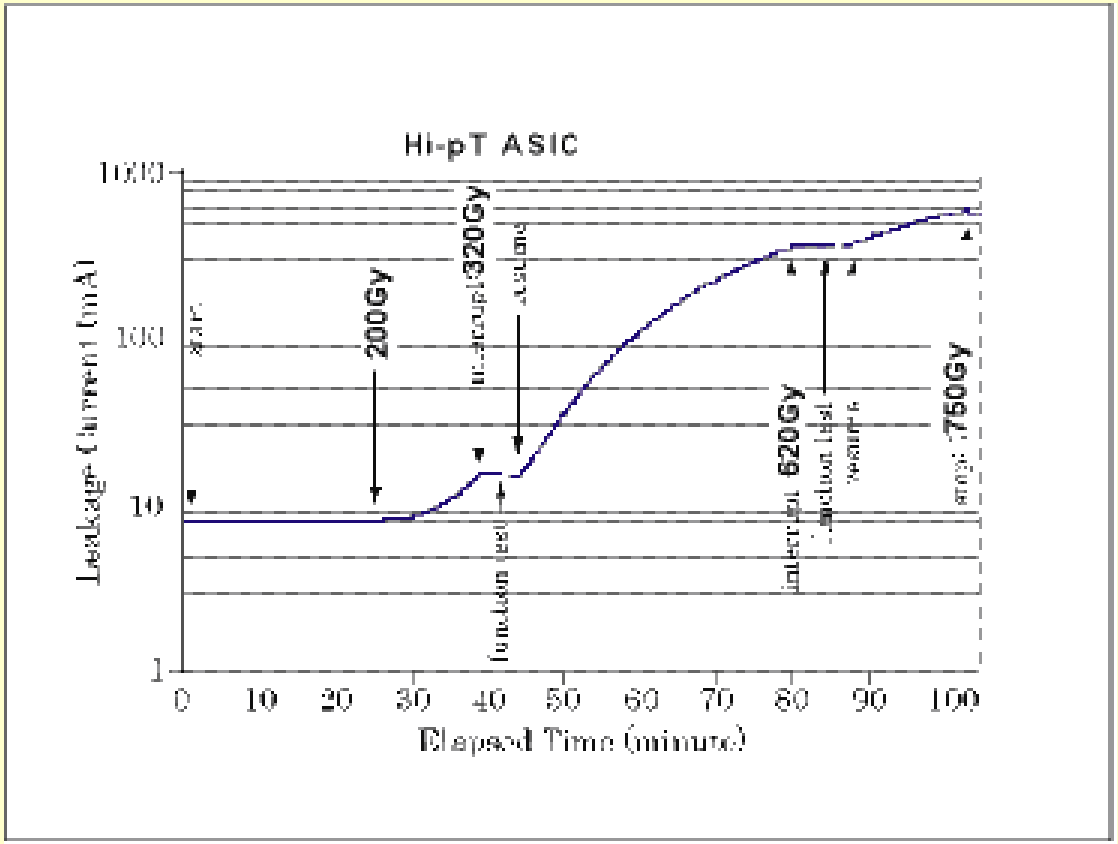
  - Special Made Ring Oscillator





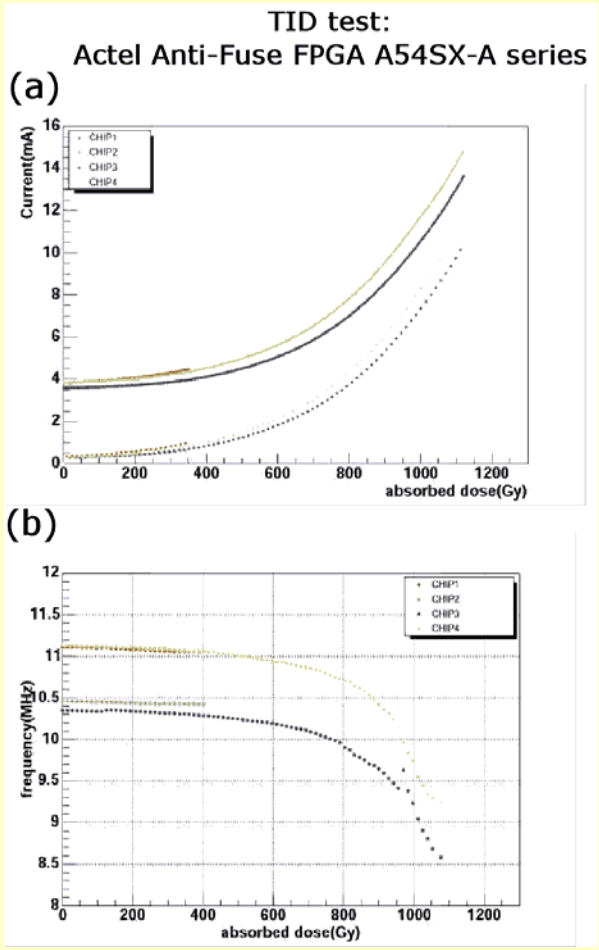
TID test result CMOS Hitachi 0.35μm Gate Array (Hi-pT ASIC)

- Hi-pT ASIC TID test

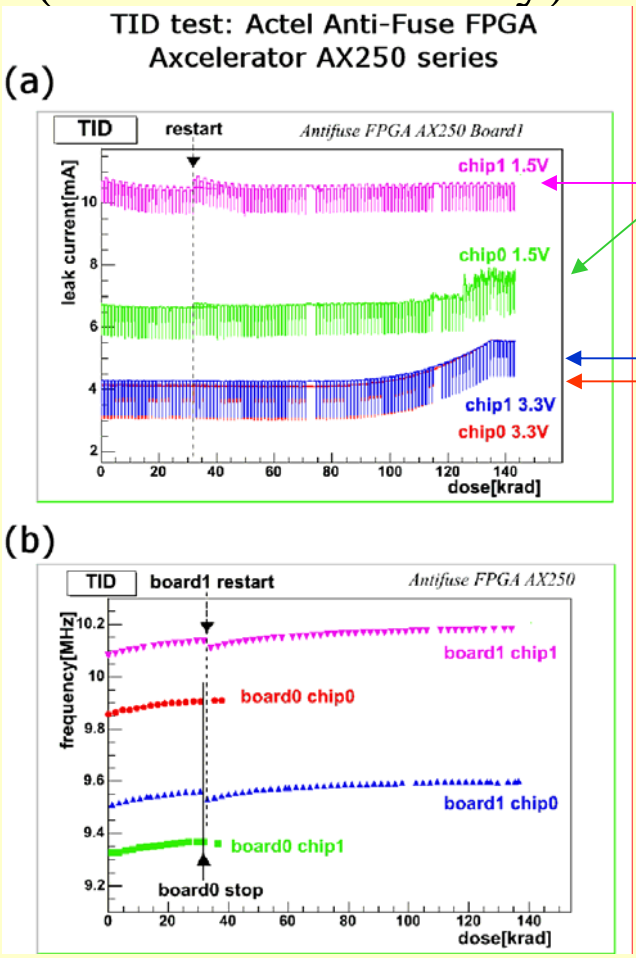


Actel Anti-fuse FPGA series (Ring Oscillator Circuit)

- SX-A series



- Axcelerator series (embedded memory)



Single Event Effect Test: Proton 70MeV

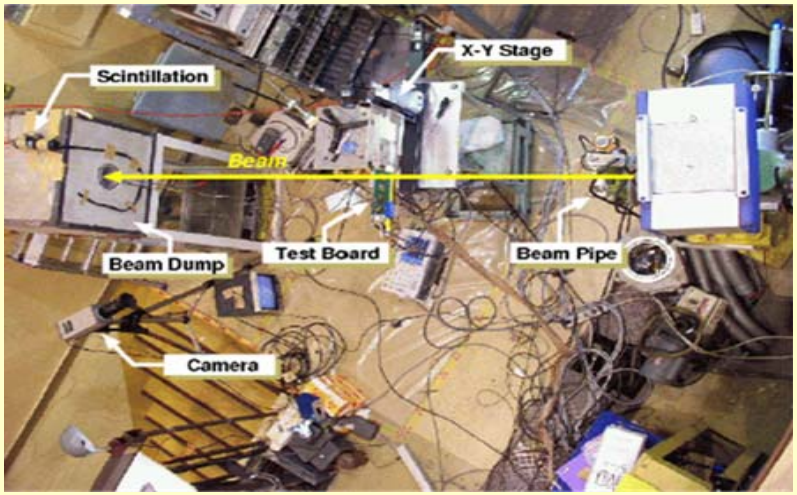
- SEE : Radiation induced bit flip (soft&hard)
- If we know σ_{SEE} for a chip experimentally, we can predict SEE rate with

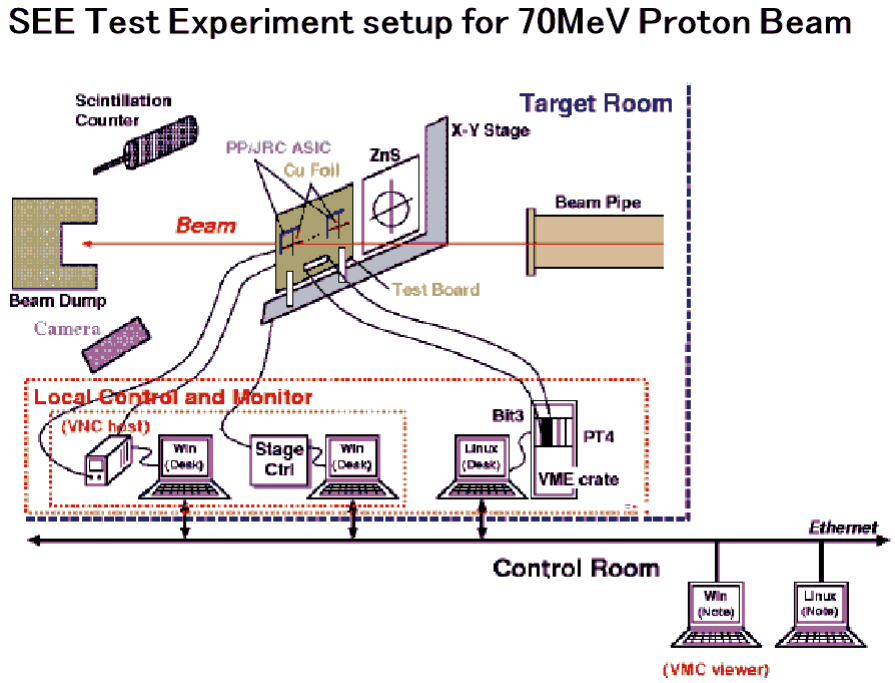
  SEE rate = σ_{SEE} x Nbits x SRLsee x SFsim

Nbits	Number of Bits	100(Hi-pT)~3000(SLB)
SRLsee	SEE radiation level (hadrons/cm^2/s)	PS board: **2.11x10^2** HSC VME crate:**1.42x10^2**
SFsim	Safety Factor	5

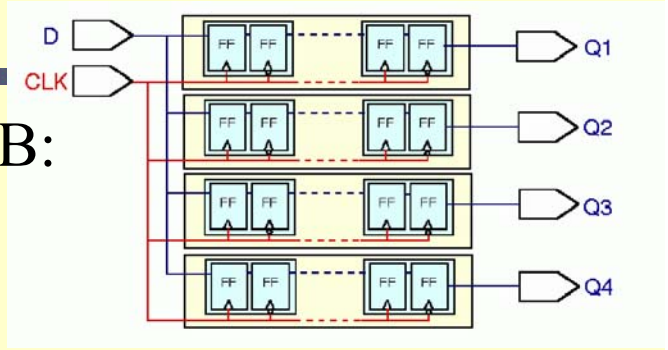
SEE test experiment at Tohoku Univ.

- 70 MeV proton beam at Tohoku University Cyclotron (CYRIC) laboratory
- Proton Intensity & beam profile were determined with dosimetry measurement of Cu foils (0.1mm) attached in front of DUT

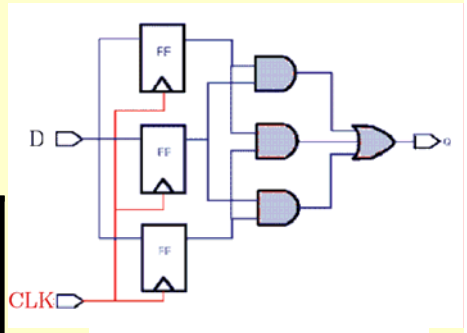




SEE Test results: ASIC



- σ_{SEE} for ROHM 0.35μm chips for PP, SLB:
  - A special IC was made (4bit shift registers)
- σ_{SEE} for HITACHI 0.35μm GA
  - JTAG Boundary Scan reg.
- Results: Soft SEE (No hard SEE observed)



Majority Logic

Technology	Chip	σ_{SEE} cm^{-2}/bit	Nbits/Numb. Of chips	SEU rate/day (system)
ROHM 0.35um	PP	2.8×10^{-14}	95/10000	2
ROHM 0.35um	SLB		3007/3000	23
HITACHI 0.35um	Hi-pT	$<4.7\times10^{-15}$	30/1000	<0.001

w/o majority Logic: It is installed in all the bits in chips

SEE test results: Actel Anti-fuse FPGA

- A54SX-A series: 256 stage 4-bit Shift register
  - No SEE error has been observed with proton fluence of 2.6×10^{12} proton/cm^2
  - $\sigma_{SEE} < 1.5 \times 10^{-15}$ (1/cm^2/bit)
- Axcelerator AX250 series
  - 345 stage 4-bit Shift registers in R-CELL (FF-cell)
    - 32 SEE with proton fluence of 1.4×10^{12} proton/cm^2
    - $\sigma_{SEE} = 1.6 \times 10^{-14}$ (1/cm^2/bit)
  - 54Kbit embedded memory (dual port type)
    - 3869 SEE
    - $\sigma_{SEE} = 4.9 \times 10^{-14}$ (1/cm^2/bit)

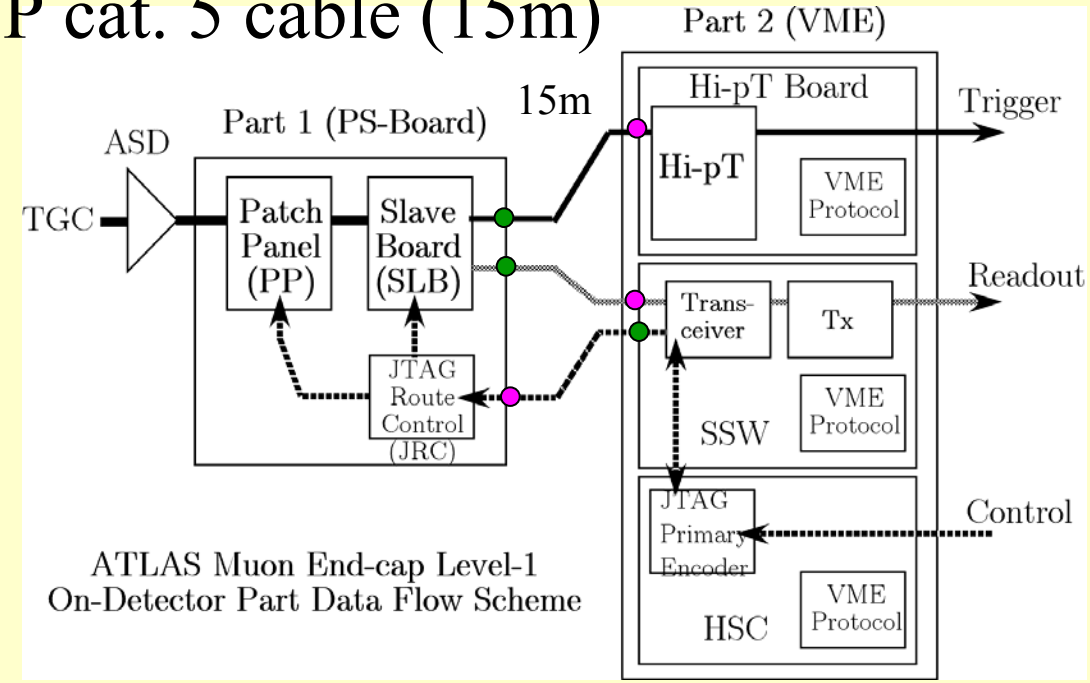
Soft SEE only,
No Hard SEE

SEE rate for Actel FPGAs in whole system/day <2

Majority logic will be installed also

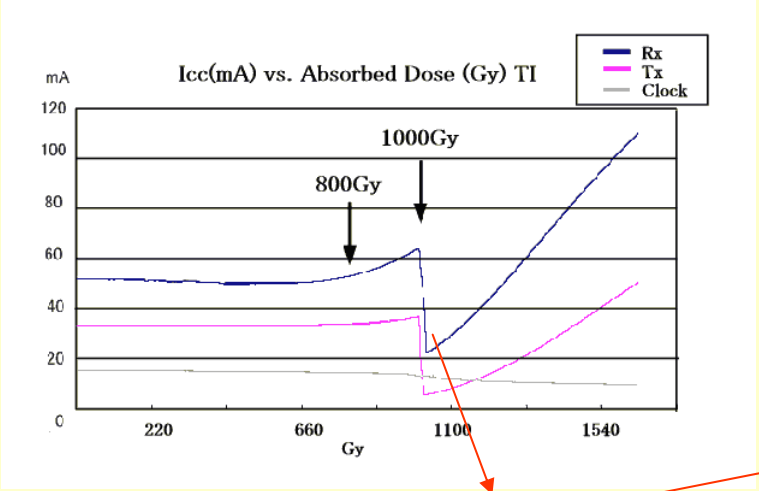
LVDS serializer/deserializer

- LVDS serializer and deserializer candidates
  - NS:DS65LV1023/1024
  - TI:SN65LV1023/1224
- Connected with UTP cat. 5 cable (15m)



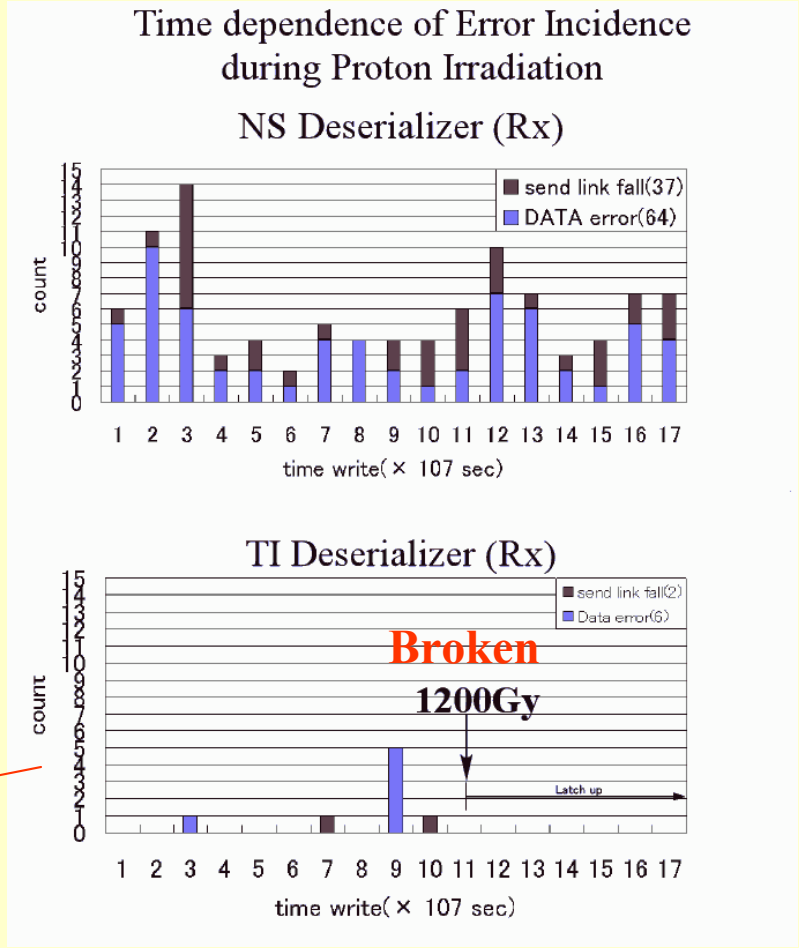
TID and SEE tests of LVDS ser/deser

- TID test up to 1600Gy
  - **NS: Icc vs. Dose:** No significant Icc increase
  - **TI: Icc vs. Dose: ↓**



TI chip will be fine if dose < 1000Gy

- SEE test



LECC2004 Irradiation test of ASIC and FPGA for ATLAS TGC Level-1Trigger System

Summary

- ATLAS TGC electronics
  - TID 140-200Gy/10 years & SEE ~$2x10^{10}cm^2$/10years
- γ-irradiation (TID) Test
  - ASIC/Actel anti-fuse FPGA chips have no problem up to ~1000Gy
- Proton 70MeV irradiation (SEE) Test
  - Measurement of σ_{SEE} for Soft SEE: rate will be expected as very low
  - No destructive (hard) SEE like Latch-up has been observed.
- Link (LVDS, G-link) components
  See in detail our Poster presented in this workshop