GTK chip I/O interconnections

with notes on Logic standards appended

CERN: GTK ASIC design review S. Chiozzi, INFN-FE

GTK chip I/O interconnections

First attempt to find interconnection solutions between GTK demonstrator chips and external Daq/Test logic with different power supply operating conditions.

GTK chip demonstrators power supply requirements:

- GTK-CERN chip

  Vcore = 1.2V

  Vddio = 2.5V

- GTK-TO chip

  Vcore = 1.2V

  Vddio = 1.2V … 2.5V (?)

GTK chip I/O interconnections

GTK chip demonstrators I/O logic:

GTK-CERN chip:

single ended: LVCMOS @ 2.5V (?)

differential: LVDS @ 2.5V

GTK-TO chip:

single ended: LVCMOS @ 1.2V .. 2.5V (?)

differential: LVDS @ 2.5V (?)

HSTL_12 @ 1.2V (?)

GTK chip I/O interconnections

Low voltage High speed differential I/O logic standards:

- LVDS

(Low Voltage Differential Signaling, **ANSI/TIA/EIA-644-A**)

- HSTL_12

(High Speed Transceiver Logic, 1.2V, **JEDEC JESD8-16a**)

- CML

(Current Mode Logic, not explicitly standardized. CML implementation can meet the requirements of Clause 47 of the IEEE 802.3 standard that defines the physical layer of the XAUI interface)

GTK chip I/O interconnections

Low voltage single ended I/O logic standards:

- IC logic (wide range, 1.2V +/- 0.1V)

(JEDEC standard **JESD76-1**)

- LVCMOS (1.2V typ, wide range, 0.8V to 1.3V)

(JEDEC standard **JESD76-1**)

- SSTL_3, SSTL_2, SSTL_18

(Stub series terminated Logic, JEDEC standards **JESD8 - 8 / 9B / 15A**)

GTK chip I/O interconnections

All demonstrator chips will use differential I/O channels for clock, data and control lines (maybe some test/control I/O will be implemented with single ended standard library LVCMOS pads e.g. Artisan library for IBM 0.13u).

• GTK-CERN I/O will use LVDS standard (Vddio = 2.5V, Vref = 1.2V).

• GTK-TO I/O probably will spam between LVDS (Vddio = 2.5V, Vref = 1.2V) and low voltage differential HSTL_12 logic (Vddio = 1.2V, Vref = Vddio / 2 = 0.6 V).

GTK chip I/O interconnections

Main goal:

Try to find commercial logic driver / transceiver that accommodates all supply voltage in 1.2V to 2.5V range and interfaces with common FPGAs I/O LVDS standard.

Current FPGA includes I/O working with power supply as low as 1.2V: these devices can be connected directly to GTK demonstrators working at different power supply (but FPGA tend to shows many restrictions with 1.2V supply voltages).

Using dedicated drivers/adapters for GTK chips gives the possibility to realize control logic with standard FPGA using a well know LVDS interface.

This solution (if exists) moves towards a common GTK demonstrator control board that accepts both chip prototypes and give the possibility of use FPGA with common industry standards I/O.

GTK chip I/O interconnections

Questions about GTK differential I/O:

• GTK LVDS I/O minimum Vddio ? (i.e. what is the minimum power supply requirement for output driver to work properly?)

• GTK LVDS outputs common voltage Vcm = 1.2V (LVDS standard) or simply Vcm = Vddio / 2 ?

• GTK LVDS inputs voltage range rail-to-rail ? (i.e. receiver works properly if Vcm shifts from ideal Vddio/2 level and reach power rails ?)

GTK chip I/O interconnections

GTK LVDS I/O minimum Vddio ? (i.e. what is the minimum power supply requirement for output driver to work properly?)

Normally LVDS outputs drive a 1.2V common mode voltage developed from an internal reference. This voltage reference need a minimum Vddio voltage to work properly: most LVDS drivers are powered with 3.3V or 2.5V.

There is the possibility to develop LVDS drivers with two power supply pins: the main logic works at 2.5V and the output part use a Vccio lower than 2.5V. **In any case standard set the common mode to 1.2V and Vdiff = +/-350mV, so Vccio cannot be below 1.8V**

See “IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 2, FEBRUARY 2005, Low-Voltage Low-Power LVDS Drivers”

GTK chip I/O interconnections

GTK LVDS outputs common voltage Vcm = 1.2V (LVDS standard) or simply Vcm = Vddio / 2 ?

If GTK differential output current is guarantee independent from voltage supply variations and output driver includes some form of programmable common mode voltage (i.e. Vcm defined by external reference voltage or by internal divider network to (Vccio / 2)) then there is the possibility to use only one power supply with wider Vdd range.

If Vddio = 2.5V and Vcm = 1.2 V then GTK driver behaves as standard LVDS output.

If Vddio = 1.2V and Vcm = 0.6V then GTK driver behaves as standard HSTL_12 output.

In both cases GTK differential receiver must works with a minimum +/-200mV input signal amplitude. Common mode voltage range should be rail-to-rail.

GTK chip I/O interconnections

GTK LVDS inputs voltage range rail-to-rail ? (i.e. receiver works properly if Vcm shift from ideal Vddio/2 level and reach power rails ?)

In the attempt to work with only one power supply voltage value for all chip sections, a first market survey has found some new logic components with output levels range 1.2V .. 1.8V.

These translators are differential “ANY-input-to-CML” types: typical CML output has a swing comparable with LVDS standard but different common mode voltage. Note that CML output VOH equals Vddio rail.

If GTK differential inputs are guaranteed to work with CML signal levels, the interfacing problem at 1.2V is quite solved: all GTK chips will be driven by a pool of “Any-to-CML” translators powered at 1.2V. An external LVDS input is compatible with CML output and an external LVDS output is translated to GTK I/O ring voltage levels.

GTK chip I/O interconnections

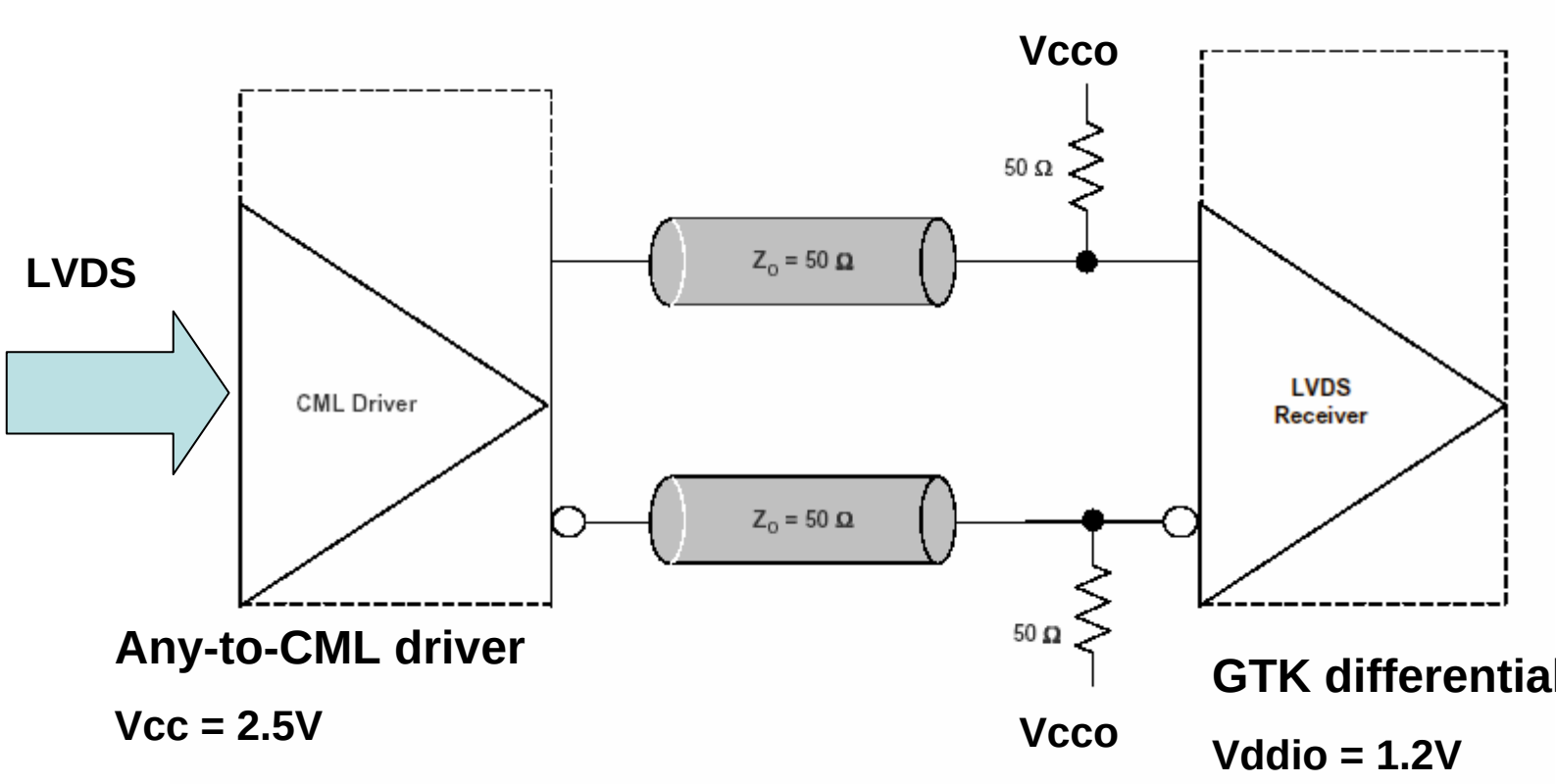
GTK LVDS inputs voltage range rail-to-rail ? (i.e. receiver works properly if Vcm shift from ideal Vddio/2 level and reach power rails ?)

(continued)

If GTK differential inputs have typical receivers optimized for signals with voltage common range Vddio/2 the direct connection with external CML logic is not feasible and requires some adapter network (line termination + common range reduction). In this case there will be a big constellation of resistors (i.e. six resistors for each LVDS link) with unavoidable additional capacitance (RC networks affecting signal edges).

GTK chip I/O interconnections

CML to LVDS connection example: GTK receiver rail-to-rail compliant with Vddio = 1.2V



Any-to-CML driver

Vcc = 2.5V

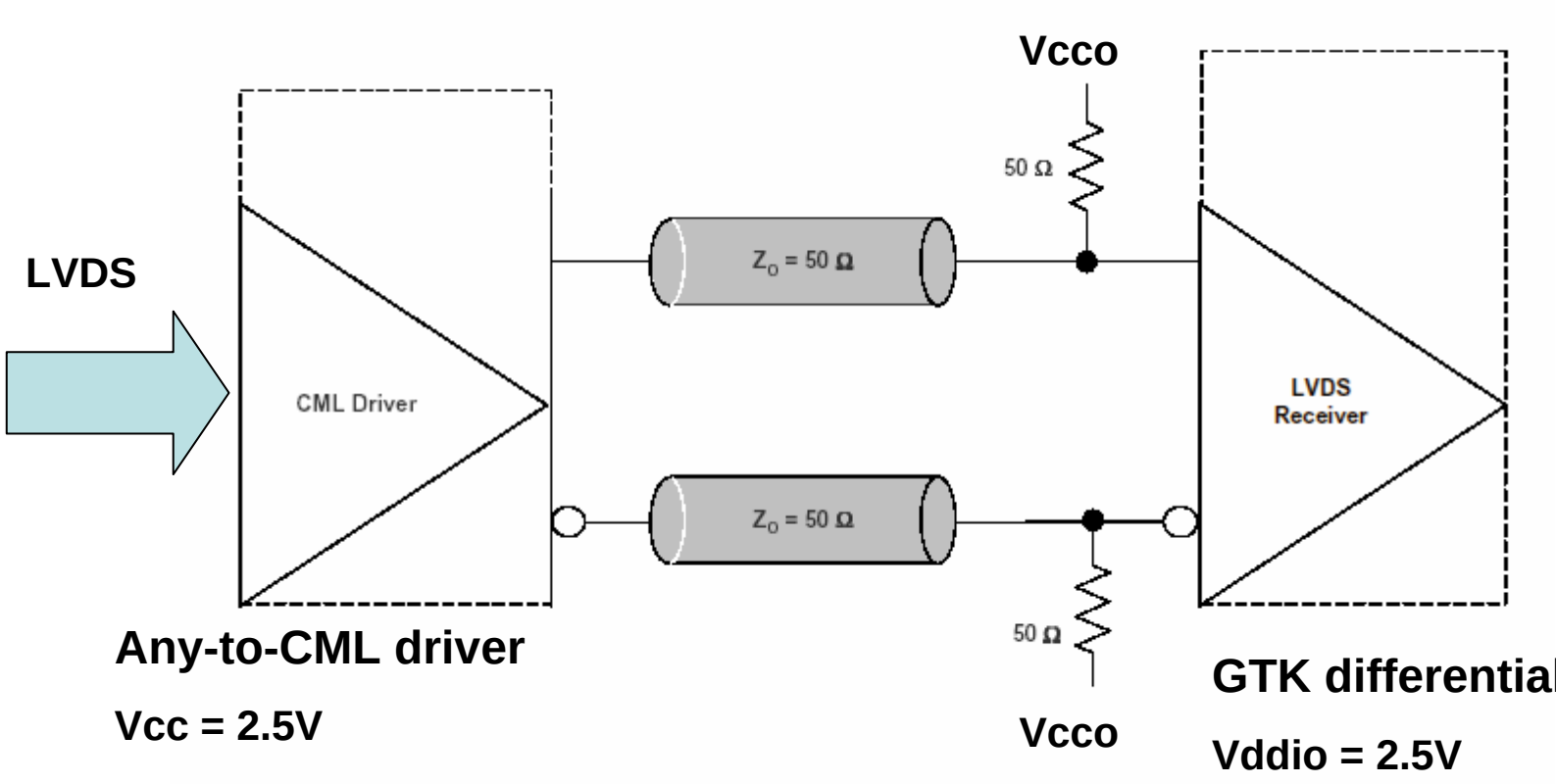
Vcco = 1.2V

GTK differential receiver

Vddio = 1.2V

GTK chip I/O interconnections

CML to LVDS connection example: GTK receiver rail-to-rail compliant with Vddio = 2.5V



Any-to-CML driver

Vcc = 2.5V

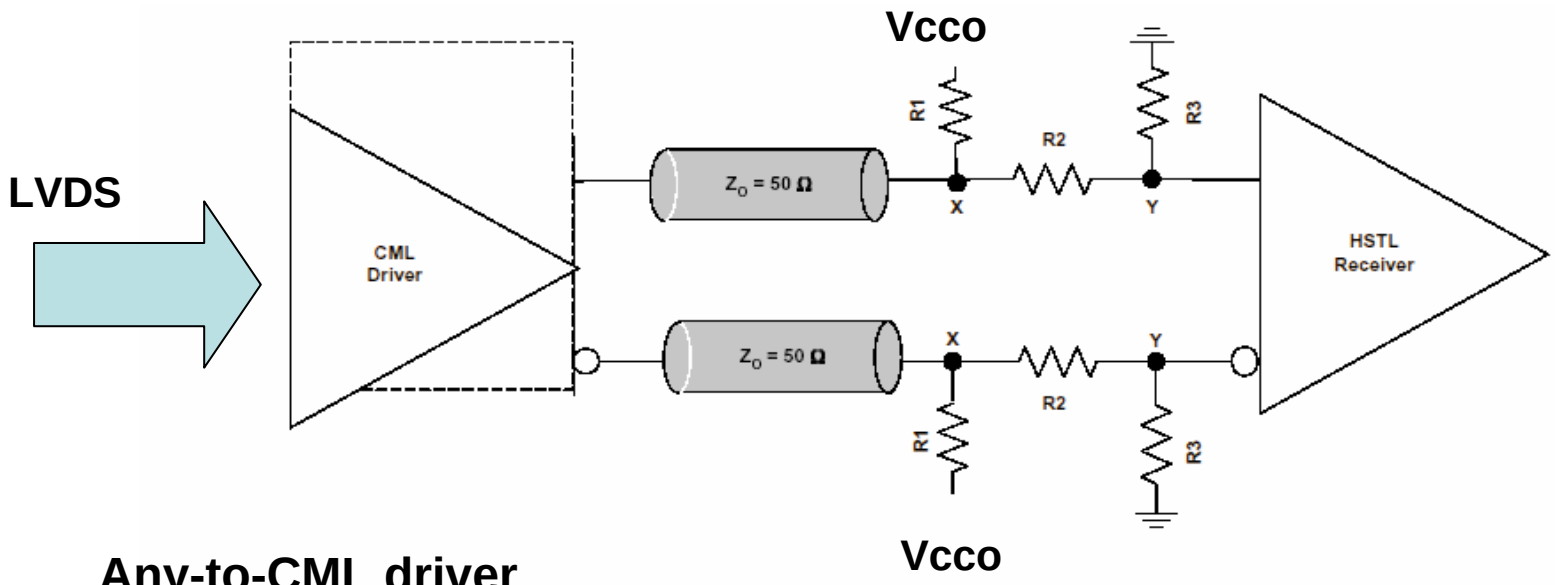
Vcco = 1.8V max

GTK differential receiver

Vddio = 2.5V

GTK chip I/O interconnections

CML to LVDS connection example: GTK receiver NOT rail-to-rail compliant with Vddio = 1.2V



Any-to-CML driver

Vcc = 2.5V

Vcco = 1.2V

GTK differential receiver

Vddio = 1.2V

GTK chip I/O interconnections

“Any-Input-to-CML” differential translators specifications:

- **Micrel new 1.2/1.8 Ultra-Low Voltage CML product family**
- **Core power supply of 2.5V with output drivers powered by 1.2/1.8V supply.**
- **Operate up to 3.2GHz with jitter performance to be less than 10ps p-p over industrial temperature range (-40-degC to +85-degC)**
- **Products include a 1:2 Fanout Buffer, Differential Line Driver/Receiver, 2:1 Multiplexer, and a 2 x 2 Crosspoint Switch**
- **All devices are declared in volume production with pricing for 1K quantities starting at $1.54.**

GTK chip I/O interconnections

Notes:

• Using "Any-to-CML" translators requires a minimum of two resistors (termination) per link, LVDS standard employs only one.

• If GTK differential receivers are rail-to-rail compliant, "Any-to-CML" translators can be powered at Vcco = 1.2V and this supply should works for both GTK Vddio = (1.2V, 2.5V).

• If GTK differential receivers are NOT rail-to-rail compliant, to avoid additional resistor networks other interconnect solutions include standard LVDS drivers/repeaters with asymmetrical power supply (i.e. 3.3V LVDS powered with Vdd=+2.5V, Vss=-0.8V) → output common mode voltage will be shifted and centered with GTK I/O rails.

• <u>If both demonstrators chips will use fixed Vddio = 2.5V, there are NO external interconnection problems and many LVDS drivers / repeaters exists (also Rad-Tol tested from LHC data base).</u>

Appendix: notes on Logic standards

- SSTL
- HSTL
- BIC
- CML
- LVDS
- LVPECL

Notes on Logic standards

- **SSTL Description**

SSTL [Stub Series Terminated Logic] is an electrical interface commonly used with DDR [Double Data Rate] DRAM memory IC and memory modules.
There are currently three main types of SSTL signally standards (JEDEC/EIA):

SSTL_3	**JESD8-8**	Stub Series Terminated Logic for 3.3 Volts
SSTL_2	**JESD8-9B**	Stub Series Terminated Logic for 2.5 Volts
SSTL_18	**JESD8-15A**	Stub Series Terminated Logic for 1.8 Volts
		(SSTL_18 used in DDR2 SDRAM specification **JESD79-2E**)

Notes on Logic standards

- **SSTL Electrical Levels**

Parameters:
Vddq: Output driver power supply
Vt: Line termination power supply
Vref: Reference Voltage for receivers
NOTE: standard do not specify IC power supply, only output driver powers are defined

SSTL_3 requires Vddq = 3.3V, Vt = Vref = 0.5 x Vddq
(used with **DDR** memory)

SSTL_2 requires Vddq = 2.5V, Vt = Vref = 0.5 x Vddq
(used with **DDR I** memory)

SSTL_18 requires Vddq = 1.8V, Vt = Vref = 0.5 x Vddq
(used with **DDR II** memory)

Notes on Logic standards

- **Example: SSTL_2 driver/receiver**

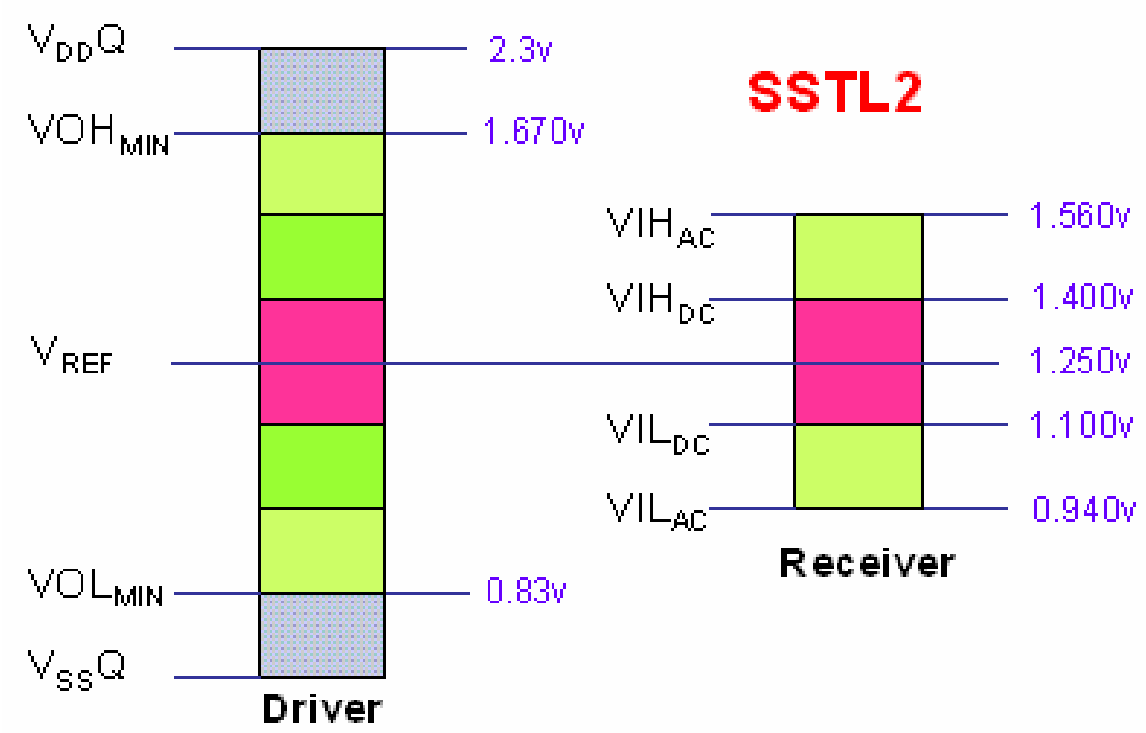
SSTL_2 interconnects require a 25 ohm series resistor at the source and a 50 ohm termination resistor at the destination pulled to Vtt [assuming a 50 ohm class I system].

Set the termination resistor to 25 ohms in a class II system [class II uses 16.2mA, class I use 8.1mA].

Bi-Directional signals require the 50 termination resistor at the source in additional to the series termination resistor.

Notes on Logic standards

- **Example: SSTL_2 driver/receiver voltage levels:**



Note: voltage levels taken from base version JESD8-9. For updated voltage levels see tables in last JEDEC revision JESD8-9B.

Notes on Logic standards

- **Example: SSTL_2 output driver termination (class I)**

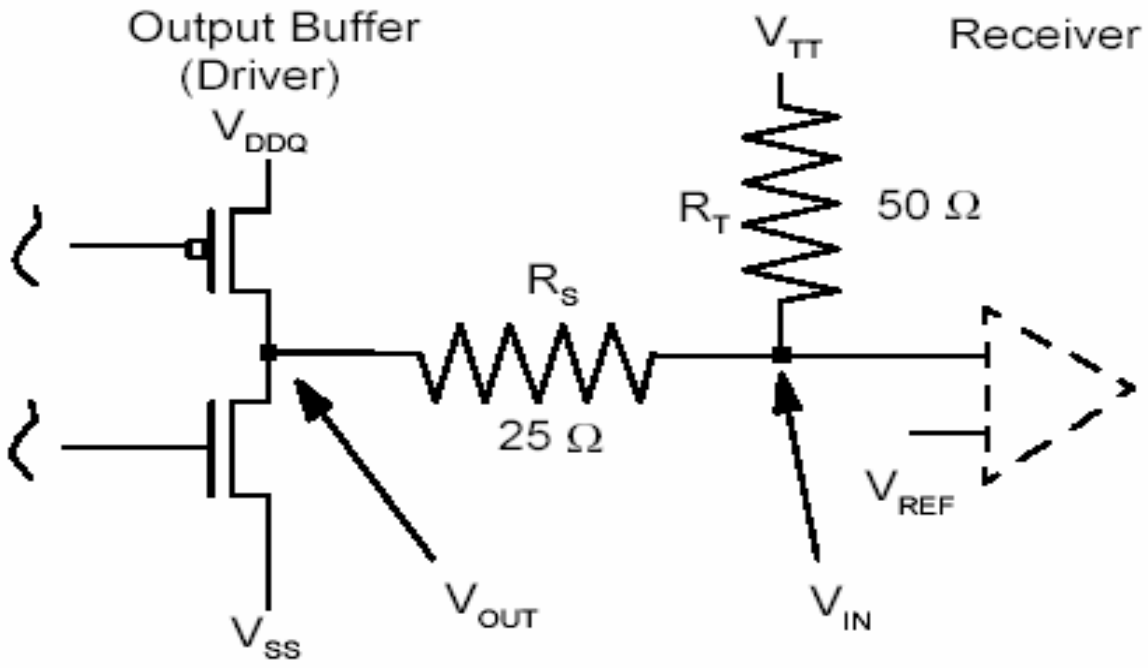


Figure 3 — Typical output buffer (driver) environment

Notes on Logic standards

- **Example: SSTL_2 output driver termination (class I)**

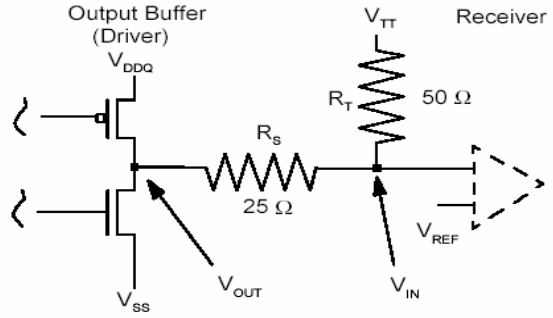


Figure 3 — Typical output buffer (driver) environment

The important condition is that **VIN be at least 405 mV above or below VTT** as a result of VOUT attaining its maximum low or it's minimum high value (standard JESD 8-9B).
The two cases of interest for SSTL_2 are where the series resistor RS equals 25 ohm and the termination resistor RT equals 50 ohm (for Class I) or 25 ohm (for Class II). VTT is specified as being equal to 0.5 x VDDQ.

In order to meet the 405 mV minimum requirement for VIN, a minimum of **8.1 mA (Class I, RT = 50ohm)** or **16.2 mA (Class II, RT equals 25)** must be developed across RT.

Notes on Logic standards

- **Example: SSTL_2 output driver termination (class I)**

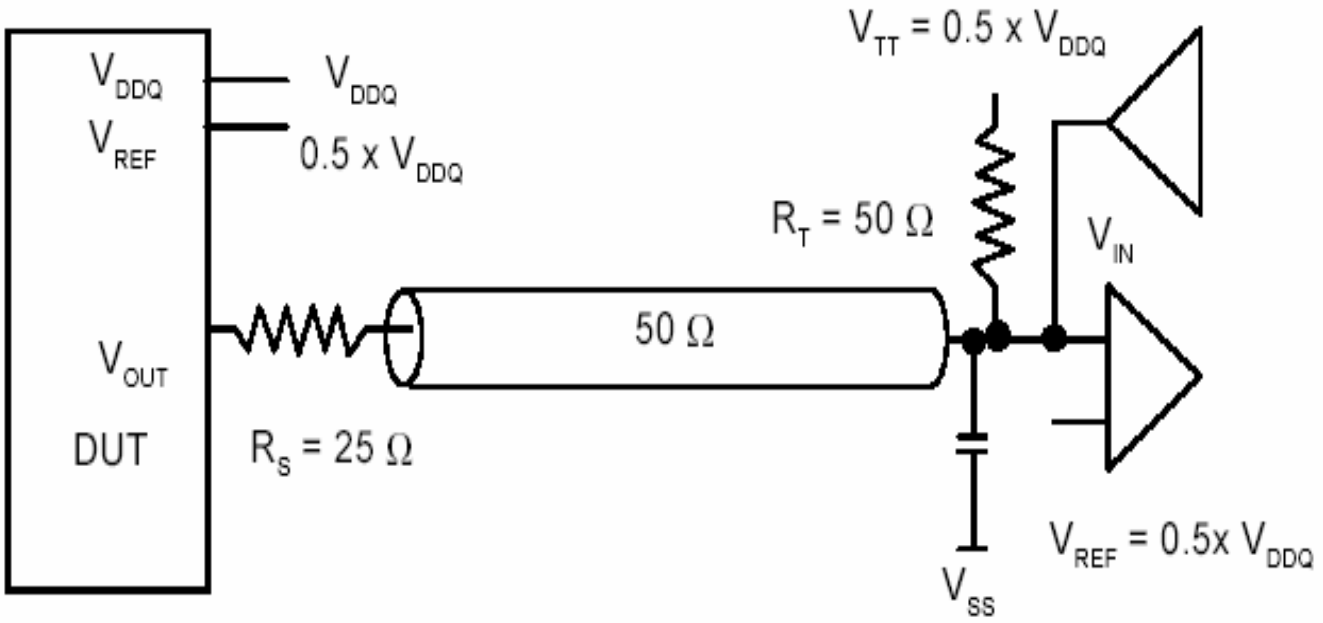


Figure 4 — Example of SSTL_2, Class I, symmetrically single parallel terminated output load, and series resistor

Notes on Logic standards

- **Example: SSTL_2 output driver termination (class II)**

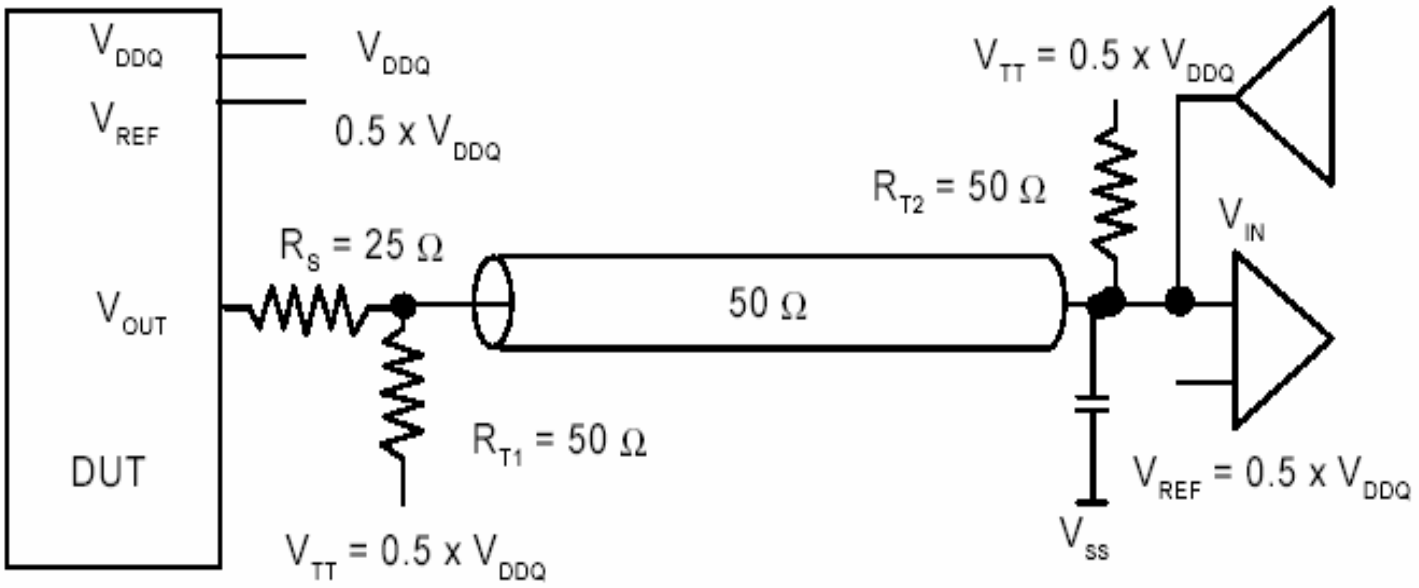


Figure 5 — Example of SSTL_2, Class II, symmetrically double parallel terminated output load with series resistor

Notes on Logic standards

- **Example: SSTL_2 output driver termination (class II)**

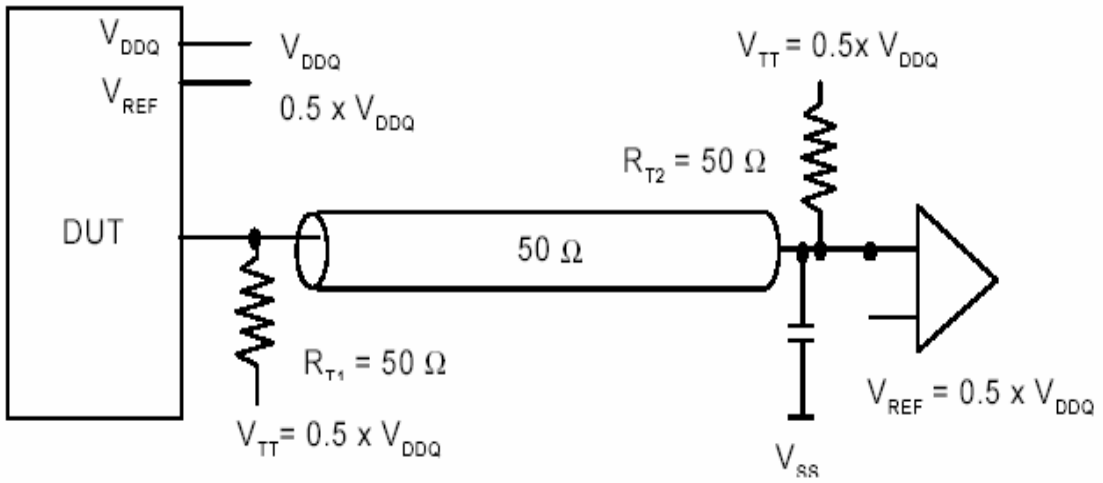


Figure 9 — Example of SSTL_2, Class I, buffer with symmetrically double parallel terminated output load

For bus systems which must be terminated at both sides: the drivers are connected directly onto the bus so **there are no stubs present**.
In that case, the designer may decide to eliminate the series resistors entirely.
This application can be implemented using a Class I or Class II driver and SSTL_2 receiver (however a Class II buffer would dissipate more power due to its larger current drive and thus might require special cooling).

Notes on Logic standards

- **Example: SSTL_2 differential signals interconnection**

The following specifications were added to JESD8-9 base standard (single ended logic). This is particularly relevant to DDR DRAM clock signals.

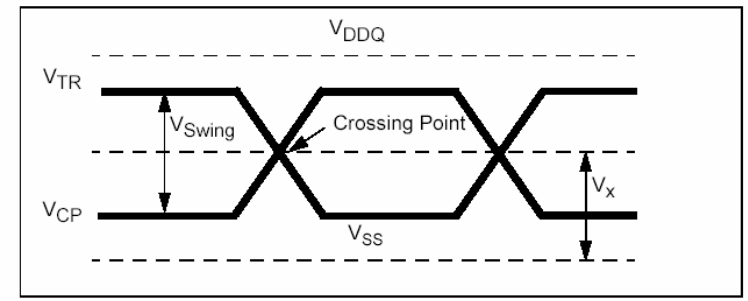


Figure 10 — SSTL_2 differential input levels

Differential input logic levels

	Min	**Max**
VIN(dc)	(-0.30V)	(Vddq + 0.30V)
VSwing(dc)	(0.30V)	(Vddq + 0.6 V)
VSwing(ac)	(0.62V)	(Vddq + 0.6 V)
Vx(ac)	(0.5 x Vddq) +/- 200mV	

Notes on Logic standards

- **Example: SSTL_2 differential signals interconnection**

The following specifications were added to JESD8-9 base standard (single ended logic). This is particularly relevant to DDR DRAM clock signals.

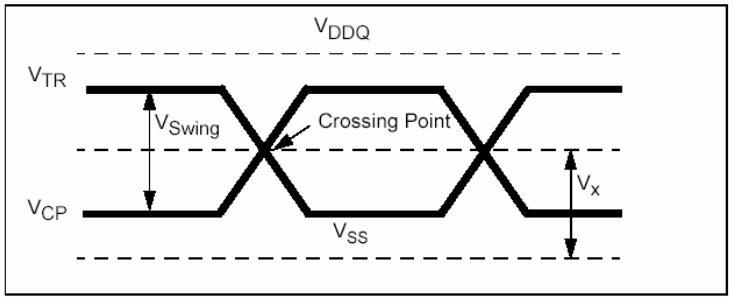


Figure 10 — SSTL_2 differential input levels

Differential input AC test conditions

Input timing measurement reference level: Vx crosspoint
Input signal peak to peak swing voltage: 1.5V max
Input signal slew rate: 1.0V/ns min
Periodic clock inputs: clock duty cycle 45% to 55%

Notes on Logic standards

- **Example: SSTL_2 differential signals termination (class I)**

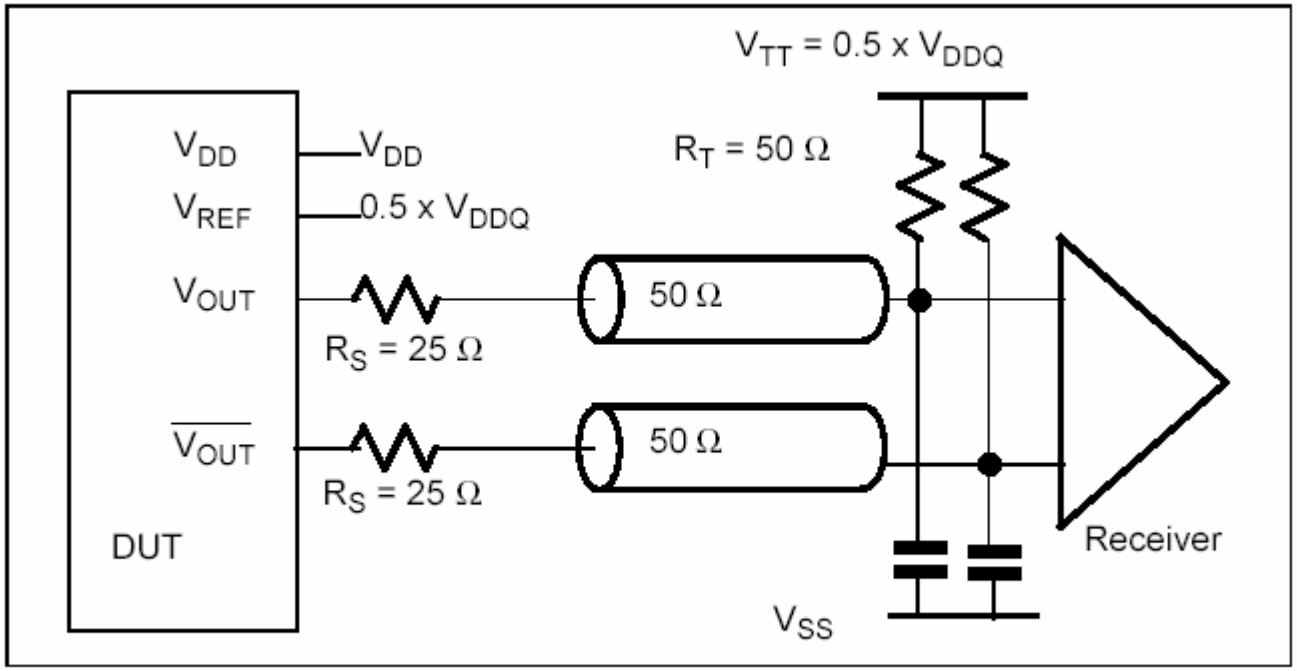


Figure 12 — Example of SSTL_2 class I, differential signal using single load, and series resistor.

Notes on Logic standards

- **Example: SSTL_2 differential signals termination (class I)**

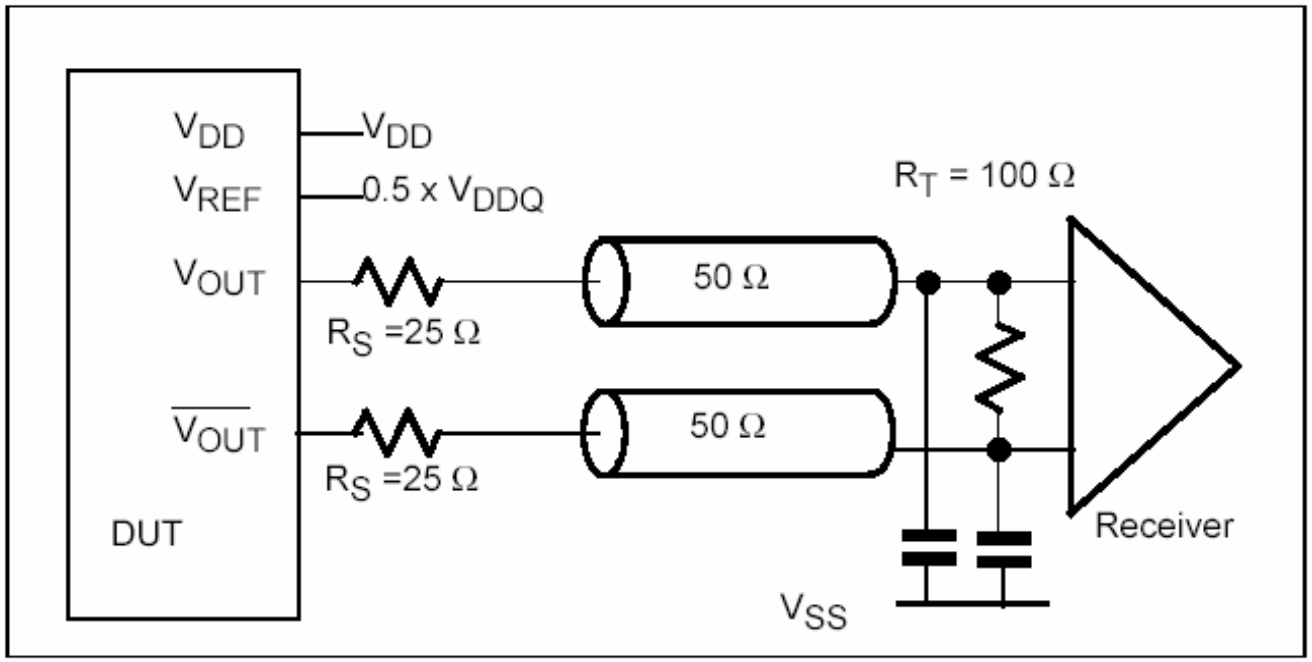


Figure 13a — Example of SSTL_2 Class I differential signal using direct termination resister, and series resistor. (Reference only)

Notes on Logic standards

- **Example: SSTL_18 differential signals termination (class I)**

3.2.1 Push-pull output buffer for symmetrically double parallel terminated loads with series resistor (V_{TT} = 0.5 * V_{DDQ})

Table 5 — Output dc current drive

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{OH(dc)}$	Output minimum source dc current	-13.4	-	mA	1, 3, 4
$I_{OL(dc)}$	Output minimum sink dc current	13.4	-	mA	2, 3, 4

Differential output parameters

Differential outputs may be created using either true differential drivers or by combining pairs of SSTL_18 compliant, single-ended drivers driven from true and complementary signals. As a result, differential output parameters are assumed to be identical to those for single-ended outputs except for additional specifications provided in Table 10.

Table 10 — Differential AC Output Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{OX(ac)}$	ac differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

Notes on Logic standards

- **Example: SSTL_18 differential signals termination (class I)**

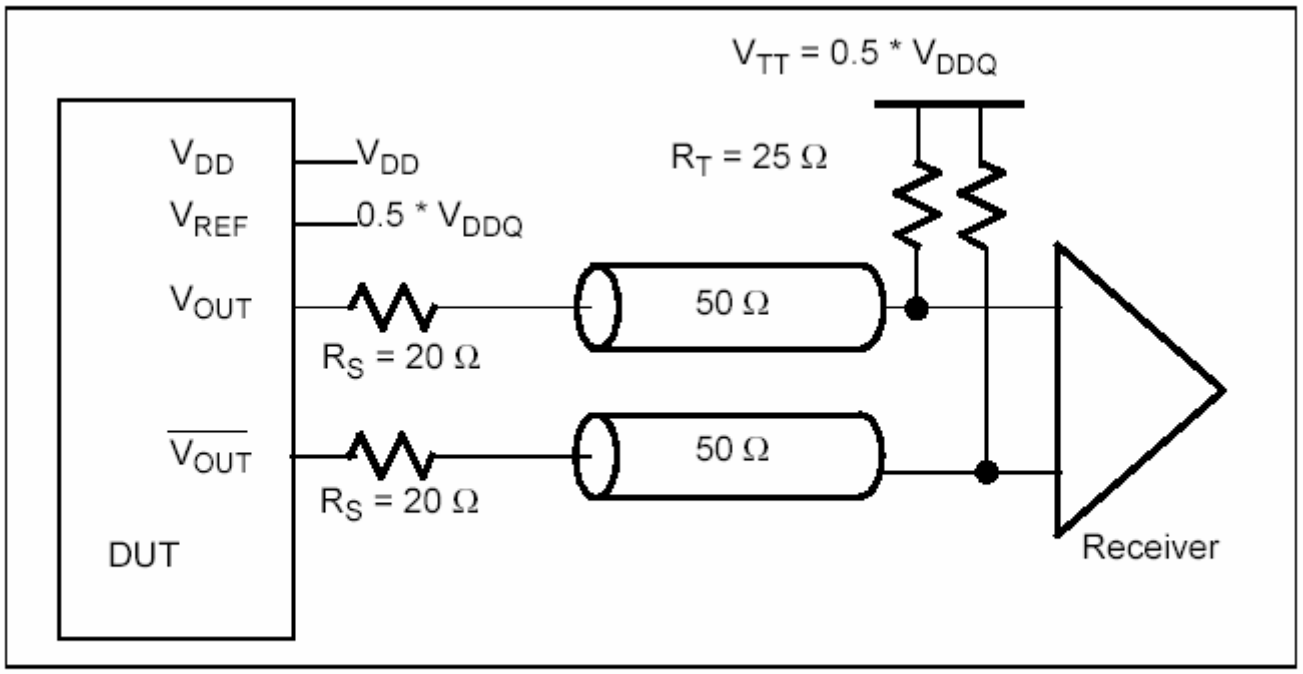


Figure 13 — Example of SSTL_18 differential signalling using series resistors and independent parallel termination resistors.

Notes on Logic standards

- **Example: SSTL_18 differential signals termination (class I)**

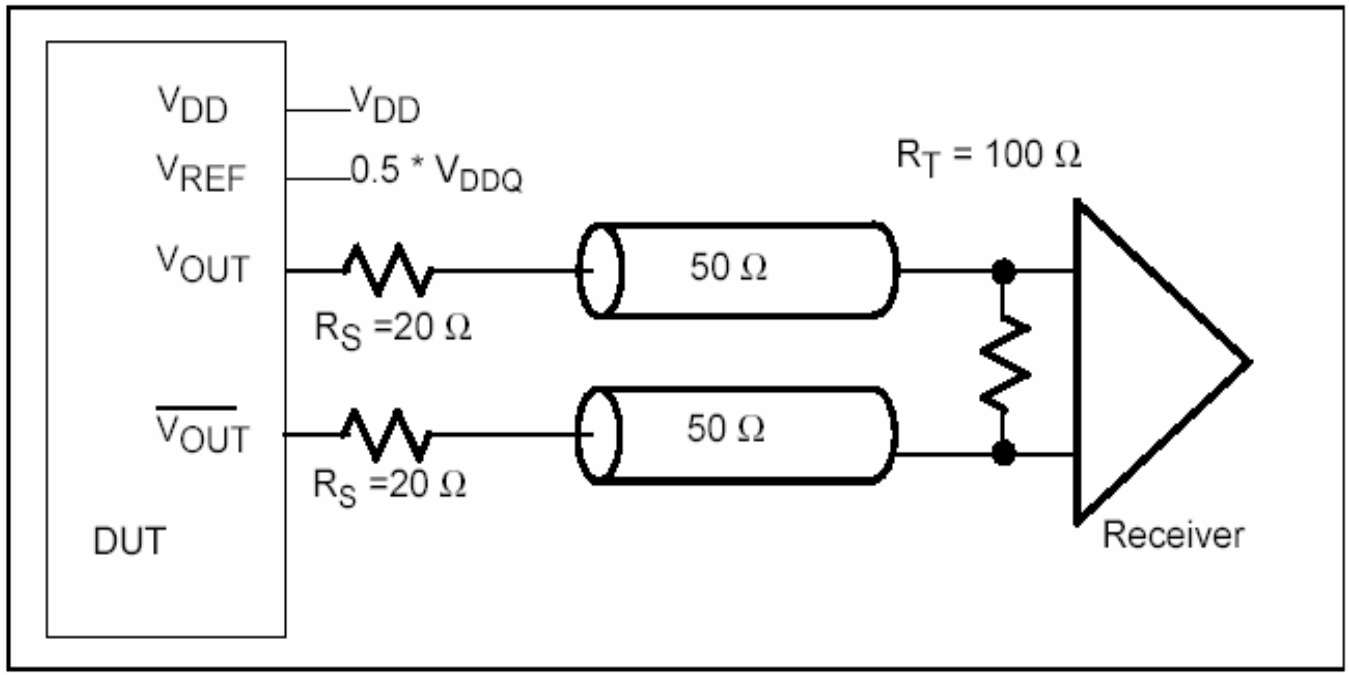


Figure 14 — Example of SSTL_18 differential signalling using series resistors and a differential termination resistor.

Notes on Logic standards

- **HSTL Description**

HSTL [High Speed Transceiver Logic] is an electrical interface defined by JEDEC/EIA standard **JESD8-6**.
Commonly used with DDR3 [Double Data Rate] DRAM memory IC and memory modules (standard JEDEC/EIA JESD79-3B).

Logic designed to operate at **1.5V output buffer supply voltage**.
Standard defines single ended and differential input buffer specifications as well as various push-pull output driver specifications.

Notes on Logic standards

- **HSTL Electrical Levels**

Output drivers are classified in four types:

Class I:	IOH = -8mA	IOL = +8mA	(VTT=0.75V, RT=50ohm)
Class II:	IOH = -16mA	IOL = +16mA	(VTT=0.75V, RT1=RT2=50ohm)
Class III:	IOH = -8mA	IOL = +24mA	(VTT=1.5V, RT=50ohm)
Class IV:	IOH = -8mA	IOL = +48mA	(VTT=1.5V, RT1=RT2=50ohm)

HSTL_15 (Class I, II)	Vtt = 0.5 x Vddq = Vref = 0.75V
HSTL_15 (Class III, IV)	Vtt = Vddq, Vref = 0.6 x Vddq = 0.9V

Notes on Logic standards

- **HSTL Electrical Levels (Class I, II, III, IV)**

Single ended input logic levels

	Min	**Max**
VIH(dc)	(Vref + 0,10V)	(Vddq + 0.30V)
VIL(dc)	(-0.30V)	(Vref – 0.10V)
VIH(ac)	**(Vref + 0.20V)**	
VIL(ac)		**(Vref – 0.20V)**

Vin: Vref +/-200mV

Single ended output logic levels

	Min	**Max**
VOH(dc)	(Vddq - 0.40)	
VOL(dc)		(0.40V)
VOH(ac)	**(Vddq - 0.50)**	
VOL(ac)		**(0.50V)**

Vout: Vref +/- 250mV

Notes on Logic standards

- **HSTL Electrical Levels (Class I, II, III, IV)**

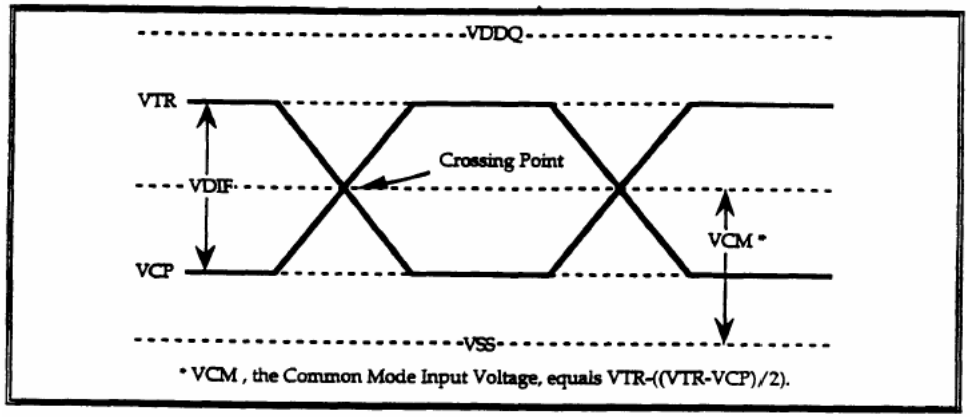


Figure 2.3 — HSTL differential input levels

Differential input logic levels

	Min	Max
VIN(dc)	(-0.30V)	(Vddq + 0.30V)
Vdif(dc)	(0.20V)	(Vddq + 0.60V)
VCM(dc)	(0.68V)	(0.90V)
Vdif(ac)	**(0.40V)**	**(Vddq + 0.60V)**
Vx(ac)	(0.68V)	(0.90V)

Differential input AC test conditions

Input timing measurement reference level: 0.75V
Input signal peak to peak swing voltage: 1.0V
Input signal slew rate: +/- 1.0V/ns

Vdif = +/- 400mV,

Vcm = 0.75V - 70mV to 0.75V +150mV

Notes on Logic standards

- **Example: HSTL_15 output driver termination (class I)**

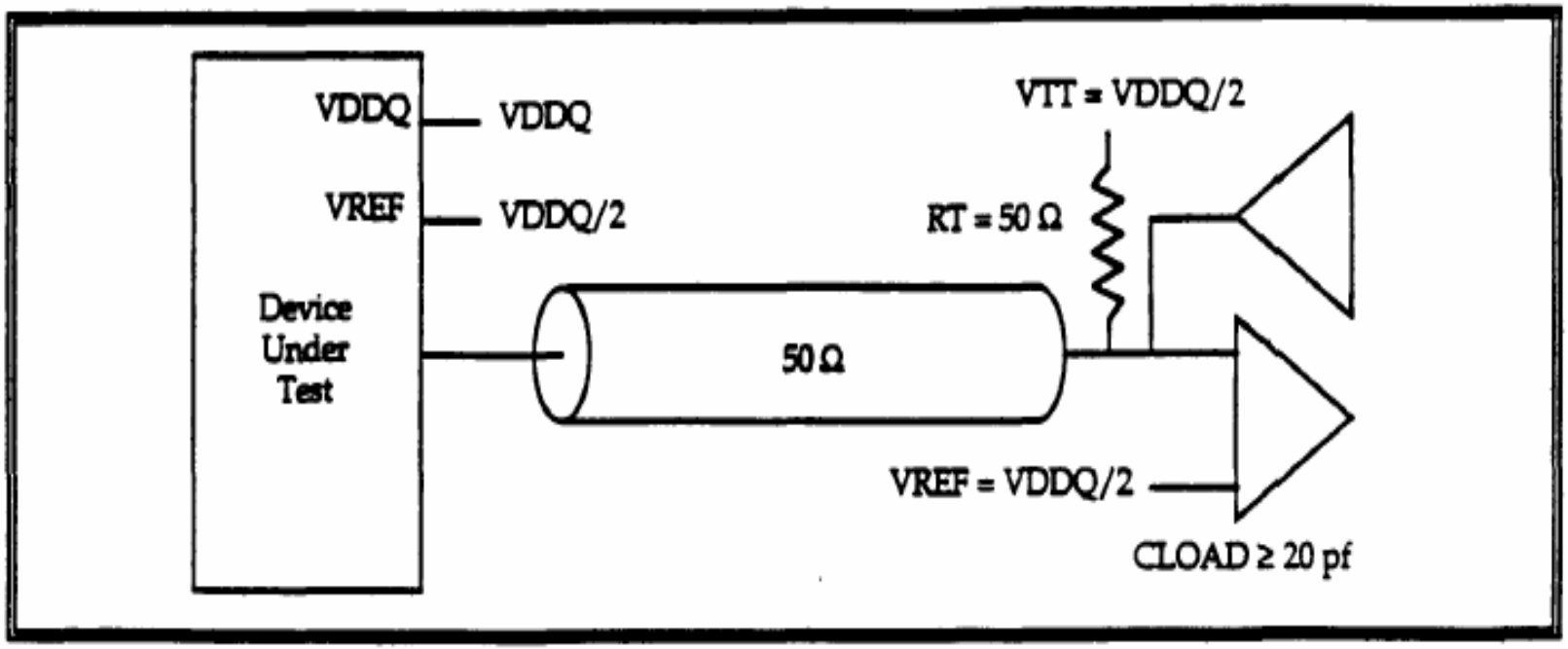


Figure 3.1-b — An example HSTL symmetrically parallel terminated output load and Class I HSTL ac test load diagram

Notes on Logic standards

- **Example: HSTL_15 output driver termination (class II)**

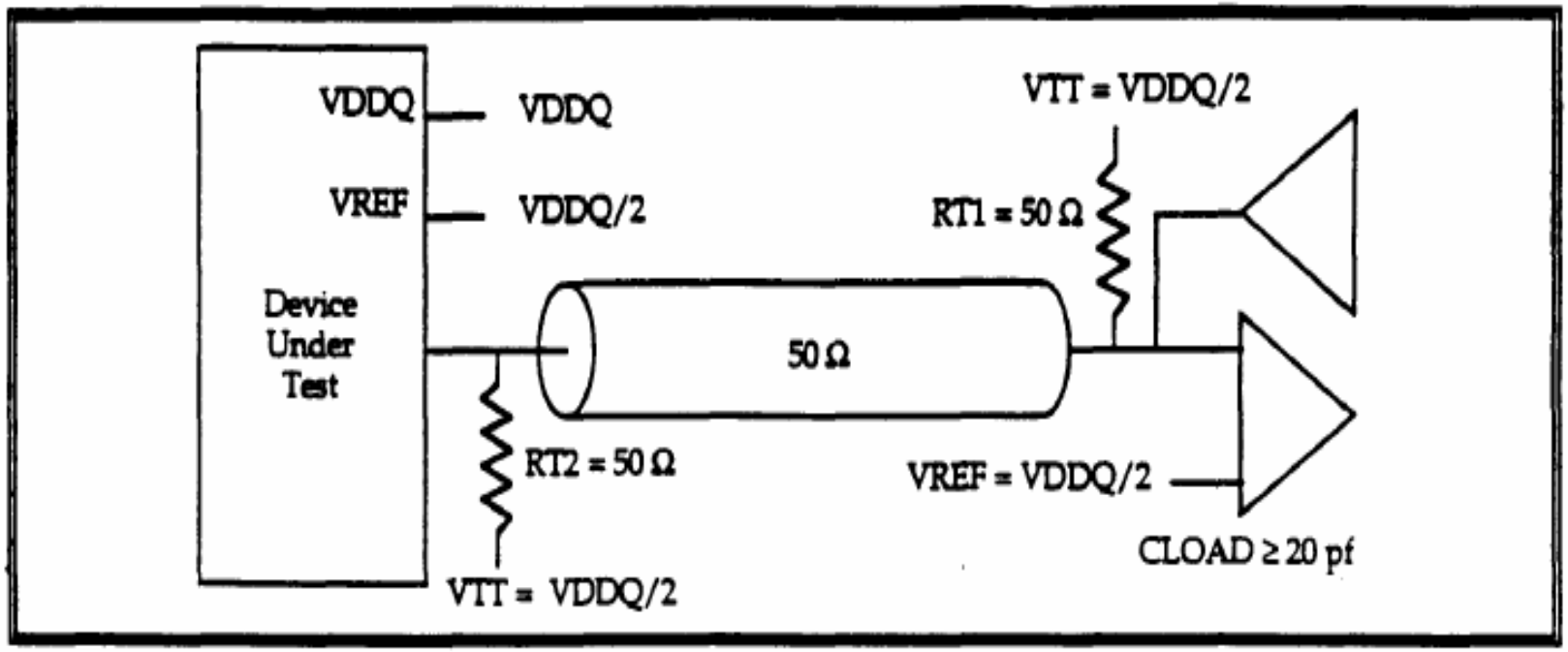


Figure 3.2-b — An example HSTL symmetrically double parallel terminated output load and Class II HSTL ac test load diagram

Notes on Logic standards

- **Example: HSTL_15 output driver termination (class III)**

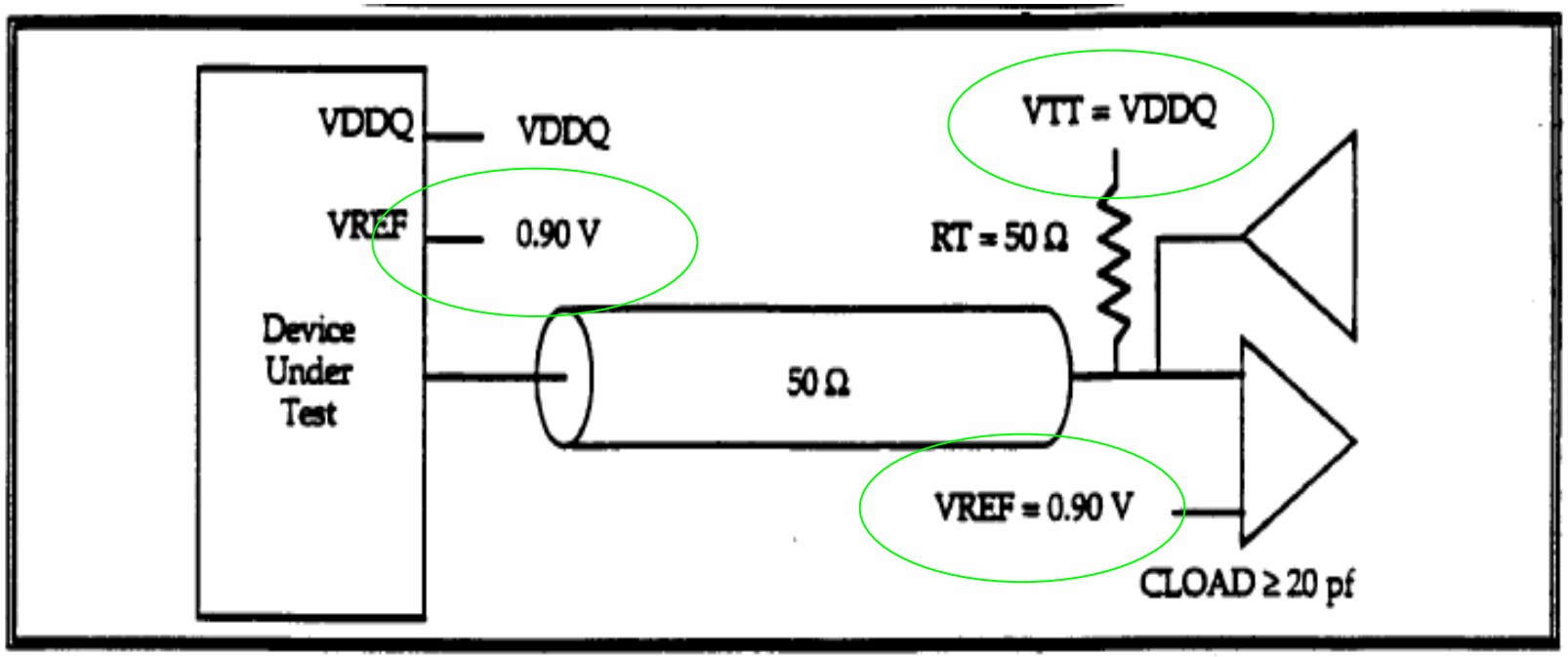


Figure 3.3-a — An example HSTL asymmetrically parallel terminated output load and Class III HSTL ac test load diagram

Notes on Logic standards

- **Example: HSTL_15 output driver termination (class IV)**

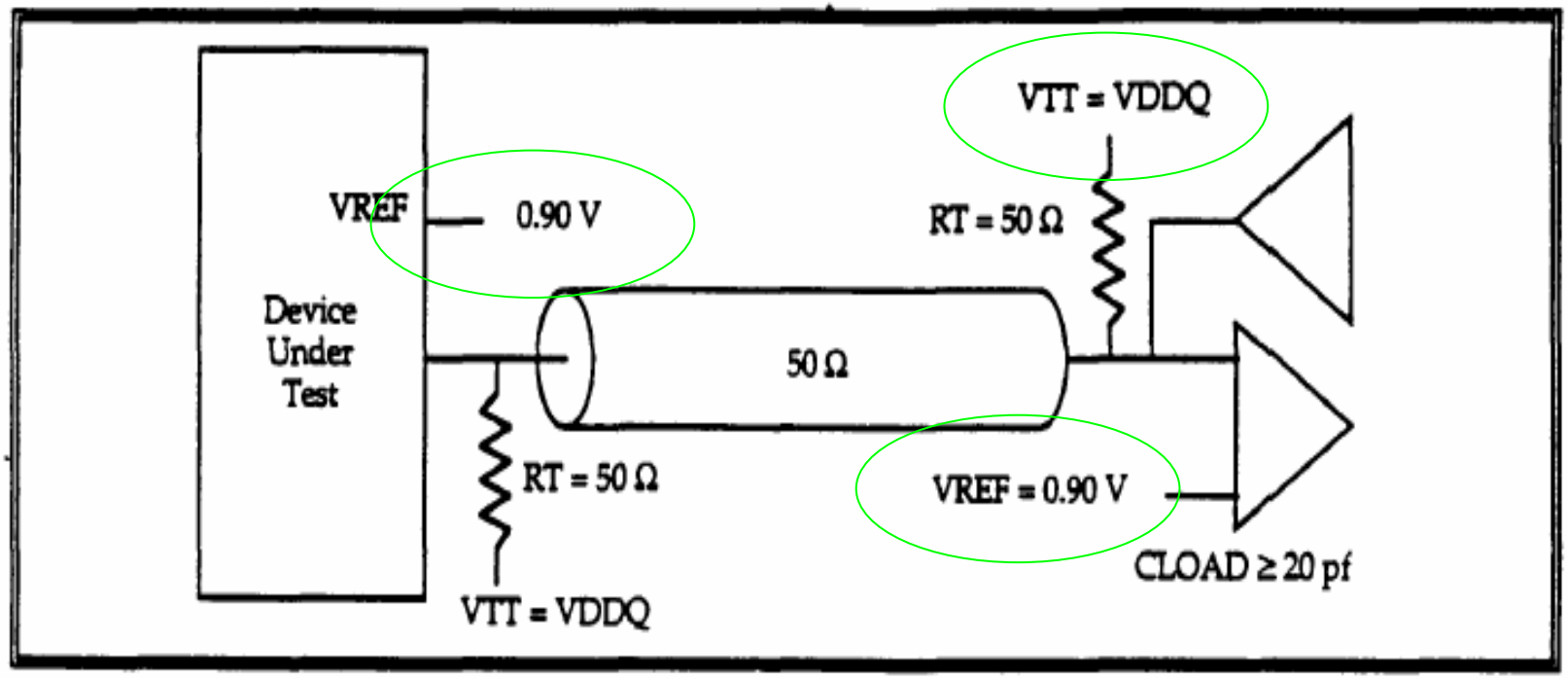


Figure 3.4-a — An example HSTL asymmetrically double parallel terminated output load and class IV HSTL ac output load diagram

Notes on Logic standards

- **BIC (HSTL_12) Description**

BIC [Bus interconnect logic] is an electrical interface defined by JEDEC/EIA standard **JESD8-16a**.

Designed to operate at **1.2V output buffer supply voltage**.

(Note: JEDEC defined standard JESD8-6, the HSTL standard, for use in 1.5V electrical environments. BIC is similar to HSTL, except the power supply voltage has dropped from 1.5V to 1.2V, and interface requirements are tightened to allow much higher speeds.
Sometimes BIC compatible i/o devices are also named **HSTL_12**).

Notes on Logic standards

- **BIC (HSTL_12) Description**

BIC is optimized for use with on die termination (ODT).
In some applications, this allows the components on the interface to be actively tuned for optimum performance and low noise under varying conditions.

BIC is defined in both a differential form and a single ended with VREF form. While the two versions have different signal requirements and are not fully interchangeable, they are compatible at the signal level and can be interconnected with minimal performance degradation.

Notes on Logic standards

- **BIC (HSTL_12) Description**

The **single ended version** has been optimized for parallel bus operation, **requiring termination at both the source and receiver** (it is expected that all termination will be on die, eliminating the need for external resistors, but external resistive components are compatible with BIC).

The **differential version** has been optimized for distributing clock signals or other very high-speed signals where signal integrity is critical.
Differential BIC can also be used for parallel busses (if the user can tolerate the extra signal lines required for differential signaling).

Notes on Logic standards

- **BIC (HSTL_12) Description**

BIC has three output classes:

BIC Class 1 (BIC1) has been optimized for driving 50 ohm environments or transmission lines.

BIC Class 2 (BIC2) has been optimized for driving 25 ohm environments (e.g. a 50 ohm transmission line with a 50 ohm termination at both ends).

BIC Class 3 (BIC3) allows a user to adjust the device output impedance between 40 ohm and 50 ohm or a larger vendor specified range.

Notes on Logic standards

- **BIC (HSTL_12) Electrical Levels (Class I, II, III)**

Supply voltage levels (V):

	Min	**Nom**	**Max**
Vddq	(1.14)	(1.2)	(1.26)
Vref(dc)	(0.48 * Vddq)	(0.50 * Vddq)	(0.52 * Vddq)
Vref(ac)	(0.47 * Vddq)	(0.50 * Vddq)	(0.53 * Vddq)
VTT		(Vddq / 2)	

Notes on Logic standards

- **BIC (HSTL_12) Electrical Levels (Class I, II, III)**

Single ended input logic levels (V)

	Min	**Max**
VIH(dc)	(Vref + 0,08)	(Vddq + 0.15)
VIL(dc)	(-0.15)	(Vref – 0.08)
VIH(ac)	**(Vref + 0.15V)**	(Vddq + 0.24)
VIL(ac)	(-0.24)	**(Vref – 0.15V)**

Single ended output logic levels (V) (class type dependent, for details see standard tables; typ values for well-balanced termination)

	Typ
VOH(ac, dc)	(Vddq * 0.75)
VOL(ac, dc)	(Vddq * 0.25)

Vout (typ) = (1.2V / 2) +/- 300mV

Notes on Logic standards

- **BIC (HSTL_12) Electrical Levels (Class I, II, III)**

Differential input logic levels (V)

	Min	**Nom**	**Max**
VIX		(0.5 * Vddq)	
Vdif (dc)	(0.16)		(Vddq + 0.30)
Vdif (ac)	**(0.30)**		(Vddq + 0.48)
Vcm(dc)	**(0.4 * Vddq)**	**(0.5 * Vddq)**	**(0.6 * Vddq)**
VIN (dc)	(-0.15)		(Vddq + 0.15)
VIN (ac)	(-0.24)		(Vddq + 0.24)

Differential output logic levels (V)

	Min	**Nom**	**Max**
VOX		(0.5 * Vddq)	
VOH (dif)		defined by class type	
VOL (dif)		defined by class type	
VOUT (dc)	(-0.15)		(Vddq + 0.15)
VOUT (ac)	(-0.24)		(Vddq + 0.24)

Notes on Logic standards

- **BIC (HSTL_12) Output driver termination (Class I)**

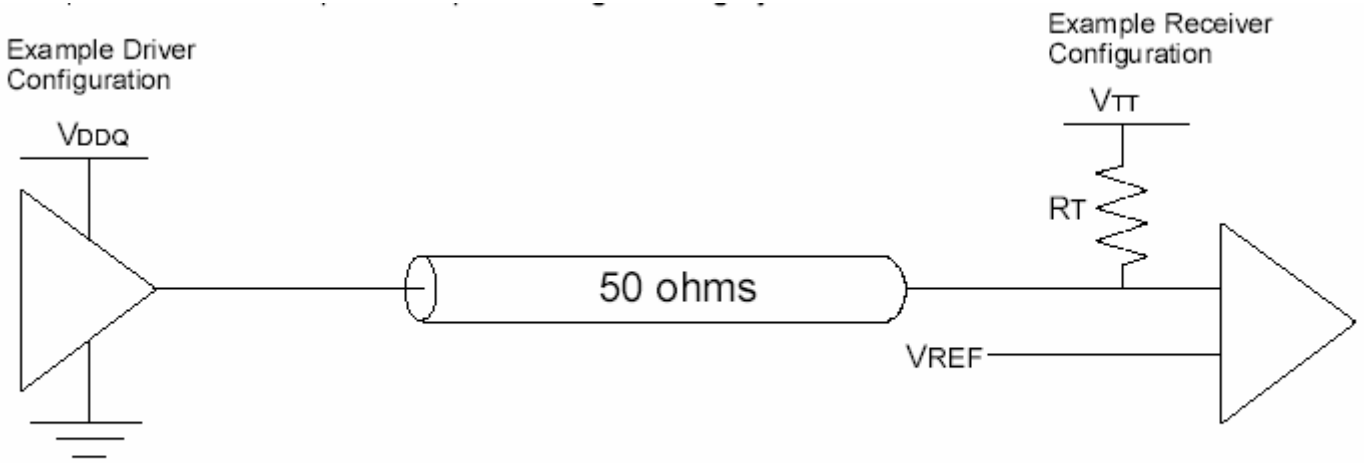


Figure 3 — Example of BIC Class 1 usage

Figure 3 shows a possible usage of BIC1 in a unidirectional application. The termination resistor RT may be either an “on die” termination or an external resistor. The source impedance of BIC1 is approximately 44 ohm, and is intended for use in a point-to-point application. The value of RT should be set to provide optimum signal integrity at the receiver.

Notes on Logic standards

- **BIC (HSTL_12) Output driver termination (Class II)**

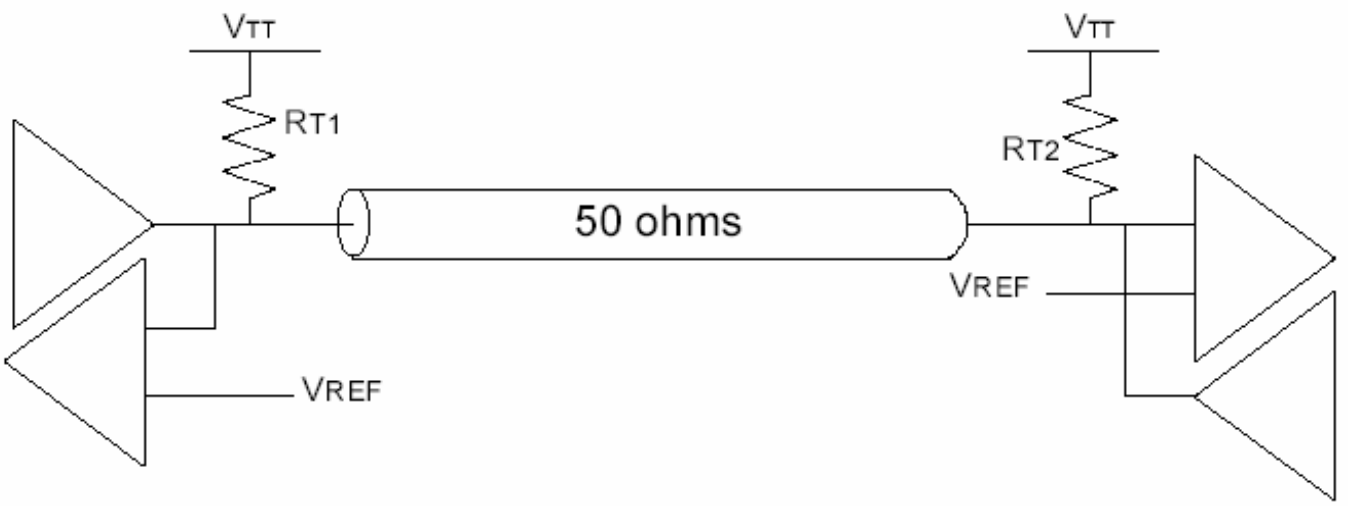


Figure 4 — Example of BIC Class 2 usage

Figure 4 shows a possible usage of BIC2 in a bi-directional application. The termination resistors RT may be either “on die” termination or external resistors. The approximately 22 ohm source impedance of BIC2 drivers has been set to drive the parallel impedances of the transmission line and the termination resistor RT at the near end. At the far end of the transmission line, the termination resistor should match the transmission line impedance, providing optimum signal integrity.

Notes on Logic standards

- **BIC (HSTL_12) Output driver termination (Class III)**

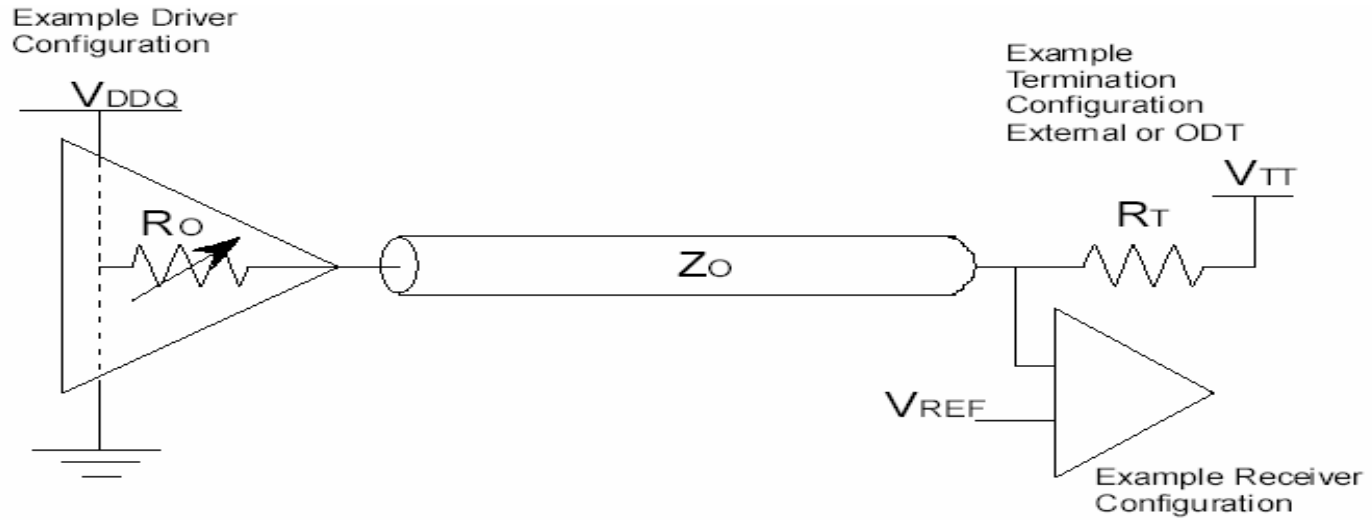


Figure 5 — Example of BIC Class 3 usage

Figure 5 shows an example of a BIC3 adjustable impedance output, driving a single load in a point-to-point application utilizing external termination. Through the adjustment of Ro, BIC3 can be adapted for other applications, including bi-directional, multi-drop, and ODT.

Notes on Logic standards

- **CML**

CML [current mode logic] is a high-speed point-to-point interface capable of data rates in excess of 10 Gbps.

CML uses a passive pull-up to the positive rail, which is typically 50 ohm.

There is no standard so **CML tends to be vendor specific**
(note: while not explicitly standardized, CML implementations can meet the requirements of Clause 47 of the IEEE 802.3 standard that defines the physical layer of the XAUI interface).

Notes on Logic standards

- **CML output levels**

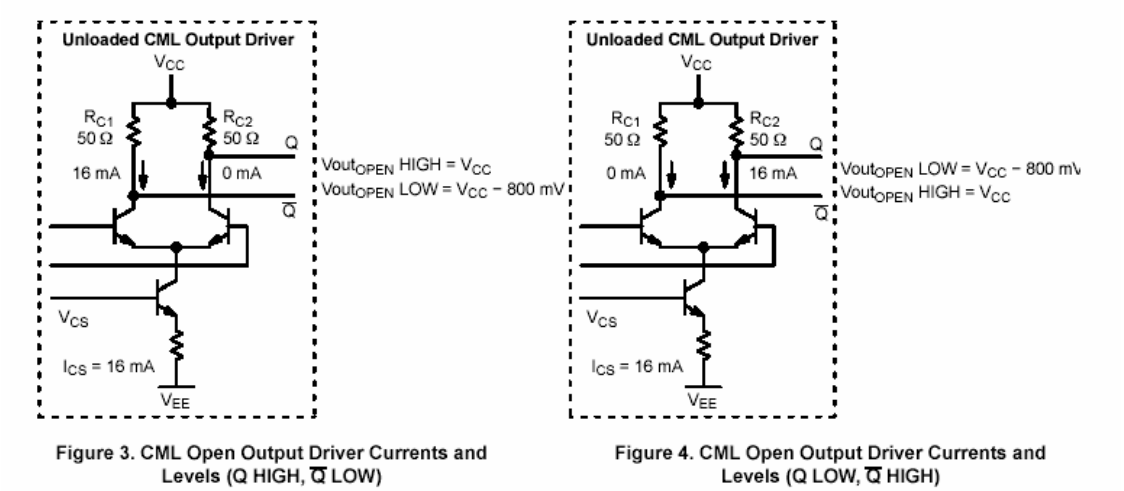


Figure 3. CML Open Output Driver Currents and Levels (Q HIGH, $\overline{Q}$ LOW)

Figure 4. CML Open Output Driver Currents and Levels (Q LOW, $\overline{Q}$ HIGH)

Table 1. CML DRIVER LEVELS (with Open, Unloaded Outputs)

Parameter	Level	Unit
$V_{OUT_{OPEN\ HIGH}}$	V_{CC}	
$V_{OUT_{OPEN\ CM}}$	V_{CC} − 400	mV
$V_{OUT_{OPEN\ LOW}}$	V_{CC} − 800	mV
$V_{OUT_{OPEN\ SE}}$ (Note 1)	800	mVpp
$V_{OUT_{OPEN\ DIFF}}$	1600	mVpp

1. Each line measured single−ended.

Vout = (Vcc - 800mV) to (Vcc)

(unloaded outputs)

Notes on Logic standards

- **CML output levels**

Vout = (Vcc - 400mV) to (Vcc)

(loaded outputs)

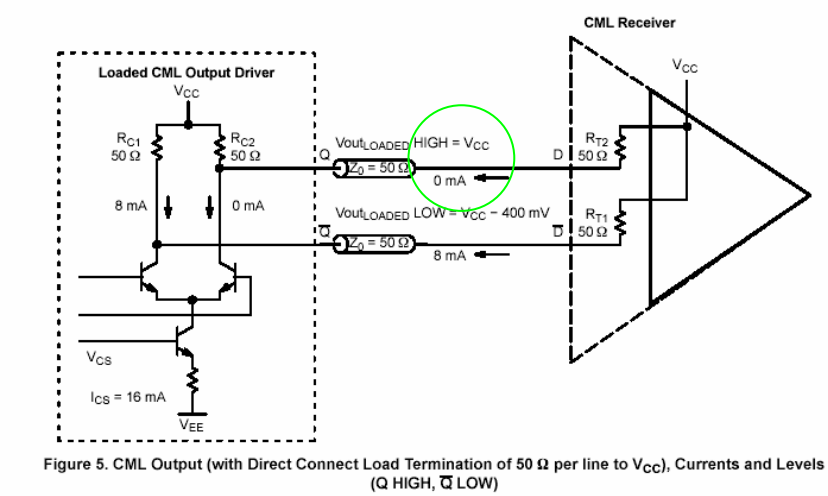


Figure 5. CML Output (with Direct Connect Load Termination of 50 Ω per line to V_{CC}), Currents and Levels (Q HIGH, $\overline{Q}$ LOW)

Table 2. CML DRIVER LEVELS (with Direct Connect Load Termination of 50 Ω to V_{CC})

Parameter	Level	Unit
$Vout_{LOADED}$ HIGH	V_{CC}	
$Vout_{LOADED}$ CM	V_{CC} – 200	mV
$Vout_{LOADED}$ LOW	V_{CC} – 400	mV
$Vout_{LOADED}$ SE (Note 2)	400	mVpp
$Vout_{LOADED}$ DIFF	800	mVpp

2. Each line measured single−ended.

When the output is connected to a current source (loaded), the driver's internal constant 16mA tail current, ICS, now draws from the active side transistor through the internal 50 ohm RC (collector resistor), and also through the receiver's 50 ohm (RT) termination to a current source.

A typical receiver termination (internal or external termination resistor) is 50 ohm to VCC as shown in Figures 5. Both output lines in a differential pair should have equal loads to maintain balanced dynamic signal loading to the driver. **The complementary side draws essentially zero current Ioff and remains near VCC.**

Notes on Logic standards

- **CML line termination**

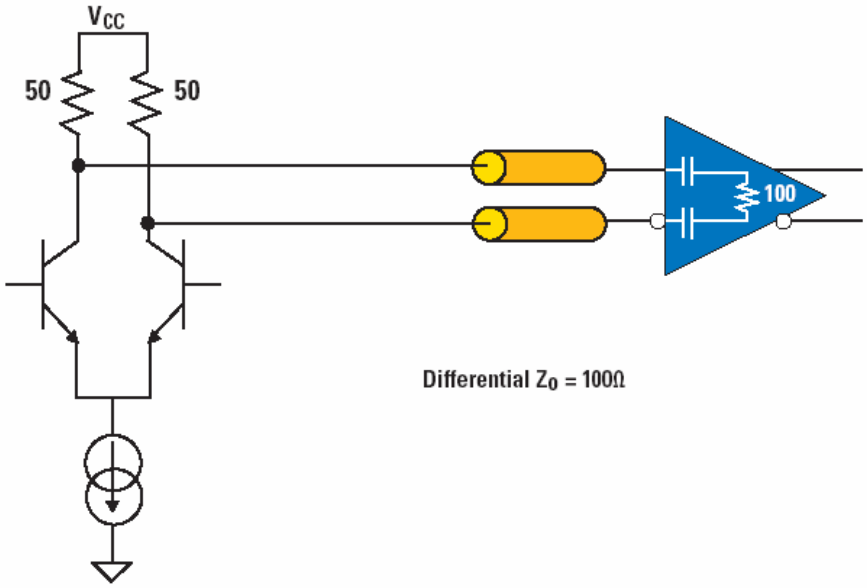


Figure 1-4. Typical CML Implementation

As shown in ***Figure 1-4***, a common feature of CML is that termination networks are integrated typically into both drivers and receivers.
Most implementations of CML are AC coupled, and therefore require DC-balanced data (DC-balanced data tests require data coding that contain, on average, an equal number of ones and zeros).

Notes on Logic standards

- **CML line termnation**

Vout = Vterm +/- 200mV

(ac coupled loaded outputs)

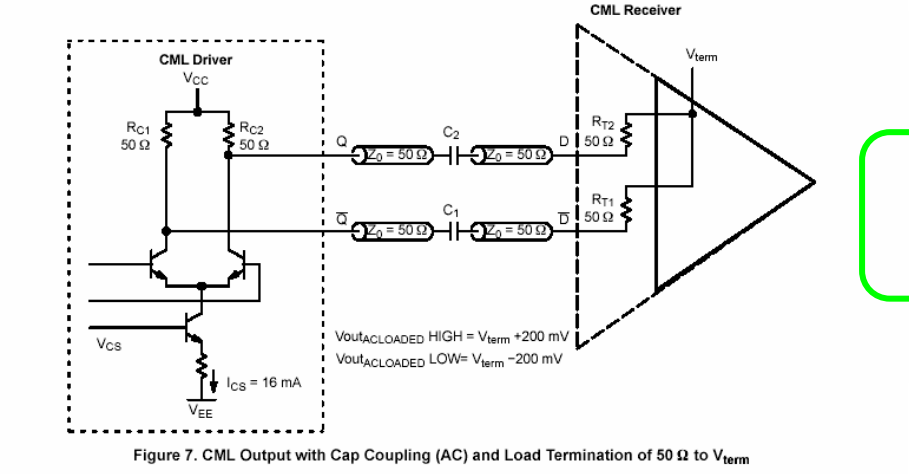


Figure 7. CML Output with Cap Coupling (AC) and Load Termination of 50 Ω to V_{term}

Table 3. CML DRIVER LEVELS (with Cap Coupled Termination of 50 Ω per line to V_{CC})

Parameter	Receiver Level	Unit
$Vout_{AC}$ LOADED HIGH	V_{term} + 200	mV
$Vout_{AC}$ LOADED CM	V_{term}	mV
$Vout_{AC}$ LOADED LOW	V_{term} − 200	mV
$Vout_{AC}$ LOADED SE (Note 3)	400	mVpp
$Vout_{AC}$ LOADED DIFF	800	mVpp

3. Each line measured single−ended.

A driver and receiver using a cap, Cx, coupled (AC) differential interconnect and receiver side 50 ohm termination (RT) requires a DC receiver side rebiasing, Vterm, to the signal lines as shown in Figure 7. The coupling cap, Cx, value and the load impedance constitute an RC network affecting the signal edges. Cap coupling (AC) restricts low frequency response and may require coding to maintain a sufficient crossing density.

Notes on Logic standards

- **Example: CML driver direct connected (dc) to LVPECL**

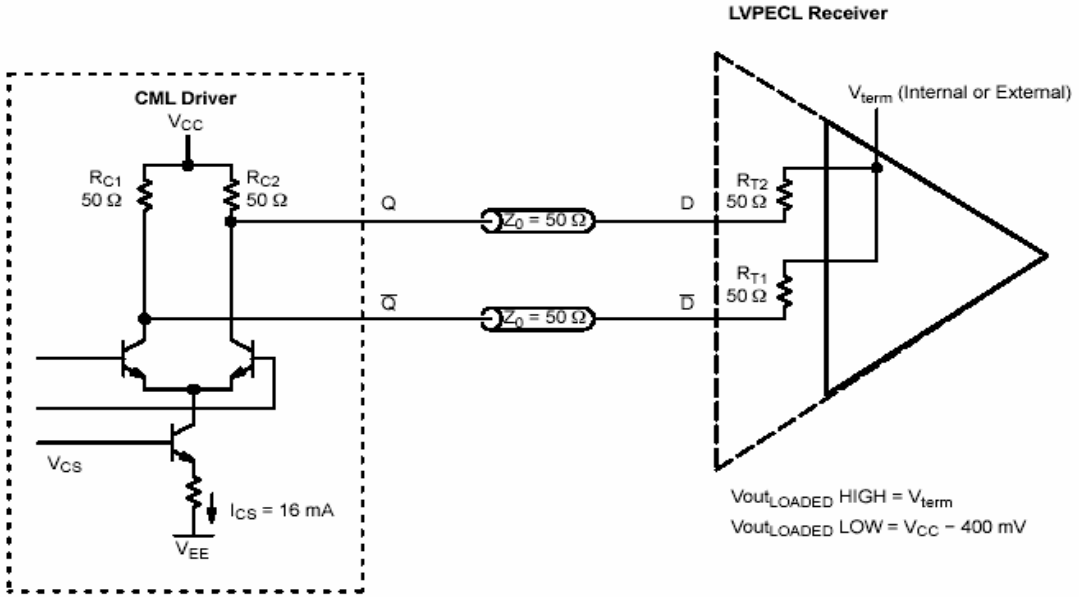


Figure 10. CML Output with Direct (DC) Interconnect and Termination of 50 Ω to V_{term}

Table 5. CML DRIVER LEVELS (WITH DIRECT CONNECT TERMINATION OF 50 Ω PER LINE TO V_{term})

V_{term}	$Vout_{CM}$	$Vout_{HIGH}$	$Vout_{LOW}$	$Vout_{PP}$ (Note 4)	Unit
3.3	3.1	3.25	2.95	0.300	V
3.0	2.95	3.10	2.85	0.300	V
2.5	2.75	2.85	2.55	0.295	V

4. Each line measured single−ended

Notes on Logic standards

- **Example: CML driver direct connected (dc) to LVPECL**

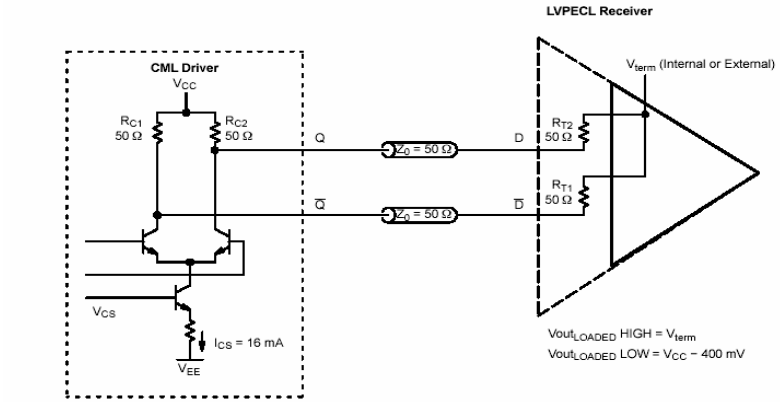


Figure 10. CML Output with Direct (DC) Interconnect and Termination of 50 Ω to V_{term}

Table 5. CML DRIVER LEVELS (WITH DIRECT CONNECT TERMINATION OF 50 Ω PER LINE TO V_{term})

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3.3	3.1	3.25	2.95	0.300	V
3.0	2.95	3.10	2.85	0.300	V
2.5	2.75	2.85	2.55	0.295	V

4. Each line measured single−ended

From On-semi app.note AND8173/D (“Termination and Interface of On Semiconductor ECL Devices With CML (Current Mode Logic) OUTPUT Structure”):

“A proper Vterm DC bias must be selected for the receiver to comply with common mode specifications, such as VIHCMR or VCMR. Most devices will tolerate Vterm at VCC while others may spec a signal HIGH level, VIHmax (consult device data sheet) requiring an appropriately lower Vterm supply (a lower Vterm supply affects the receiver VoutHIGH and VoutLOW levels). A typical On Semiconductor ECL Device with CML OUTPUT Structure, directly (DC) driving an internally terminated LVPECL input with various Vterm values, produces a characteristic swing amplitude, VoutPP (each line is measured single ended), and a common mode voltage, VoutCM, presented in Table 5.
Both CML driver and LVPECL receiver were supplied VCC @ 3.3 V.
Note the insensitivity of the output swing to changes in the Vterm supply as it ranges from VCC to VCC - 2.0V, the typical VTT termination voltage for Emitter Follower ECL structures ”.

Notes on Logic standards

- **LVDS**

LVDS [Low Voltage Differential Signaling] is a high-speed and low-power differential interface for generic applications.

It supports both point-to-point and also multidrop bus configurations.

LVDS is standardized as an electrical layer standard by the TIA and is published as **ANSI/TIA/EIA-644-A.**

Notes on Logic standards

- **LVDS**

LVDS driver provides a typical 350mV differential output voltage centered at about +1.25V.

The receiver is specified with a 100mV threshold over the **receiver's input range of ground to +2.4V** (this allows for the nominal active signal to shift up or down 1V in common-mode due to ground potential differences or coupled noise).

The driver is intended to be used with 100-Ohm interconnects terminated in 100-Ohms.

Data rate is device and application specific but it tends to be in the DC to 2.5Gbps range.

Notes on Logic standards

- **LVDS**

LVDS is unique in that it delivers high-speed operation while consuming little power.
Power is minimized in three ways:
- the load current is limited to 3.5mA
- the current mode driver tends to limit dynamic power dissipation
- static current is minimized by the use of sub-micron CMOS processes.

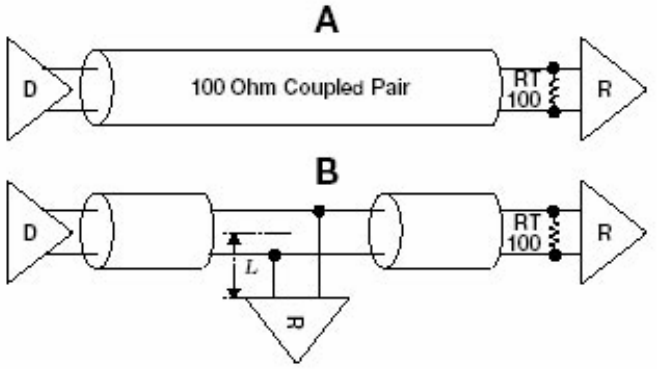
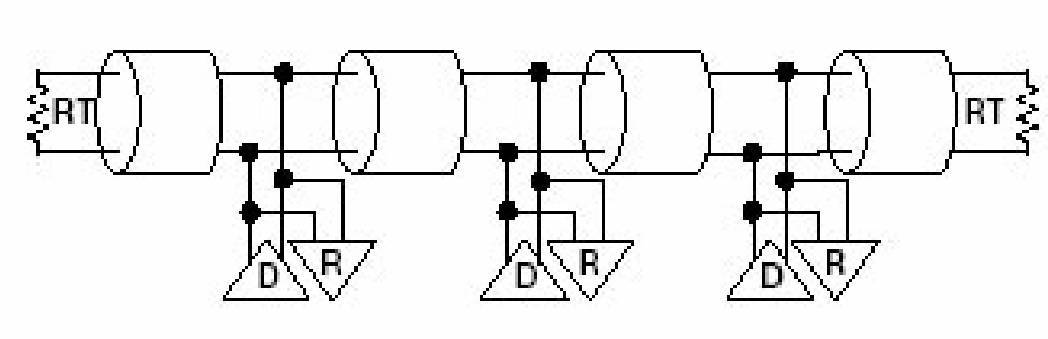


Figure 2: A: LVDS terminated by 100 Ohm parallel termination; B: Multidrop LVDS terminated by 100 Ohm parallel termination at the far end only, stubs off the main line should be minimized in length.

Notes on Logic standards

- **M-LVDS**

A newer related LVDS standard is the ANSI/TIA/EIA-899 known as M-LVDS: this version supports a multipoint bus with double terminations. Due to the bus configuration and stub lengths, M-LVDS is limited to 500 Mbps or less.



Multipoint LVDS bus terminated by two parallel terminations which are equal to 100 Ohms or the effective loaded impedance of the bus - typically in the 54 to 100 Ohm range