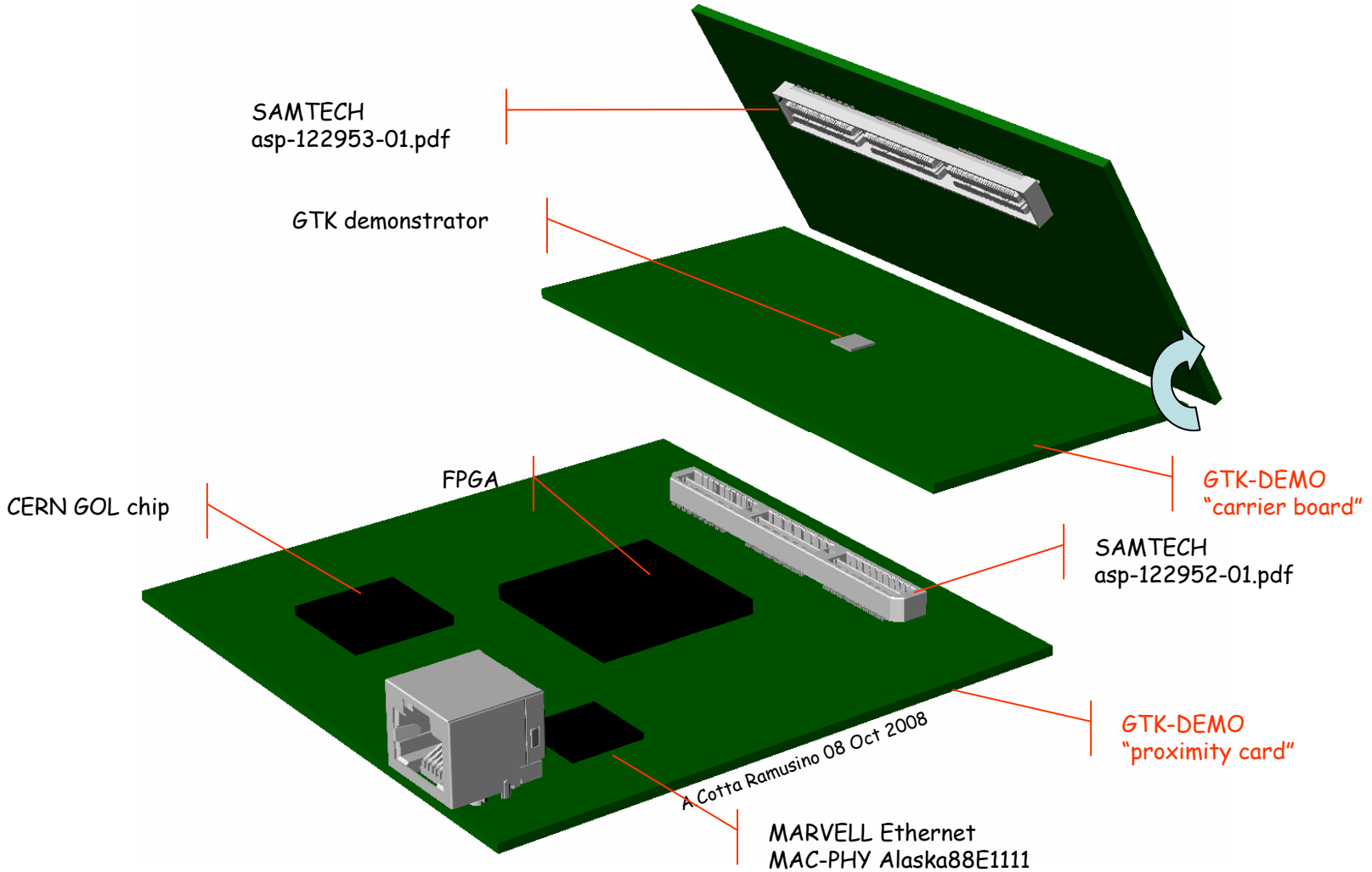


Testing of the GTK demonstrators

CERN - 07/08 Oct 2008, GKT design review

A.Cotta Ramusino INFN-FE

Testing of the GTK demonstrators

Summary:

- specifications for the "GTK proximity card"
- a proposal for the GTK demonstrators DAQ
- ALTERA FPGA resources: I/O standards, SER-DES units, memory and more
- XILINX FPGA resources: I/O standards, SER-DES units, memory and more
- ACTEL FPGA resources (brief)

Specifications for the "GTK proximity card"

The "GTK proximity" card must:

- **provide a low-jitter clock to the GTK ASIC** (160MHz to the INFN-TO GTK demonstrator ASIC, 320 MHz to the CERN GTK demonstrator ASIC) starting from a low-jitter 40MHz clock. The "GTK proximity" card should have an input port for a "system-wide" 40MHz clock in a **test (beam) setup** with multiple GTK ASICs and GTK proximity cards (eventually one board could have an on-board oscillator and act as a timing master for the others)

- **provide a "RESET" signal to the GTK ASIC**; the "RESET" timing could be determined by an external source (like the "Trigger Logic Unit-TLU" discussed later on) or by an internal source. Eventually one board could act as a "RESET" master for the other boards in a **test (beam) setup** with multiple "GTK proximity" cards

- **provide regulated power supplies to the GTK ASIC**

- **provide all programmable bias voltages needed by the GTK ASIC**. Remote controlled of these programming voltages is provided via an Ethernet "SLOW CONTROL" port

- **provide a "CALIBRATE" signal to the GTK ASIC**: the "CALIBRATE" timing could be determined by an external source or by an internal one (a "SLOW CONTROL" command for instance). Eventually one board could act as a "CALIBRATE" master for the other boards in a test beam setup with multiple "GTK proximity" cards

- **read out the GTK ASIC (+provide temporary data storage and trigger matching if a triggered DAQ is foreseen)**

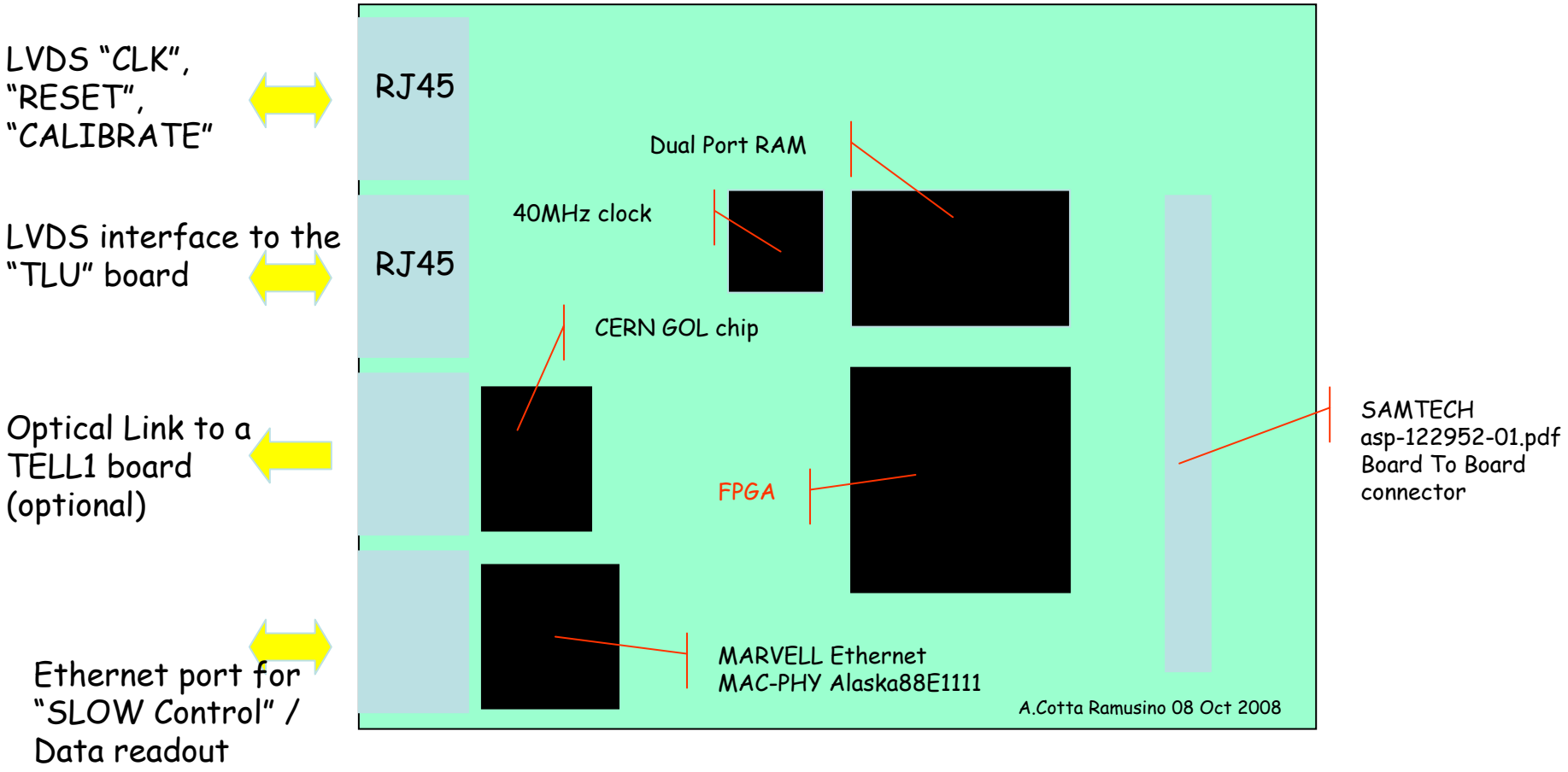
- **foresee a trigger input interface and resources for trigger matching** if the test (beam) setup foresees an experimental trigger (generated for instance by the "Trigger Logic Unit" introduced later on)

- **transfer readout data via a Gigabit Ethernet port** (MORE THAN 1 are needed?) to the test(beam) CPU farm

- **drive (optionally) the output data also through a CERN GOL chip + laser + fiber to a TELL1 board** (if there is enough time to attempt reading out the GTK demonstrator already with the LHCb's TELL1 board)

Specifications for the "GTK proximity card"

GTK-DEMO "proximity card" block diagram



Specifications for the "GTK proximity card"

Summary (as of last meeting) of the I/O signals for basic GTK operation and readout

#bit per porta	tipo della porta	direz. per la FPGA	nome della porta	freq. operativa	per GTK ASIC	note
1	diff LVDS / HyperTransport (LDT_25)	IN	**NA62Clk_IN**	@40.04MHz		
1	HyperTransport (LDT_25)	OUT	**GTK_CLK** = NA62Clk_IN * 4	≈ 160MHz	GTK-TO	sfruttando PLL interna a FPGA
1	diff LVDS	OUT	**GTK_CLK** = NA62Clk_IN * 8	≈ 320MHz	GTK-CERN	sfruttando PLL interna a FPGA
1	diff LVDS/ HyperTransport (LDT_25)	OUT	**GTK_SYNCH**		entrambi	
16	HyperTransport (LDT_25)	IN	GTK-TO**_data**	@ ≈ 160MHz	GTK-TO	
1	HyperTransport (LDT_25)	IN	GTK-TO**_DataValid**	@ ≈ 160MHz	GTK-TO	
1	HyperTransport (LDT_25)	IN	GTK-TO**_Full**	@ ≈ 160MHz	GTK-TO	
1	HyperTransport (LDT_25)	IN	GTK-TO**_EOC**	@ ≈ 160MHz	GTK-TO	(End Of Column Readout Enable) (?)
1	s.e. (LVCMOS?)	OUT	GTK-TO**_BackPressure**		GTK-TO	
2	HyperTransport (LDT_25)	OUT	GTK-TO**_OE**	@ ≈ 160MHz	GTK-TO	
1*9	diff LVDS	IN	GTK-CERN **_data**	@ ≥ 320MHz	GTK-CERN	lettura alla velocita' massima consentita dal registro di uscita dell'ASIC o dall' FPGA
1*9	diff LVDS	OUT	GTK-CERN **_ReadClk**	@ ≥ 320MHz	GTK-CERN	lettura alla velocita' massima consentita dal registro di uscita dell'ASIC o dall' FPGA
1*9	s.e. (LVCMOS?)	IN	GTK-CERN **_DataValid**		GTK-CERN	
1*9	s.e. (LVCMOS?)	OUT	GTK-CERN **_ReadoutDone**		GTK-CERN	

I just figured out a couple days ago that the HyperTransport (alias LDT_25) is probably compatible with the signal levels expected by the INFN-TO GTK ASICs which has a 1.2V supply also for the I/O cells.

Specifications for the "GTK proximity card"

- Q: Do we need a "rad-hard" FPGA?
- A: I assume not, until proven wrong, in which case:

  - **ALTERA** provides an indication that the configuration memory was upset by radiation → possible to detect the event and fix the upset by re-configuration → dead time).
  - **XILINX** does not seem to have a similar feature but makes rad-hard chips (Virtex-4Q at 14K€ according to G.Mazza)
  - **ACTEL** makes the RTAX-S/SL familyfeaturing SEU-hardened flip-flops implemented without any user intervention: it offers the benefits of user-implemented triple module redundancy (TMR) without the associated overhead. (I have no price information). An antifuse device such as the AX2000-1FG1152 costs about 570$

- Q: What FPGA should we use to accomodate the standard and the quantities of signals involved in handling the GTK-DEMO ASICs?
- A: I was not able to find one FPGA which could interface to the INFN-TO chip directly, due to the 1.2V supply chosen for the I/O cells.

For instance: the ALTERA STRATIX II / STRATIX II GX and XILINX VIRTEX-4 support HyperTransport (alias LDT_25) which is fine for the differential lines to/from the INFN-TO GTK but they don't support a s.e. standard LVCMOS @1.2V (only HSTL_12 which is a voltage referenced standard).
The ALTERA Cyclone III devices support LVCMOS @1.2V but do not support LDT_25.
Similarly the VIRTEX-4Q support LDT_25 but only the GTL-DCI standard (1.2V supply, voltage referenced at 0.8V)…

Specifications for the "GTK proximity card"

Question to the TORINO GTK Designer: IS IT POSSIBLE TO BRING THE I/O SUPPLY to 2.5V on the GTK demonstrator ???

If not we could:

- Use a Cyclone III, for instance, not supporting the Hypertransport standard but supporting the LVCMOS @1.2V. Cyclone III supports the LVDS standard and this could be possibly translated to match the 1.2V voltage compliance of the INFN-TO GTK as explained in details in the paper by Stefano Chiozzi, INFN-FE.

Or:

- use a Stratix II / Stratix II GX / Virtex-4 device supporting the Hypertransport-LDT_25 standard for high speed differential connections to the GTK demonstrator and use a bus switch such as, for instance, the (slow!) AnalogDevices ADG3308 to translate the 1.5V-LVCMOS down to 1.2 for non timing critical single ended connections to the GTK ASIC

ADG3308: Low Voltage, 1.15 V to 5.5 V, 8-Channel Bidirectional Logic Level Translator

The ADG3308/ADG3308-1/ADG3308-2 are bidirectional level translators containing eight bidirectional channels. They can be used in multivoltage digital system applications, such as a data transfer ...More

On This Page:
- Data Sheet
- Resources
- Features
- Diagrams
- Specifications
- Explore Other Products
- Pricing, Packaging & Availability

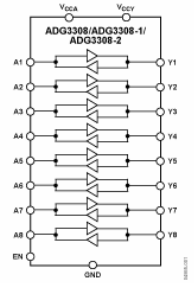
Quick Links
- Data Sheet Rev C, 09/2007, (pdf, 615 kB)
- (About Data Sheets)
- Lead(Pb) - Free Data

Resources
- Overview
- Rarely Asked Questions
- Solutions Bulletins

Features
- Bidirectional logic level translation
- Operates from 1.15 V to 5.5 V
- Low quiescent current < 1 µA
- No direction pin

Diagrams

Enlarge | Other Diagrams | Symbols and Footprints



Functional Block Diagram for ADG3308

Specifications

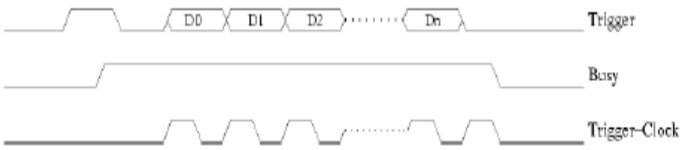
Data Rate (typ)	60Mbps	Pkg	CSP,TSSOP
t Prop Delay (typ)	5ns	Temp Range (°C)	-40 to 85
Bus Enable Time (typ)	1µs	Vcc 2 (V)	1.65V - 5.5V
VCC 1 (V)	1.15 - 5.5	Bus Width	8
ICC2 (Max)	1µA		

a proposal for the GTK demonstrators DAQ

The EUDET "TLU" (Trigger Logic Unit): a candidate (?) Trigger unit for the GTK demonstrator readout

13 Trigger Data Handshake

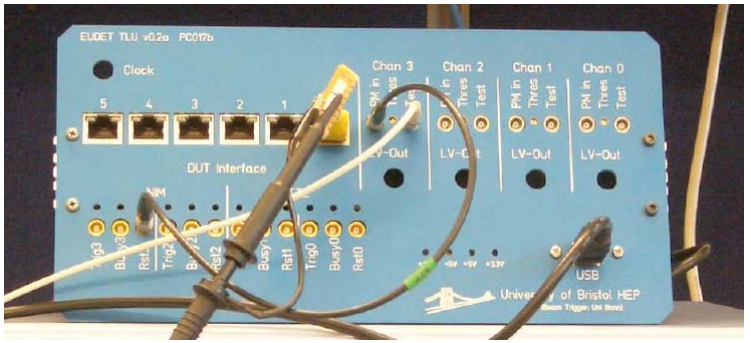
1) TLU receives trigger from beam scintillators
2) TLU asserts TRIGGER
3) On receipt of TRIGGER going high, the detector asserts BUSY
4) On receipt of BUSY going high, TLU de-asserts TRIGGER and switches the TRIGGER line to the output of a shift register holding the trigger number/data.
5) The DUT clocks data out of the shift register by toggling TRIGGER_CLOCK. Data changes on the rising edge of TRIGGER_CLOCK. The least significant bit of the trigger data is shifted out first.
6) After clocking out the trigger number (and the detector being ready to take more data, the DUT de-asserts BUSY)
7) System is ready for triggers again.

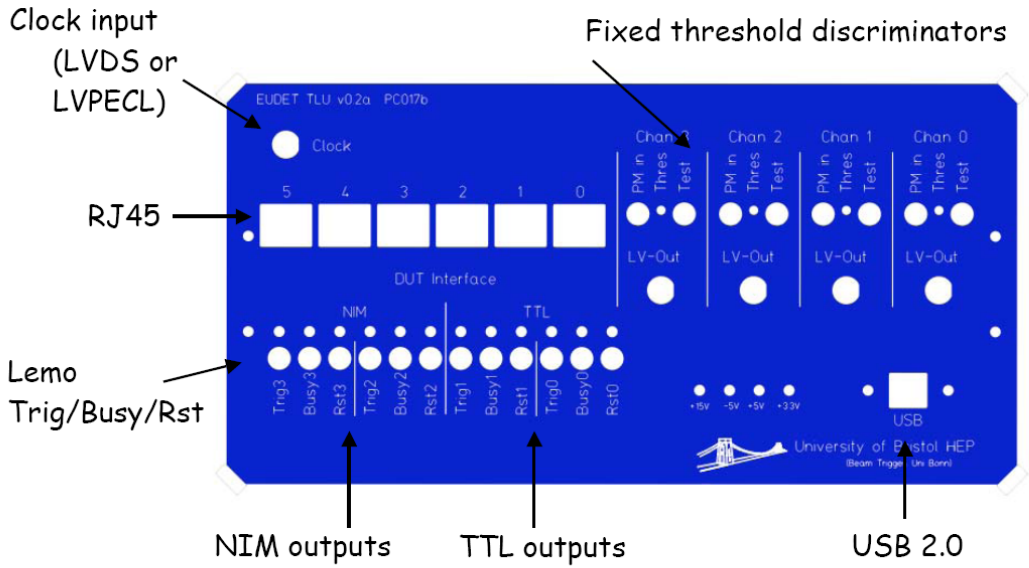


9 LVDS Interfaces

Six RJ45 connectors on front panel. LVDS levels. Pin out

1. Trigger+
2. Trigger-
3. Busy+
4. Reset+
5. Reset-
6. Busy-
7. Data-clock+
8. Data-clock-

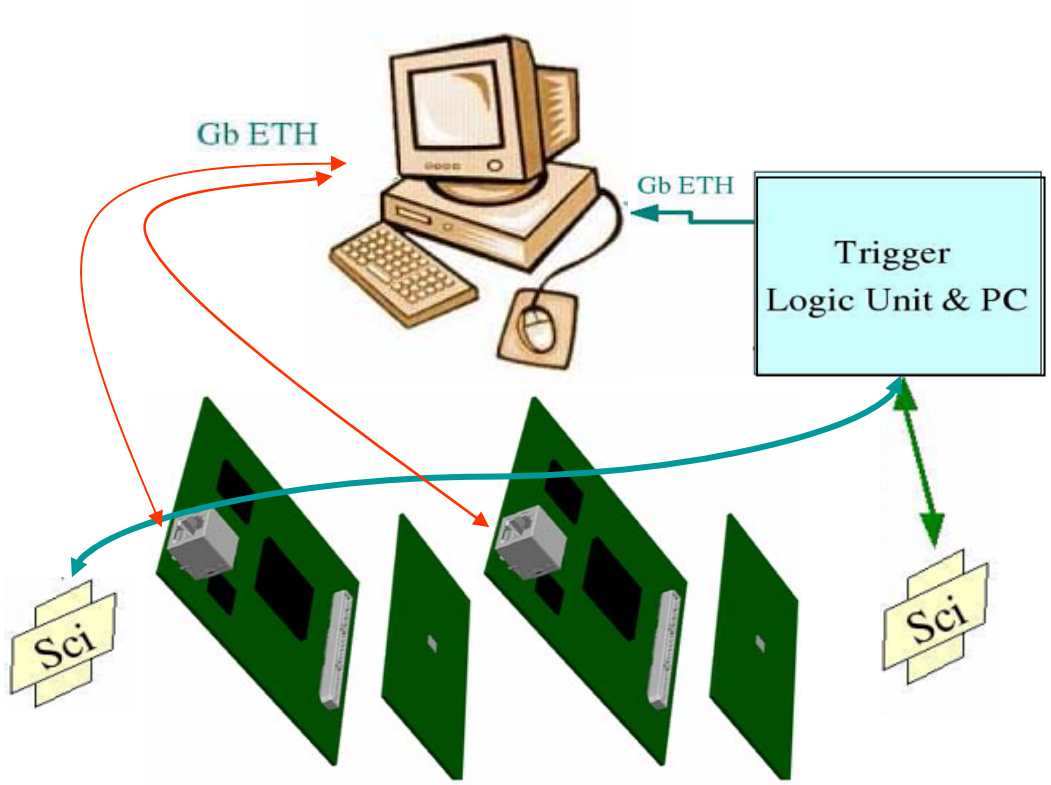




David Cussans, Geneva, May 2008

Source: http://indico.cern.ch/getFile.py/access?contribId=7&sessionId=1&resId=0&materialId=slides&confId=34050

a proposal for the GTK demonstrators DAQ



A simple DAQ system for a beam test could be based on:
• a clock distribution network (not shown)
• a TLU, generating triggers from PMTs and distributing triggers along with trigger numbers
• two (or more) "GTK proximity" cards connected to the TLU (to get the trigger number and set the BUSY signal) and connected to the DAQ PC: data is transferred via the GigabitEthernet. To improve ethernet throughput more events could be accumulated in a "Multievent" packet (as in the TELL1 board) to form a "jumbo" ethernet Frame. In that case the BUSY is not set on a event-by-event bases

ALTERA FPGA resources:

I/O standards, SER-DES units, memory and more

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Pricing (approximate)

Stratix III: minimum size currently available according to ALTERA web site: 150K logic elements

Manufacturer Part Number	Description	Category	Series		Minimum Quantity	Quantity Available	Unit Price USD
EP3SL150F780C3N	IC STRATIX III FPGA 150K 780FBGA	FP…	…III		1	17	2,840.00000
EP3SL150F780C2N	IC STRATIX III FPGA 150K 780FBGA	FP…	Stratix® III		4	Non-Stock	3,691.99250

Out of question

Stratix II: prices for chips with 30K logic elements

Manufacturer Part Number	Description	Category	Series		Minimum Quantity	Quantity Available	Unit Price USD
EP2S30F672C4	IC STRATIX II FPGA 30K 672-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II		1	6	616.00000
EP2S30F672C5	IC STRATIX II FPGA 30K 672-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II		1	7	495.00000
EP2S30F672C3	IC STRATIX II FPGA 30K 672-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II		1	8	792.00000

Stratix II GX: prices for chips with 30K logic elements

Manufacturer Part Number	Description	Category	Series		Minimum Quantity	Quantity Available	Unit Price USD
EP2SGX30CF780C3	IC STRATIX II GX 30K 780-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II GX		1	7	814.00000
EP2SGX30CF780C4	IC STRATIX II GX 30K 780-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II GX		8	Non-Stock	637.99875
EP2SGX30CF780C5	IC STRATIX II GX 30K 780-FBGA	FPGAs (Field Programmable Gate Array)	Stratix® II GX		1	8	517.00000

Cyclone III: prices for chips with 40K logic elements

Manufacturer Part Number	Description	Category	Series		Minimum Quantity	Quantity Available	Unit Price USD
EP3C40F780C6	IC CYCLONE III FPGA 40K 780FBGA	FPGAs (Field Programmable Gate Array)	Cyclone™ III		1	49	166.50000

Cyclone III: prices for chips with 80K logic elements

Manufacturer Part Number	Description	Category	Series		Minimum Quantity	Quantity Available	Unit Price USD
EP3C80F780C6	IC CYCLONE III FPGA 80K 780FBGA	FPGAs (Field Programmable Gate Array)	Cyclone™ III		1	34	368.50000

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Stratix II/Stratix II GX SUPPORTED I/O STANDARDS (with orange background Stratix II/GX specific)

SingleEnded	Differential	JEDEC support	IN Reference LEVEL [V]	IN: V_{CCIO} LEVEL [V]	OUT: V_{CCIO} LEVEL [V]	Board term. Voltage [V]
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS (PCI clamp must be enabled)		JESD8-B	-	3.3 3.0 2.5	3.0	-
2.5V-LVTTL / LVCMOS		JESD8-5	-	3.3; 3.0; 2.5	2.5	-
1.8V-LVTTL / LVCMOS		JESD8-7	-	1.8; 1.5	1.8	-
1.5V-LVCMOS		JESD8-11	-	1.8; 1.5	1.5	-
SSTL-2 classI/classII	SSTL-2 classI/classII **(**)**	JESD8-9A	1.25	2.5	2.5	1.25
SSTL-18 classI/classII	SSTL-18 classI/classII **(**)**	JESD8-15	0.9	1.8	1.8	0.9
HSTL-18 classI/classII	HSTL-18 classI/classII **(**)**	JESD8-6	0.9	1.8	1.8	0.9
HSTL-15 classI/classII	HSTL-15 classI/classII **(**)**	JESD8-6	0.75	1.5	1.5	0.75
HSTL-12 classI/classII **(****)**		JESD8-16a	0.6	1.2	1.2	0.6
PCI (3.3V) / PCI-X (3.3V mode 1)		-		3.0	3.0	-
	LVPECL **(*)**	-			3.3	
	LVDS		-		2.5 **(***)**	-
	HyperTransport technology				2.5	

(*): I/O standard available only for input and output column clocks pins for StratixII devices

(**): This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.

(***): VCCIO is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 9, 10, 11, and 12). The clock input pins supporting LVDS on banks 3, 4, 7, and 8 use **VCCINT=1.2V** for LVDS input operations and have no dependency on the VCCIO level of the bank. With a 1.2-V VCCINT level, input pins are 1.5-, 1.8-, 2.5-, and 3.3-V tolerant.

(****): 1.2-V HSTL is only supported in I/O banks 4,7, and 8.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

CYCLONE III SUPPORTED I/O STANDARDS (with yellow background Cyclone III specific)

SingleEnded	Differential	JEDEC support	IN Reference LEVEL[V]	IN: V_{CCIO} LEVEL [V]	OUT: V_{CCIO} LEVEL[V]	Board term. Voltage [V]
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS (PCI clamp must be enabled)		JESD8-B	-	3.3 3.0 2.5	3.0	-
2.5V-LVTTL / LVCMOS		JESD8-5	-	3.3; 3.0; 2.5	2.5	-
1.8V-LVTTL / LVCMOS		JESD8-7	-	1.8; 1.5	1.8	-
1.5V-LVCMOS		JESD8-11	-	1.8; 1.5	1.5	-
1.2V-LVCMOS		JESD8-12A	-	1.2	1.2	-
SSTL-2 classI/classII	SSTL-2 classI/classII **(*),(**)**	JESD8-9A	1.25	2.5	2.5	1.25
SSTL-18 classI/classII	SSTL-18 classI/classII **(*),(**)**	JESD8-15	0.9	1.8	1.8	0.9
HSTL-18 classI/classII	HSTL-18 classI/classII **(*),(**)**	JESD8-6	0.9	1.8	1.8	0.9
HSTL-15 classI/classII	HSTL-15 classI/classII **(*),(**)**	JESD8-6	0.75	1.5	1.5	0.75
HSTL-12 classI/classII	HSTL-12 classI/classII **(*),(**)**	JESD8-16a	0.6	1.2	1.2	0.6
PCI (3.3V)/PCI-X (3.3V mode 1) (PCI LocalBus Rev 2.2/1.0A)		-		3.0	3.0	-
	LVPECL **(***)**	-		2.5		
	LVDS			2.5	2.5	
	BLVDS (BusLVDS)			2.5	2.5	
	PPDS **(****)**				2.5	
	RSDS **(****)**				2.5	
	mini-LVDS **(****)**				2.5	

(*): Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them.

(**): Differential HSTL and SSTL are only supported on CLK, DQS inputs or PLL_OUT ouputs pins.

(***): I/O standard available only on CLK,DQS INPUTS for Cyclone III devices

(****):PPDS, mini-LVDS, RSDS only supported on output pins; registered trade marks of National Semiconductors

(*****): BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses LVDS input buffer.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

I/O STANDARDS		Applications	
SingleEnded	Differential	SingleEnded	Differential
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS		General Purpose (PCI clamp must be enabled)	General Purpose (PCI clamp must be enabled)
2.5V-1.8V-1.5V-1.2V LVTTL/LVCMOS		General Purpose	General Purpose
SSTL-2 classI/classII	SSTL-2 classI/classII	DDR SDRAM	DDR SDRAM
SSTL-18 classI/classII	SSTL-18 classI/classII	DDR SDRAM	DDR2 SDRAM
HSTL-18 classI/classII	HSTL-18 classI/classII	QDRII SRAM/RLDRAM II/SRAM	Clock Interfaces
HSTL-15 classI/classII	HSTL-15 classI/classII	QDRII SRAM/RLDRAM II/SRAM	Clock Interfaces
HSTL-12 classI/classII	HSTL-12 classI/classII	General Purpose **(*)**	Clock Interfaces **(*)**
PCI (3.3V) / PCI-X (3.3V mode 1)		PC /embedded systems @33/66MHz for PCI, @133MHz for PCI-X Spec Rev 1.0A	
	LVPECL **(**)**		Video graphics and clock distribution
	LVDS		**High-speed communications**
	HyperTransport technology		PCB interfaces
	BLVDS:Bus LVDS		bidirectional backplanes
	RSDS: **(***)**		reduced swing diff. signaling **(***)**
	mini-LVDS **(***)**		smaller voltage swing than LVDS **(****)**
	PPDS: **(***)**		point-to-point differential signaling

(*): single ended 1.2-V HSTL is only supported in I/O banks 4,7, and 8 in STRATIX II devices; Differential HSTL and SSTL are only supported on CLK, DQS inputs or PLL_OUT ouputs pins in **Cyclone III** devices

(**): available only for input and output column clocks pins for StratixII devices and only on CLK,DQS INPUTS for **Cyclone III** devices

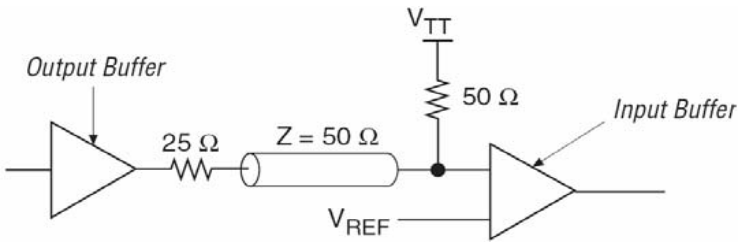
(***): PPDS, mini-LVDS, RSDS only supported on output pins; registered trade marks of National Semiconductors

(****): National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the display column drivers.

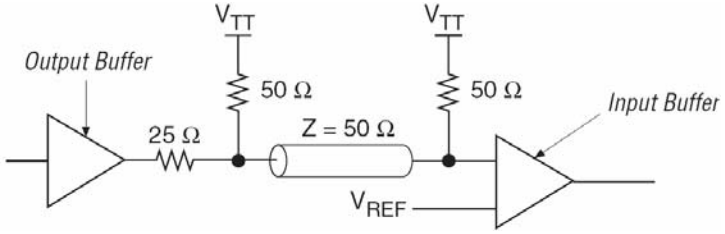
ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Termination schemes: S.E. SSTL/HSTL

Source: "Stratix II device handbook", vol.2 – section: "Stratix II and Stratix II GX I/O Standards Support"

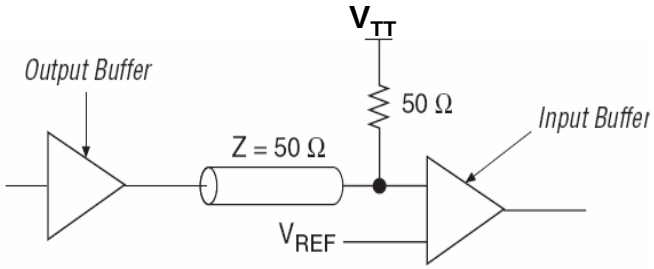


x.xV-SSTL Class I termination

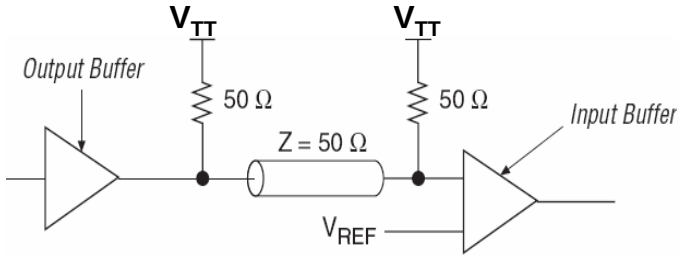


x.xV-SSTL Class II termination

V_{TT} = x.x / 2 [V]
V_{REF} = x.x / 2 [V]



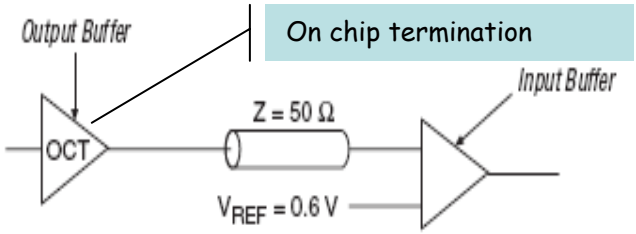
x.xV-HSTL Class I termination



x.xV-HSTL Class II termination

Single ended standards requiring reference (V_{REF}) and termination (V_{TT}) voltages

Figure 4–9. 1.2-V HSTL Termination

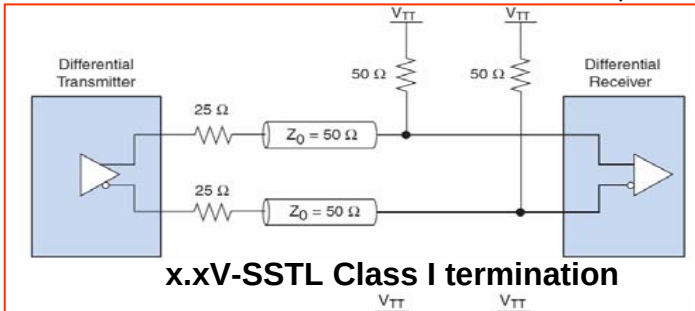


Although there is no EIA/JEDEC standard available for the 1.2-V HSTL standard, Altera supports it for applications that operate in the 0.0 to 1.2-V HSTL logic nominal switching range. 1.2-V HSTL can be terminated through series or parallel on-chip termination (OCT).

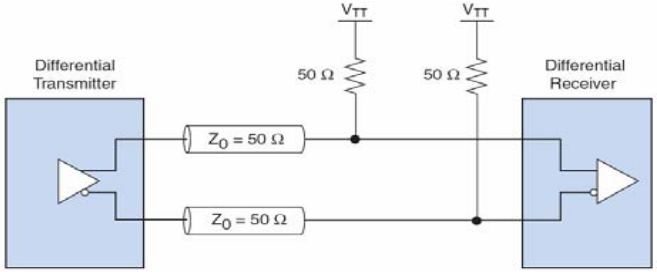
ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Termination schemes/voltage levels: diff. SSTL/HSTL, LVPECL, HyperTransport

Source: "Stratix II device handbook", vol.2 – section: "Stratix II and Stratix II GX I/O Standards Support"



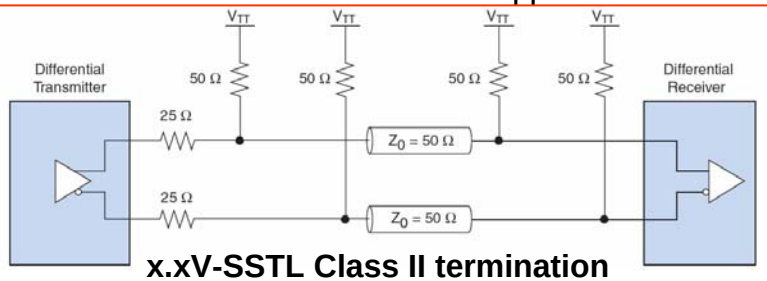
x.xV-SSTL Class I termination



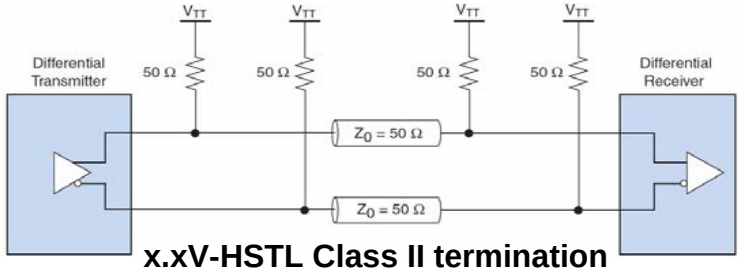
x.xV-HSTL Class I termination

Differential standards requiring termination (V_{TT}) voltages

V_{TT} = x.x / 2 [V]

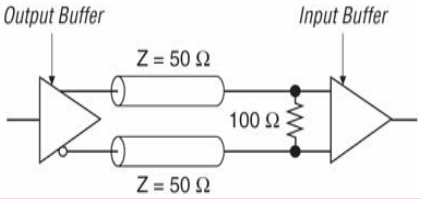


x.xV-SSTL Class II termination

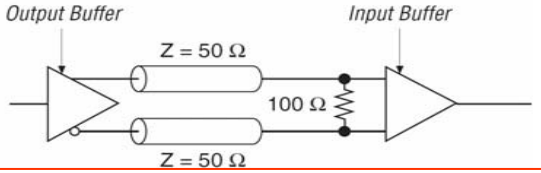


x.xV-HSTL Class II termination

LVPECL DC Coupled Termination



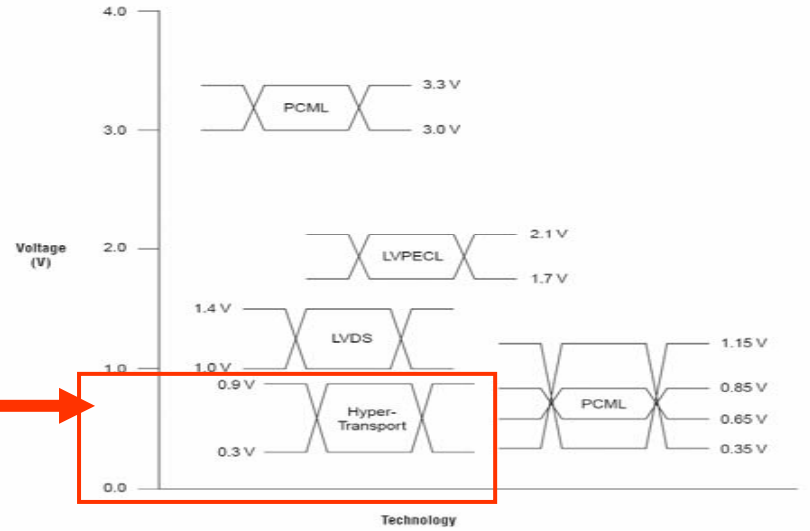
HyperTransport Termination



compatible with INFN-TO GTK ASIC's I/O levels

Altera Corporation — The Evolution of High-Speed Transceiver Technology

Figure 2. Differential I/O Technologies



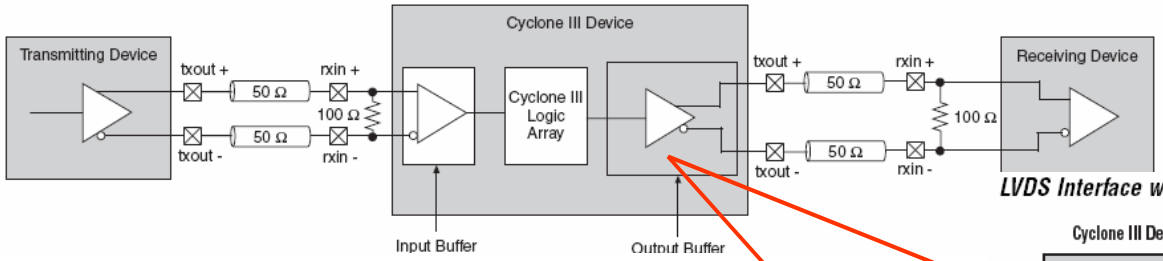
ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Termination schemes (most relevant): LVDS

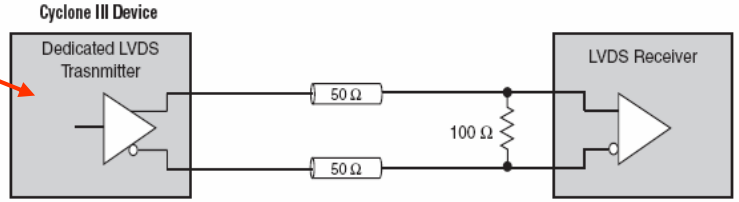
Source: "**Cyclone III** device handbook", vol.1 – section: "High-Speed I/O Standards Support"

compatible with CERN GTK ASIC's I/O levels

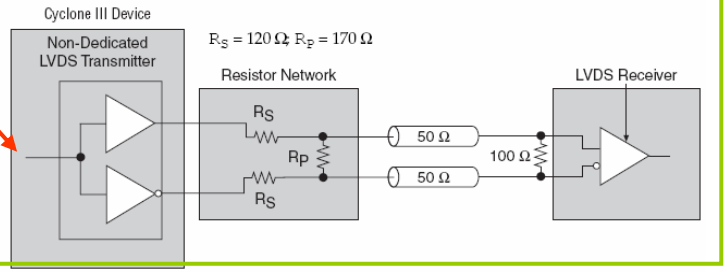
Typical LVDS Application



LVDS Interface with Dedicated Output Buffer on the Left and Right I/O Banks



LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks



NOTE on LVDS in Cyclone III devices:

You can use I/O pins and **internal logic** to implement the LVDS I/O receiver and transmitter in Cyclone III devices.

Cyclone III devices do not contain dedicated serialization or de-serialization circuitry.

Therefore, shift registers, internal PLLs, and IOEs are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

Source: "**Stratix II** device handbook", vol.1

Table 5–10. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.500	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

Table 5–11. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} (1)	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.300	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II devices)		90	100	110	Ω

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Stratix II** device handbook", pages 766

There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

		Max Toggle rate for a -3 STRATIX II device MAX clock toggle rate is different from MAX data bit rate. If MAX clock toggle rate on a regular I/O pin is 300 MHz, MAX data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.					
		COLUMN **[MHz]**		ROW **[MHz]**		DEDICATED CLOCK **[MHz]**	
SingleEnded	Differential	IN	OUT **(@ 0pF load)**	IN	OUT **(@ 0pF load)**	IN	OUT **(@ 0pF load)**
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS		500	1030	500	580	500	1100 (3.3V LVCMOS)
2.5V-1.8V-1.5V LVTTL/LVCMOS		500	**1131**(1.8V)	500	660(1.8V)	500	**1131**(1.8V)
SSTL-2 classI/classII	SSTL-2 classI/classII	500 | 500	400 | 400	500 | -	400(I) | 400(I)	500 | 500	400 | 400
SSTL-18 classI/classII	SSTL-18 classI/classII	500 | 500	700(I) | 700(I)	500 | -	500(I) | 350(I)	500 | 500	650(I) | 650(I)
HSTL-18 classI/classII	HSTL-18 classI/classII	500 | 500	700(I) | 700(I)	500 | -	700(I) | -	500 | 500	700(I) | 700(I)
HSTL-15 classI/classII	HSTL-15 classI/classII	500 | 500	700 | 700	500 | -	700(I) | -	500 | 500	700 | 700
HSTL-12 classI/classII		280	280 (OCT 50Ω)	-	-	280	280 (OCT 50Ω)
PCI (3.3V) / PCI-X (3.3V mode 1)		500	1000	-	-	500	1000
	LVPECL	-	-	-	-	450	450
	LVDS L/R banks	**-**	**-**	**520**	**500**	**717**	**450**
	LVDS T/B banks	**-**	**-**	**-**	**500**	**450**	**450**
	HyperTransport	-	-	520	500	717	-

Table 5–2. Differential Channels in Stratix II Devices (Part 1 of 2) Notes (1), (2), and (3)

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA Within the 1,508-pin Fin
EP2S15	38 transmitters 42 receivers		38 transmitters 42 receivers			
EP2S30	38 transmitters 42 receivers		58 transmitters 62 receivers			
EP2S60	38 transmitters 42 receivers		58 transmitters 62 receivers		84 transmitters 84 receivers	
EP2S90		38 transmitters 42 receivers		64 transmitters 68 receivers	90 transmitters 94 receivers	118 transmitters 118 receivers
EP2S130				64 transmitters 68 receivers	88 transmitters 92 receivers	156 transmitters 156 receivers

For a 30K gate EP2S30F672C3 device in a 672 pin FBGA package

CAVEATS:

- Stratix II devices offer a complete clock management solution with internal clock frequency of up to 550 MHz
- In Stratix II devices, the LVDS I/O standard requires a 2.5-V VCCIO level for the side I/O pins in banks 1, 2, 5, and 6. The top and bottom banks have different VCCIO requirements for the LVDS I/O standard. The LVDS clock I/O pins in banks 9 through 12 require a 3.3-V VCCIO level. Within these banks, the PLL[5,6,11,12]_OUT[1,2] pins support output only LVDS operations. The PLL[5,6,11,12]_FB/OUT2 pins support LVDS input or output operations but cannot be configured for bidirectional LVDS operations. The LVDS clock input pins in banks 4, 5, 7, and 8 use VCCINT and have no dependency on the VCCIO voltage level.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Stratix II GX** device handbook", pages 1484

There are two dedicated high-speed PLLs in the EP2SGX30 device and four dedicated high-speed PLLs in the EP2SGX60, EP2SGX90, and EP2SGX130 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Max Toggle rate for a -3 STRATIX II GX device

MAX clock toggle rate is different from MAX data bit rate. If MAX clock toggle rate on a regular I/O pin is 300 MHz, MAX data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

		COLUMN [MHz]		ROW [MHz]		DEDICATED CLOCK [MHz]	
SingleEnded	Differential	IN	OUT (@ 0pF load)	IN	OUT (@ 0pF load)	IN	OUT (@ 0pF load)
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS		500	1030	500	580	500	1100 (3.3V LVCMOS)
2.5V-1.8V-1.5V LVTTL/LVCMOS		500	**1131**(1.8V)	500	660(1.8V)	500	**1131**(1.8V)
SSTL-2 classI/classII	SSTL-2 classI/classII	500 | 500	400 | 400	500 | -	400(I) | 400(I)	500 | 500	400 | 400
SSTL-18 classI/classII	SSTL-18 classI/classII	500 | 500	700(I) | 700(I)	500 | -	500(I) | 350(I)	500 | 500	650(I) | 650(I)
HSTL-18 classI/classII	HSTL-18 classI/classII	500 | 500	700(I) | 700(I)	500 | -	700(I) | -	500 | 500	700(I) | 700(I)
HSTL-15 classI/classII	HSTL-15 classI/classII	500 | 500	700 | 700	500 | -	700(I) | -	500 | 500	700 | 700
HSTL-12 classI/classII		280 | 280	-	-	-	280	-
PCI (3.3V) / PCI-X (3.3V mode 1)		500	1000	-	-	500	-
	LVPECL	-	-	-	-	717H/450V	450
	LVDS L/R banks	**-**	**-**	**520**	**717**	**717**	**450**
	LVDS T/B banks	**-**	**-**	**-**	**717**	**450**	**450**
	HyperTransport	-	-	520	717	717H/450V	-

Table 11–3. Differential Channels in Stratix II GX Devices *Notes (1), (2), (3)*

Device	780-Pin FineLine BGA	1,152-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2SGX30	29 transmitters 31 receivers		
EP2SGX60	29 transmitters 31 receivers	42 transmitters 42 receivers	
EP2SGX90		45 transmitters 47 receivers	59 transmitters 59 receivers
EP2SGX130			71 transmitters 73 receivers

only!!!! For a 30K gate EP2S**GX**30F672C3 device in a **780** pin FBGA package

CAVEATS:

- The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix II devices, the LVDS I/O standard requires a 2.5-V VCCIO level for the side I/O pins in banks 1, 2, 5, and 6. The top and bottom banks have different VCCIO requirements for the LVDS I/O standard. The LVDS clock I/O pins in banks 9 through 12 require a 3.3-V VCCIO level. Within these banks, the PLL[5,6,11,12]_OUT[1,2] pins support output only LVDS operations. The PLL[5,6,11,12]_FB/OUT2 pins support LVDS input or output operations but cannot be configured for bidirectional LVDS operations. The LVDS clock input pins in banks 4, 5, 7, and 8 use VCCINT and have no dependency on the VCCIO voltage level.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Cyclone III** device handbook", pages 468

Max Toggle rate for a -6 Cyclone III device: MAX clock toggle rate is different from MAX data bit rate. If MAX toggle rate on a regular I/O pin is 300 MHz, MAX data bit rate for dual data rate (DDR) could be in principle as high as 600 Mbps on the same I/O pin.

SingleEnded	Differential	COLUMN [MHz] IN	COLUMN [MHz] OUT(@ 0pF load)	ROW [MHz] IN	ROW [MHz] OUT(@ 0pF load)	DEDICATED CLOCK [MHz] IN	DEDICATED CLOCK [MHz] OUT(@ 0pF load)
3.3V-LVTTL/LVCMOS 3.0V-LVTTL/LVCMOS		250	250	250	250	250	250
2.5V-1.8V-1.5V-1.2V LVTTL/LVCMOS		250 (200@1.2V)	250 (200@1.2V)	250 (200@1.2V)	250 (200@1.2V)	250 (200@1.2V)	250 (200@1.2V)
SSTL-2 classI/classII	SSTL-2 classI/classII	250 | -	250 | -	250 | -	250 | -	250 | 250	250 | 250
SSTL-18 classI/classII	SSTL-18 classI/classII	300 | -	300 | -	300 | -	300 | -	300 | 300	300 | 300(I)
HSTL-18 classI/classII	HSTL-18 classI/classII	300 | -	300 | -	300 | -	300 | -	300 | 300	300 | 300(I)
HSTL-15 classI/classII	HSTL-15 classI/classII	300 | -	300 | -	300 | -	300 | -	300 | 500	300 | 300(I)
HSTL-12 classI/classII	HSTL-12 classI/classII	125 | -	125	125(I) | -	-	125 | 125	125 | 125(I)
PCI (3.3V) / PCI-X (3.3V mode 1)		250	250	250	250	250	250
	LVPECL	-	-	-	-	438	-
	LVDS / LVDS_E_3R	**438**	**- / 320**	**438**	**420 / 320**	**438**	**- / 320**
	BLVDS:Bus LVDS	438	250	438	250		-
	RSDS / RSDSE_3R		-		180 / 180		- / 180
	mini-LVDS/mini-LVDS_E_3R		- / 155		200 / 200		- / 155
	PPDS / PPDS_E_3R		220		220 / 220		- / 220

Table 8–2. Cyclone III Device Differential Channels Notes (1), (1)

Device	Package	Pin Count	Number of Differential Channels: User I/O	Clock Pin	Total
EP3C40	EQFP	240	14	8	32
	FBGA	324	49	8	57
	FBGA	484	115	8	123
	FBGA	780	215	8	223
	UBGA	484	115	8	123
EP3C80	FBGA	484	101	8	109
	FBGA	780	169	8	177
	UBGA	484	101	8	109

223 total differential I/O channels for a EP3C40F780C6 device
177 total differential I/O channels for a EP3C80F780C6 device

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Stratix II** device handbook", vol.II, section:" High-Speed Differential I/O Interfaces with DPA in Stratix II and Stratix II GX Devices"

Stratix® II and Stratix® II GX device family offers up to 1-Gbps differential I/O capabilities to support **source-synchronous** communication protocols such as HyperTransport™ technology, RapidI/O, XSBI, and SPI.

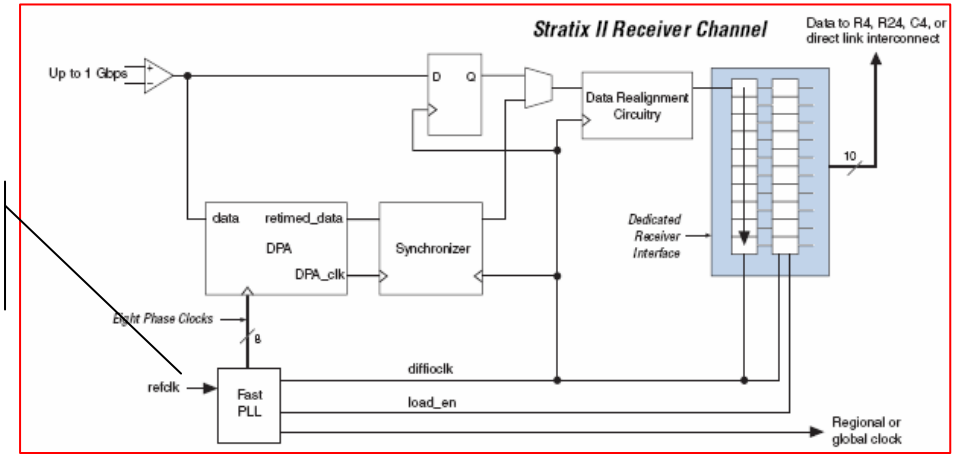
There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Stratix II and Stratix II GX devices can accommodate the high-speed differential I/O standards:

- LVDS
- HyperTransport technology
- HSTL (*)
- SSTL (*)
- LVPECL (*)

(*) for PLL clock differential inputs and outputs only.

The "slow" reference clock is transmitted along with data: **NO NEED FOR CLOCK RECOVERY FROM DATA**



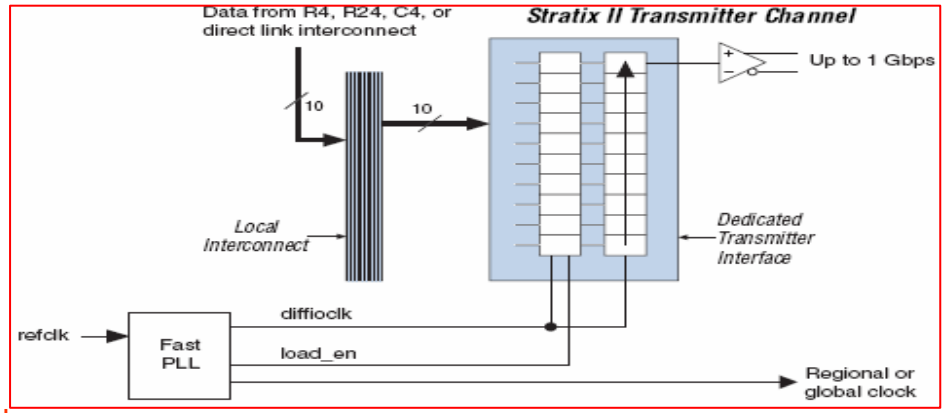
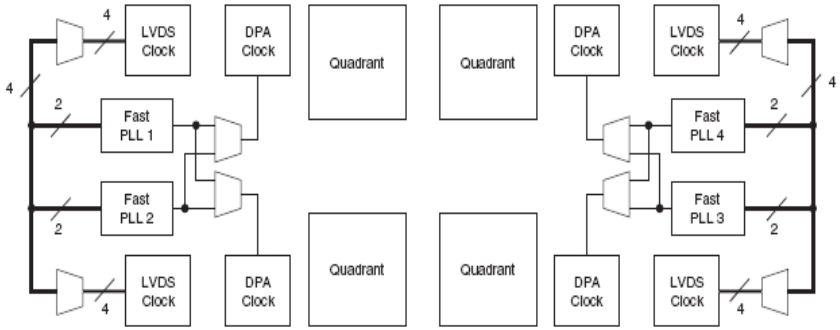


Figure 2–60. Fast PLL & Channel Layout in the EP2S15 & EP2S30 Devices *Note (1)*



Note to Figure 2–60:

(1) See Table 2–21 for the number of channels each device supports.

For a 30K gate EP2S30F672C3 device in a 672 pin FBGA package

Table 2–22. EP2S30 Device Differential Channels *Note (1)*

Package	Transmitter/ Receiver	Total Channels	Center Fast PLLs			
			PLL 1	PLL 2	PLL 3	PLL 4
672-pin FineLine BGA	Transmitter	58 *(2)*	16	13	13	16
		(3)	29	29	29	29
	Receiver	62 *(2)*	17	14	14	17
		(3)	31	31	31	31

Notes to Tables 2–21 to 2–26:

(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.
(2) This is the maximum number of channels the PLLs can directly drive.
(3) This is the maximum number of channels if the device uses cross bank channels from the adjacent center PLL.
(4) The channels accessible by the center fast PLL overlap with the channels accessible by the corner fast PLL. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Stratix II GX** device handbook"

Stratix® II and Stratix® II GX device family offers up to 1-Gbps differential I/O capabilities to support **source-synchronous** communication protocols such as HyperTransport™ technology, RapidI/O, XSBI, and SPI.

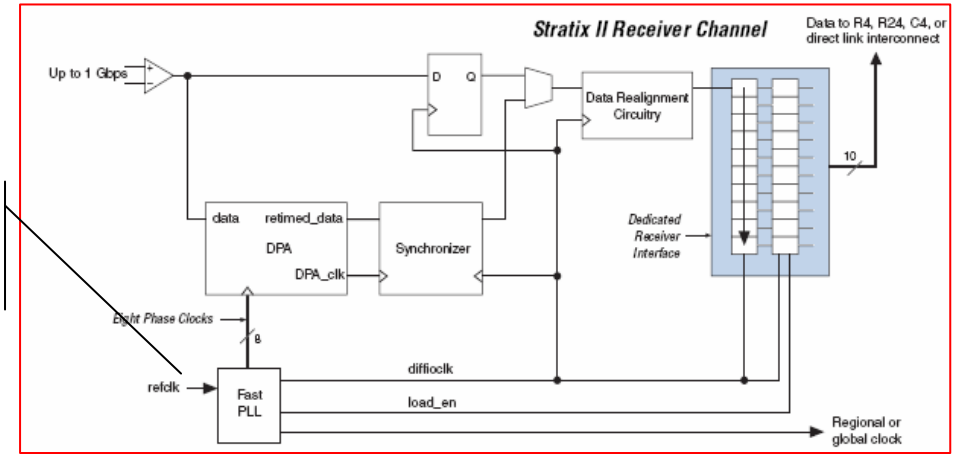
There are four dedicated high-speed PLLs in the EP2S15 to EP2S30 devices and eight dedicated high-speed PLLs in the EP2S60 to EP2S180 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Stratix II and Stratix II GX devices can accommodate the high-speed differential I/O standards:

- LVDS
- HyperTransport technology
- HSTL (*)
- SSTL (*)
- LVPECL (*)

(*) for PLL clock differential inputs and outputs only.

The "slow" reference clock is transmitted along with data: **NO NEED FOR CLOCK RECOVERY FROM DATA**



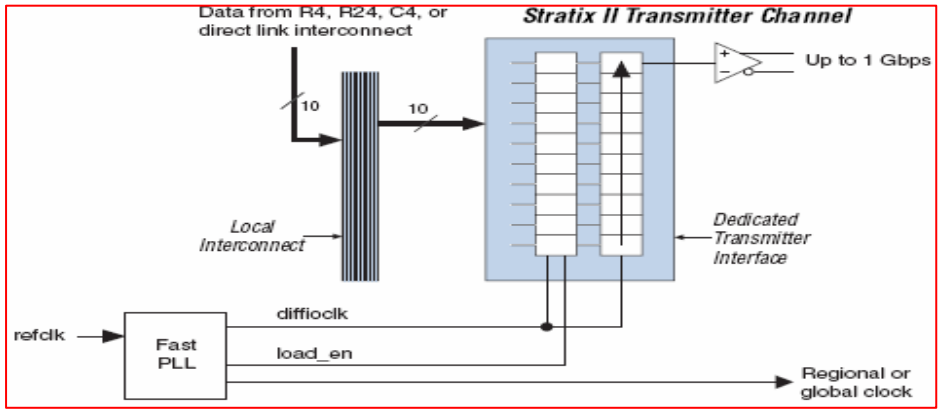
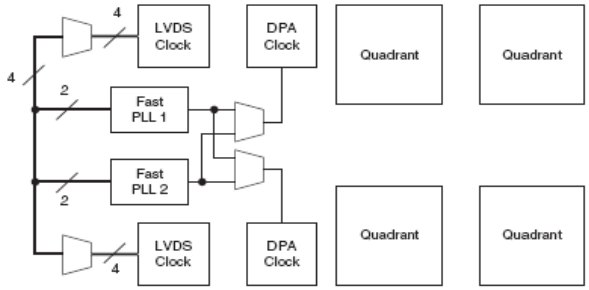


Figure 2–90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2–90:
(1) See Table 2–38 for the number of channels each device supports.

Table 2–38. EP2SGX30 Device Differential Channels *Note (1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs Package	
			PLL1	PLL2
780-pin FineLine BGA	Transmitter	29	16	13
	Receiver	31	17	14

Note to Tables 2–38 through 2–41:
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

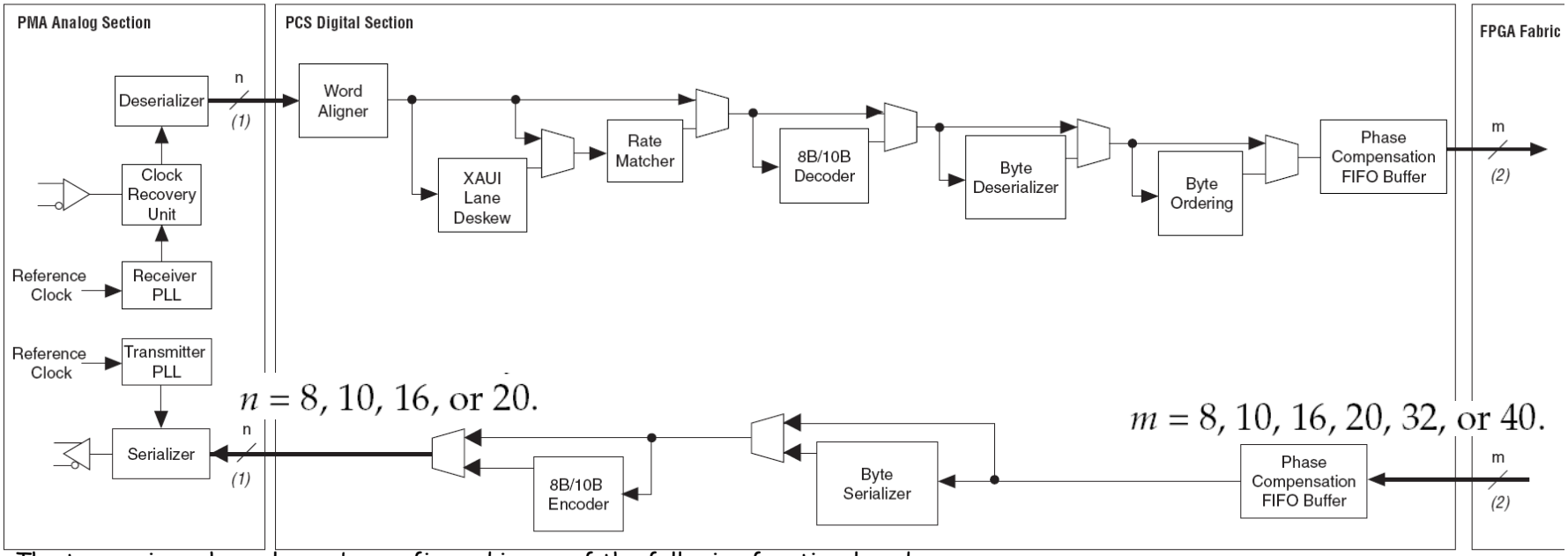
For a 30K gate EP2SGX30F672C3 device in a 780 pin FBGA package

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Source: "**Stratix II GX** device handbook"

Stratix® II GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 6.375-Gbps serial transceiver channels.
Each Stratix II GX transceiver block contains four full-duplex channels and supporting logic. The transceivers deliver bidirectional point-to-point data transmissions, with up to 51 Gbps (6.375 Gbps per channel) of full-duplex data transmission per transceiver block.

Figure 2–1. Stratix II GX Transceiver Block Diagram



The transceiver channels can be configured in one of the following functional modes:

- PCI Express (PIPE)
- OIF CEI PHY Interface
- SONET/SDH
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps single-width mode and 1 Gbps to 6.375 Gbps double-width mode)
- SDI (HD, 3G)
- CPRI (614 Mbps, 1228 Mbps, 2456 Mbps)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

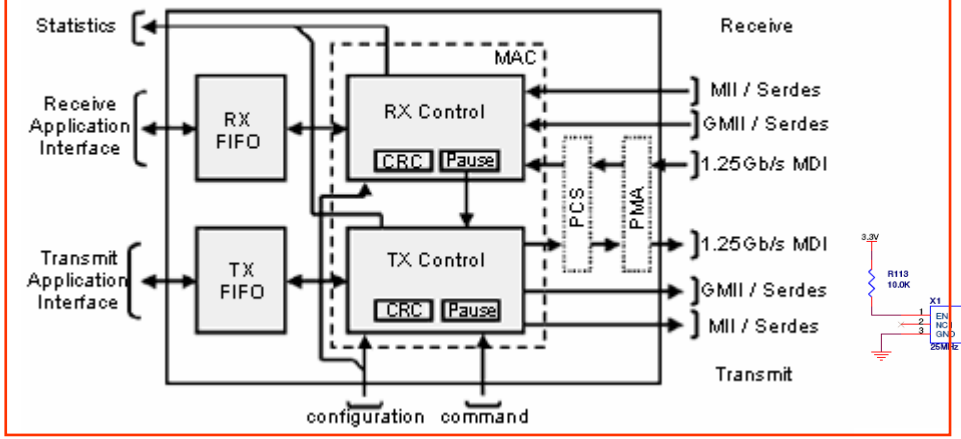
Ethernet MACs: internal (IP cores) vs external

Source: www.altera.com

10/100/1000 Mbps Ethernet MAC from *MorethanIP*

- IEEE 802.3 specification fully implemented
- Configuration dynamically supports 10-Mbps, 100-Mbps, or 1-Gbps operation.
- Interface connects seamlessly to commercial Gigabit Ethernet physical layer (PHY) device via a 8-bit gigabit medium independent interface (GMII) @ 125 MHz
- Interface connects seamlessly to commercial Fast Ethernet PHY device via a 4-bit medium independent interface (MII) operating at 25 MHz
- Integrated 1000Base-X physical coding sub-layer (PCS) and physical medium attachment (PMA) (optional) when implemented in Altera® Stratix™ GX devices with 8b/10b coding decoding and frame encapsulation
- Serial 1.25-Gbps medium dependent interface (MDI) (optional) implemented with Altera Stratix GX-embedded serializer/deserializer (SERDES)
- First-in first-out (FIFO) interface to user application

Figure 1. 10/100/1000 Mbps Ethernet MAC Block Diagram



The Marvell "Alaska" single-port 88E1111 transceiver leads the industry with the lowest power consumption (only 0.75W), as well as the smallest package footprint option - only 9 mm x 9 mm. The Alaska single-port 88E1111 product performs all of the physical layer (PHY) functions for half- and full-duplex 10BASE-T Ethernet on CAT 3, 4 and 5 cable, and half- and full-duplex 100BASE-TX and 1000BASE-T Ethernet on CAT 5 twisted pair cable. Additionally, the 88E1111 device offers additional support of 1000BASE-X through an integrated 1.25 GHz SERDES.

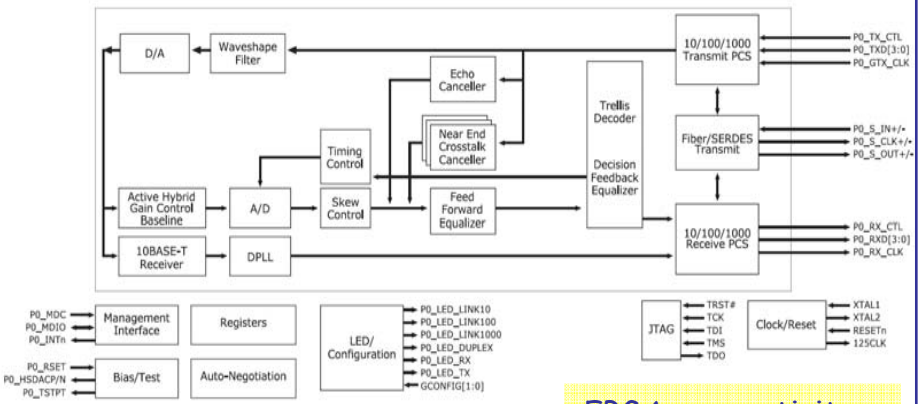
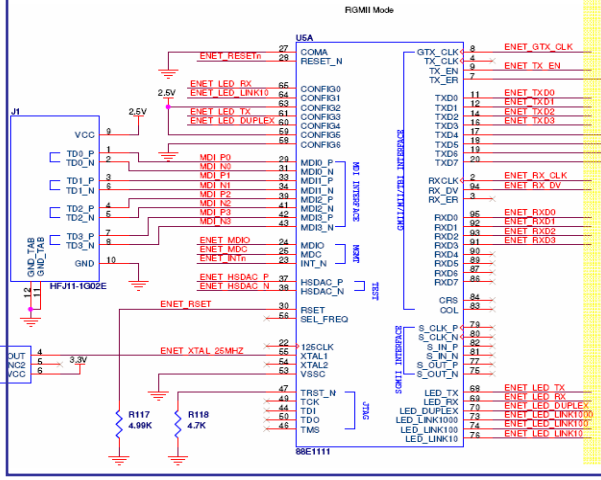


Fig 1. Alaska Single-Port GbE Transceiver (88E1111) Block Diagram



FPGA connectivity is provided via an industry standard GMII or RGMII interface.Configure Altera's Triple-Speed Ethernet MegaCore function onto Cyclone III for external PHY operation, providing an integrated solution.

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

internal memory blocks

Table 1–1 Stratix II FPGA Family Features

Feature	EP2S15	EP2S30
ALMs	6,240	13,552
Adaptive look-up tables (ALUTs) *(1)*	12,480	27,104
Equivalent LEs *(2)*	15,600	33,880
M512 RAM blocks	104	202
M4K RAM blocks	78	144
M-RAM blocks	0	1
Total RAM bits	419,328	1,369,728
DSP blocks	12	16
18-bit × 18-bit multipliers *(3)*	48	64
Enhanced PLLs	2	2
Fast PLLs	4	4
Maximum user I/O pins	366	500

Notes to Table 1–1:

(1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus® II software for logic synthesis.
(2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).
(3) These multipliers are implemented using the DSP blocks.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 500 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 550 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

Table 1–1 Stratix II GX Device Features

Feature	EP2SGX30C/D	
	C	D
ALMs	13,552	
Equivalent LEs	33,880	
Transceiver channels	4	8
Transceiver data rate	600 Mbps to 6.375 Gbps	
Source-synchronous receive channels *(1)*	31	
Source-synchronous transmit channels	29	
M512 RAM blocks (32 × 18 bits)	202	
M4K RAM blocks (128 × 36 bits)	144	
M-RAM blocks (4K × 144 bits)	1	
Total RAM bits	1,369,728	
Embedded multipliers (18 × 18)	64	
DSP blocks	16	
PLLs	4	
Maximum user I/O pins	361	
Package	780-pin FineLine BGA	

Note to Table 1–1:

(1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Table 1–1 Cyclone III FPGA Device Family Features

Feature	EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Logic Elements	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
Memory (Kbits)	414	414	504	594	1,134	2,340	2,745	3,888
Multipliers	23	23	56	66	126	156	244	288
PLLs	2	2	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20

Memory Blocks: each Cyclone III FPGA M9K memory block provides up to 9 kbits of on-chip memory capable of operation at up to **260 MHz**. The embedded memory structure consists of columns of M9K memory blocks (configurable as RAM, FIFO buffers, or ROM).

Table 4–2. Number of M9K Blocks in Cyclone III Devices

Device	Number of M9K Blocks	Total RAM Bits
EP3C5	46	423,936
EP3C10	46	423,936
EP3C16	56	516,096
EP3C25	66	608,256
EP3C40	126	1,161,216
EP3C55	260	2,396,160
EP3C80	305	2,810,880
EP3C120	432	3,981,312

Number of M9K blocks:

126

305

ALTERA FPGA resources: I/O standards, SER-DES units, memory and more

Radiation: hardness issues / fault detection (SEU mitigation)

From: "Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances" - iRoC Technologies, SA,World Trade Center, PO Box 1510 38025 Grenoble **France**, www.iroctech.com – pp.114

" 1 **Executive summary:**

• Cosmic-ray and alpha-particle soft error rates were measured for five different architectures of FPGAs, from three different vendors, using three different programming technologies.

• Test methodology was compliant with JESD-89.

• SRAM-based FPGAs are liable to configuration SEU and SEFI when exposed to high-energy neutrons and alpha particles.

• Antifuse-based and Flash-based FPGAs did not exhibit any configuration SEU or SEFI when exposed to high-energy neutrons and alpha particles.

• Test results allowed the calculation of the ratio of SEFIs to SEUs. "

ALTERA's SEU mitigation approach:

User Mode (i.e. after the FPGA configuration is over) **Error Detection**:

• **Soft errors** are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle.

• **Stratix II, Stratix II GX and Cyclone series devices have built-in error detection circuitry** to detect data corruption by soft errors in the CRAM cells. This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration.

• **The Cyclone III device error detection feature does not check memory blocks and I/O buffers**. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection **because these bits use flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.**

• You can implement the error detection CRC feature with existing circuitry in **Stratix II, Stratix II GX and Cyclone III** devices, eliminating the need for external logic. The CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. **The CRC_ERROR pin reports a soft error when configuration CRAM data is corrupted, and you must decide (by means of an independent configuration controller, for instance) whether to reconfigure the FPGA by strobing the nCONFIG pin low or ignore the error.**

XILINX FPGA resources:

I/O standards, SER-DES units, memory and more

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Pricing (approximate)

Summary of Virtex-4 Family Features

- Three Families — LX/SX/FX
  - Virtex-4 LX: High-performance logic applications solution
  - Virtex-4 SX: High-performance solution for digital signal processing (DSP) applications
  - Virtex-4 FX: High-performance, full-featured solution for embedded platform applications
- Xesium™ Clock Technology
  - Digital clock manager (DCM) blocks
  - Additional phase-matched clock dividers (PMCD)
  - Differential global clocks
- XtremeDSP™ Slice
  - 18 x 18, two's complement, signed Multiplier
  - Optional pipeline stages
  - Built-in Accumulator (48-bit) and Adder/Subtracter
- Smart RAM Memory Hierarchy
  - Distributed RAM
  - Dual-port 18-Kbit RAM blocks
    - Optional pipeline stages
    - Optional programmable FIFO logic automatically remaps RAM signals as FIFO signals
  - High-speed memory interface supports DDR and DDR-2 SDRAM, QDR-II, and RLDRAM-II.
- SelectIO™ Technology
  - 1.5V to 3.3V I/O operation
  - Built-in ChipSync™ source-synchronous technology
  - Digitally controlled impedance (DCI) active termination
  - Fine grained I/O banking (configuration in one bank)
- Flexible Logic Resources
- Secure Chip AES Bitstream Encryption
- 90-nm Copper CMOS Process
- 1.2V Core Voltage
- Flip-Chip Packaging including Pb-Free Package Choices
- RocketIO™ 622 Mb/s to 6.5 Gb/s Multi-Gigabit Transceiver (MGT) [*FX only*]
- IBM PowerPC RISC Processor Core [*FX only*]
  - PowerPC 405 (PPC405) Core
  - Auxiliary Processor Unit Interface (User Coprocessor)
- Multiple Tri-Mode Ethernet MACs [*FX only*]

Virtex-4 FX: **20K** logic cells

XC4VFX60-11FF672CS1 $ 1070,0000

XC4VFX60-10FF672CS1 $ 856,2500

Virtex-4 FX: **40K** logic cells

XC4VFX40-12FF672CS1 $ 866,2500

XC4VFX40-11FF672CS1 $ 618,7500

XC4VFX40-10FF672CS1 $ 495,0000

Virtex-4 FX: **20K** logic cells

XC4VFX20-12FF672CS1 $ 433,7500

XC4VFX20-11FF672CS1 $ 310,0000

XC4VFX20-10FF672CS1 $ 247,5000

Virtex-4 Q Pro-V: **radiation tolerant devices**

Price: 14Keuro (according to G. Mazza)
Availability: 3rd quarter 2008

Table 1: **Virtex-4 QPro-V FPGA Family Members**

Device	Configurable Logic Blocks (CLB)					Block RAM		DCMs	PMCDs	PowerPC Processor Blocks	Ethernet MACs	Total I/O Banks	Max User I/O
	Array Row x Col	Logic Cells	Slices	Max Distributed RAM (Kb)	XtremeDSP Slices	18-Kb Blocks	Max Block RAM (Kb)						
XQR4VSX55	128 x 48	55,296	24,576	384	512	320	5,760	8	4	–	–	13	640
XQR4VFX60	128 x 52	56,880	25,280	395	128	232	4,176	12	8	2	4	13	576
XQR4VFX140	192 x 84	142,128	63,168	987	192	552	9,936	20	8	2	4	17	896
XQR4VLX200	192 x 116	200,448	89,088	1392	96	336	6,048	12	8	–	–	17	960

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Virtex-4 QPro-V: radiation hardness issues

Radiation- Hardened Virtex-4 QPro-V FPGAs provide unprecedented integration with Advanced Silicon Modular Block (ASMBL™) architecture, including high-performance logic, PowerPC® embedded processors, XtremeDSP™ signal processing solution and tri-mode Ethernet MACs all in a single device. Radiation-Hardened Virtex-4 QPro-V FPGAs are a powerful alternative to ASIC and antifuse technologies.

Radiation-Hardened Virtex-4 QPro-V FPGAs are based on commercial Virtex-4 technology, providing enhancements to the popular Virtex and Virtex-II families — making previous-generation designs upwards compatible. Radiation-Hardened Virtex-4 QPro-V FPGAs offer over 350 MHz performance with TID of 250 krad.

From: "Radiation-Hardened Virtex-4 QPro-V Family Overview" - XILINX - pages 7 - March 31, 2008

Radiation-Hardness Assurance

The radiation-hardened Virtex™-4 QPro-V FPGAs are guaranteed for total ionizing dose (TID) life and single-event latch-up (SEL) immunity. Extensive single-event upset (SEU) characterization is performed and reported by the SEE Consortium.

Total Ionizing Dose

Each wafer lot is sampled and tested per Method 1019 to assure that device performance meets or exceeds the guaranteed DC electrical specification requirements, as well as AC and timing parameters at maximum guaranteed total dose levels.

Single-Event Latch-Up

The radiation-hardened Virtex-4 technology incorporates a thin epitaxial layer in the wafer manufacturing process for latch-up immunity assurance. The qualified mask set is verified in a heavy ion environment under vacuum, and tested at maximum V_{CC} and maximum operating temperature, to a fluence exceeding 1E7 particles/cm^2.

Single-Event Upset

Additional experiments are conducted in heavy ion, proton, and neutron environments in order to measure and document the susceptibility and consequence of SEU(s). An industry consortium oversees and validates the test methods, empirical data collected, and resulting analysis.

Conclusions are published on the website as well as international conferences. The Single-Event Effects Consortium Reports can be found at:

http://parts.jpl.nasa.gov/resources.htm

Table 2: **Radiation Tolerances(1)**

Symbol	Description	Min	Typical	Max	Units
TID	Total Ionizing dose Method 1019, dose rate ~50.0 rad(Si)/sec	250	–	–	krad(Si)
SEL	Single-event latch-up immunity Heavy ion linear energy transfer (LET)	100	–	–	LET (MeV-cm^2/mg)
SEFI	Single-event functional interrupt GEO 36,000 km typical day	–	1.5E–6	–	Upsets/device/day

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Virtex-4: supported I/O standards

Table 7: **SelectIO DC Input and Output Levels**

IOSTANDARD Attribute	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.2	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVCMOS33, LVDCI33	–0.2	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note(3)	Note(3)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(4)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.4	V_{CCO} – 0.45	Note(4)	Note(4)
PCI33_3[5]	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI66_3[5]	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
PCI-X[5]	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	N/A	36	N/A
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	N/A	32	N/A
HSTL I[2]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II[2]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III[2]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV[2]	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL II[2]	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	0.5	V_{CCO} – 0.5	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	–	–

Notes:
1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to the *Virtex-4 FPGA User Guide*, *SelectIO Resources*, *Chapter 6*.

GTL (Gunning Transceiver Logic)

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer. The negative terminal of the differential input buffer is referenced to the V_{REF} pin.

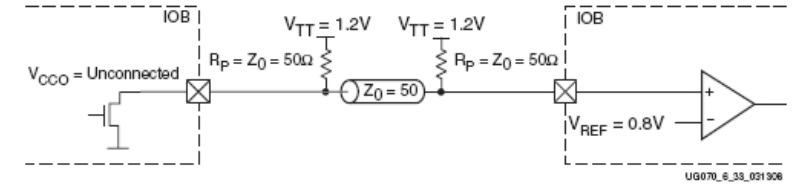


Figure 6-35: **GTL with External Parallel Termination and Unconnected V_{CCO}**

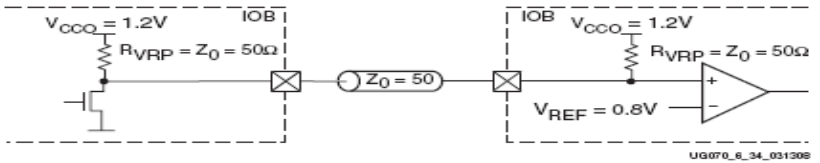


Figure 6-36: **GTL_DCI with Internal Parallel Driver and Receiver Termination**

Table 6-10: **GTL DC Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	–	N/A	-
$V_{REF} = N \times V_{TT}$ (1)	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	–
$V_{IL} = V_{REF} - 0.05$	–	0.75	0.81
V_{OH}	–	–	–
V_{OL}	–	0.2	0.4
I_{OH} at V_{OH} (mA)	–	–	–
I_{OL} at V_{OL} (mA) at 0.4V	32	–	–

Potentially compatible with INFN-TO GTK ASIC's diff. I/O levels (@1.2V supply)

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Virtex-4: supported I/O standards

LDT DC Specifications (LDT_25)

Table 8: LDT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage(1,2)	R_T = 100Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

Notes:
1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

HyperTransport Protocol (LDT)

The HyperTransport™ protocol or formally known as Lightning Data Transport (LDT) is a low-voltage standard for high-speed interfaces. Its differential signaling based interface is very similar to LVDS. Virtex-4 FPGA IOBs are equipped with LDT buffers. Table 6-35 summarizes all the possible LDT I/O standards and attributes supported.

Table 6-35: **Allowed Attributes of the LDT I/O Standard**

Attributes	Primitives	
	IBUFDS/IBUFGDS	OBUFDS/OBUFTDS
IOSTANDARD	LDT_25	
CAPACITANCE	LOW, NORMAL, DONT CARE	NORMAL
DIFF_TERM	TRUE, FALSE	Unused

Compatible with INFN-TO GTK ASIC's diff. I/O levels (@1.2V supply)

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals			1.602	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.898			V
V_{ODIFF}	Differential Output Voltage(1,2) (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

compatible with CERN GTK ASIC's diff. I/O levels

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Virtex-4: supported I/O standards

compatible with CERN GTK ASIC's diff. I/O levels

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	440	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage(1,2) (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-4 FPGA User Guide*: *Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1,2)	0.100		1.5	V

Notes:
1. Recommended input maximum voltage not to exceed V_{CCO} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

RocketIO DC Input and Output Levels

Table 12 summarizes the DC input and output specifications of the Virtex-4 FPGA RocketIO Multi-Gigabit Serial Transceivers. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage. Consult the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* for further details.

Table 12: **RocketIO DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-Peak Differential Input Voltage	DV_{IN}	Internal AC Coupled	110		2400	mV
Single-Ended Input Range	SE_{VIN}	Internal AC Coupled	0		V_{TRX}	mV
Common Mode Input Voltage Range	V_{ICM}	Internal AC Coupled	100		V_{TRX} – 100	mV
		Bypassed Internal AC Coupled (1)		800		mV
Single-Ended Output Voltage Swing(2, 3)	V_{OUT}		450		725	mV
Common Mode Output Voltage Range(3)	V_{TCM}			1000		mV
Peak-to-Peak Differential Output Voltage(2, 3)	DV_{PPOUT}		900	1050	1400	mV
Signal detect threshold	$RXOOB_{VDPP}$	RX		TBD		
Electrical idle amplitude	$TXOOB_{VDPP}$	TX		65		mV
RocketIO MGT Clock DC Input Levels						
Peak-to-Peak Differential Input Voltage	V_{IDIFF}	2 x I $V_{MGTCLKP}$ – $V_{MGTCKLN}$ I	100	600	2000	mV
Differential Input Resistance	R_{IN}		71	105	124	Ω

Notes:
1. The maximum V_{TRX} is 1.26V when bypassing the internal AC coupled V_{ICM}. V_{TRX} must be less than or equal to AVCCAUXRX.
2. The output swing and pre-emphasis levels are selected using the attributes discussed in Chapter 4: PMA Analog Considerations in the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* for details.
3. V_{TTX} is 1.5 ± 5%; different amplitudes possible with adjusted DAC values.

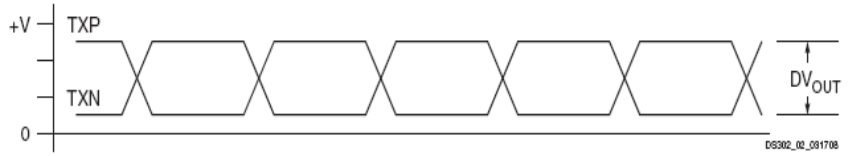


Figure 1: **Single-Ended Output Voltage Swing**

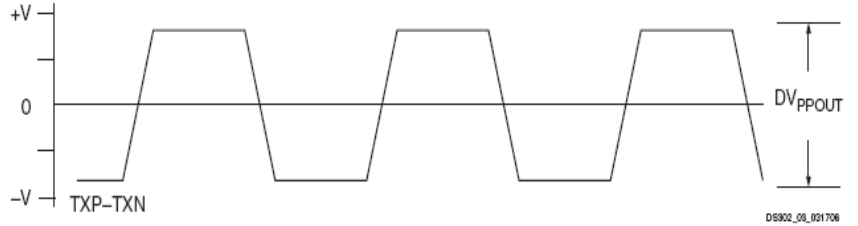


Figure 2: **Peak-to-Peak Differential Output Voltage**

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

Virtex-4: switching performances

I have not found, in the Virtex-4 datasheet, a quote on the maximum toggle frequency at the I/O pins for each standard, as in the ALTERA data sheets.
The only maximum toggle rate quoted were:

Clock Buffers and Networks

Symbol	Description	Speed Grade			Units
		-12	-11	-10	
Maximum Frequency					
F_{MAX}	Global clock tree	500	450	400	MHz

Block RAM and FIFO Switching Characteristics

Maximum Frequency					
F_{MAX}	Write first and no change mode	500.00	450.45	400.00	MHz
F_{MAX}	Read first mode	500.00	450.45	400.00	MHz
CLK-to-CLK	Read first mode	500.00	450.45	400.00	MHz
Maximum Frequency					
F_{MAX}	FIFO in all modes	500.00	450.45	400.00	MHz

Switching characteristics of I/O block pads are given in terms of propagation delays only:

Table 27: IOB Switching Characteristics[1,2]

IOSTANDARD Attribute[1]	T_{IOPI} Speed Grade			T_{IOOP} Speed Grade			T_{IOTP} Speed Grade			Units
	-12	-11	-10	-12	-11	-10	-12	-11	-10	
LVDS_25	1.00	1.15	1.28	1.61	1.71	1.85	1.61	1.71	1.85	ns
RSDS_25	1.00	1.15	1.28	1.61	1.71	1.85	1.61	1.71	1.85	ns
LVDSEXT_25	1.01	1.16	1.30	1.65	1.75	1.91	1.65	1.75	1.91	ns
LDT_25	1.00	1.15	1.28	1.58	1.68	1.82	1.58	1.68	1.82	ns
BLVDS_25	1.00	1.15	1.28	1.99	2.15	2.34	1.99	2.15	2.34	ns
ULVDS_25	1.00	1.15	1.28	1.59	1.68	1.83	1.59	1.68	1.83	ns
LVCMOS25, Fast, 16 mA	0.69	0.80	0.88	1.89	2.03	2.21	1.89	2.03	2.21	ns
LVCMOS25, Fast, 24 mA	0.69	0.80	0.88	1.83	1.96	2.13	1.83	1.96	2.13	ns

TIOPI is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
TIOOP is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
TIOTP is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

XILINX FPGA resources: I/O standards, SER-DES units, memory and more

1.3) Product Table

	XC 4VFX12	XC 4VFX20	XC 4VFX40	XC 4VFX60	XC 4VFX100	XC 4VFX140
Logic Cells	12,312	19,224	41,904	56,880	94,896	142,128
Block RAM/FIFO w/ECC (18 kbits each)	36	68	144	232	376	552
Total Block RAM (kbits)	648	1224	2,592	4,176	6,768	9,936
Digital Clock Managers (DCM)	4	4	8	12	12	20
Phase-matched Clock Dividers (PMCD)	0	0	4	8	8	8
Max Differential I/O Pairs	160	160	224	288	384	448
XtremeDSP™ Slices	32	32	48	128	160	192
PowerPC Processor Blocks	1	1	2	2	2	2
10/100/1000 Ethernet MAC Blocks	2	2	4	4	4	4
RocketIO Serial Transceivers	0	8	12	16	20	24
Configuration Memory Bits	5,017,088	7,641,088	15,838,464	22,262,016	35,122,240	50,900,352
Max SelectIO	320	320	448	576	768	896

Package	RocketIO	User I/O	User I/O	User I/O	User I/O	User I/O	User I/O
SF363	--	240	-	-	-	-	-
FF668	--	320	-	-	-	-	-
FF1148	--	-	-	-	-	-	-
FF1513	--	-	-	-	-	-	-
FF672	12	-	320 (8)**	352 (12)**	352 (12)**	-	-
FF1152	20	-	-	448 (12)**	576 (16)**	576 (20)**	-
FF1517	24	-	-	-	-	768 (20)**	768 (24)**
FF1760	24	-	-	-	-	-	896 (24)**

**Number of available RocketIO Multi-Gigabit Transceivers.

Table (1): Virtex-4 Products

Ethernet MAC Overview

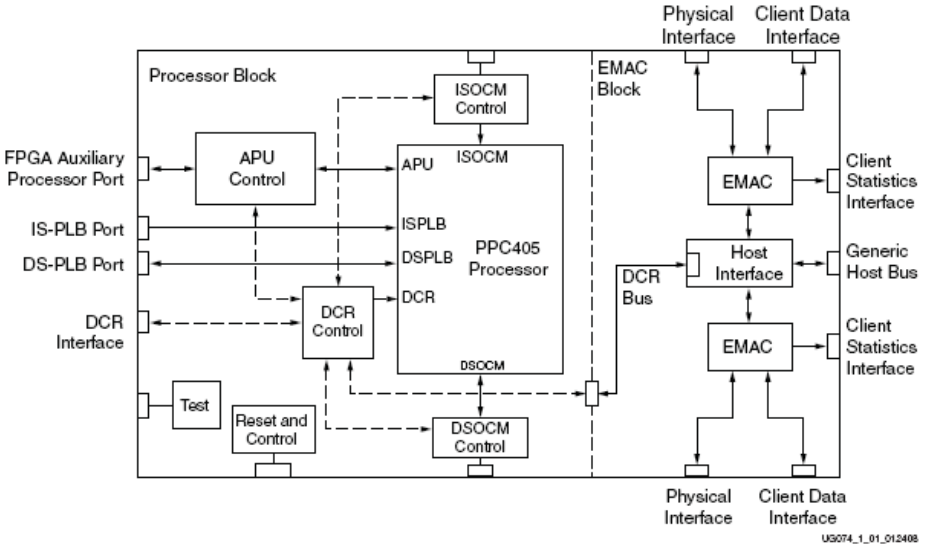


Figure 1-1: **Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC**

ACTEL FPGA resources:

I/O standards, SER-DES units, memory and more

ACTEL FPGA resources (brief)

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- Up to 684 I/Os
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  - 1.5V, 1.8V, 2.5V, 3.3V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS, 3.3V PCI, and 3.3V PCI-X
  - Differential I/O Standards: LVPECL and LVDS
  - Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
  - Registered I/Os
  - Hot-Swap Compliant I/Os (except PCI)
  - Programmable Slew Rate and Drive Strength on Outputs
  - Programmable Delay and Weak Pull-Up/Pull-Down Circuits on Inputs
- Embedded Memory:
  - Variable-Aspect 4,608-bit RAM Blocks (x1, x2, x4, x9, x18, x36 Organizations Available)
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
- Segmentable Clock Resources
- Embedded Phase-Locked Loop:
  - 14-200 MHz Input Range
  - Frequency Synthesis Capabilities up to 1 GHz
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability with Actel Silicon Explorer II
- Boundary-Scan Testing Compliant with IEEE Standard 1149.1 (JTAG)
- FuseLock™ Secure Programming Technology Prevents Reverse Engineering and Design Theft

Table 1-1 • **Axcelerator Family Product Profile**

Device	AX125	AX250	AX500	AX1000	AX2000
Capacity (in Equivalent System Gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Modules					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Embedded RAM/FIFO					
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (Segmentable)					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
PLLs	8	8	8	8	8
I/Os					
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Package					
CSP	180				
PQFP		208	208		
BGA				729	
FBGA	256, 324	256, 484	484, 676	484, 676, 896	896, 1152
CQFP		208, 352	208, 352	352	352
CCGA				624	624

Name	Function	Devices	Try It Now	Resources
Core10/100 10/100 Mbps Ethernet MAC with Host Controller DirectCore	Communications Ethernet	Fusion IGLOO ProASIC3L ProASIC3 ProASIC PLUS Axcelerator SX-A RT ProASIC3 RTAX-S/SL/DSP RTSX-SU		• Register your Design • Conformance Test Report • Brochure • Development Kit • Handbook • DirectCore IP Cores • IP Application Notes

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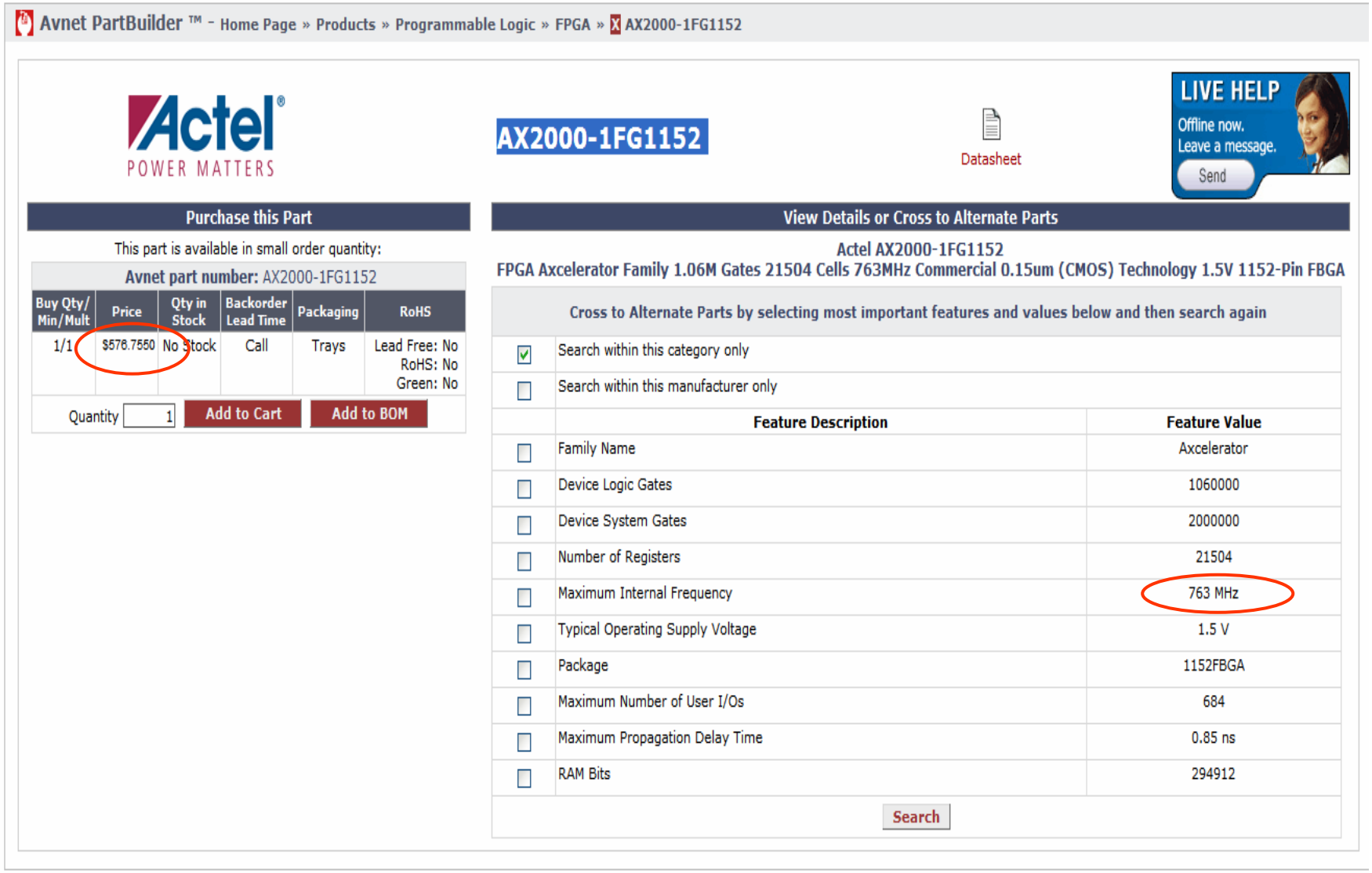
ACTEL FPGA resources (brief)



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Actel AX2000-1FG1152
FPGA Axcelerator Family 1.06M Gates 21504 Cells 763MHz Commercial 0.15um (CMOS) Technology 1.5V 1152-Pin FBGA

Cross to Alternate Parts by selecting most important features and values below and then search again

- [x] Search within this category only
- [ ] Search within this manufacturer only

	Feature Description	Feature Value
[ ]	Family Name	Axcelerator
[ ]	Device Logic Gates	1060000
[ ]	Device System Gates	2000000
[ ]	Number of Registers	21504
[ ]	Maximum Internal Frequency	763 MHz
[ ]	Typical Operating Supply Voltage	1.5 V
[ ]	Package	1152FBGA
[ ]	Maximum Number of User I/Os	684
[ ]	Maximum Propagation Delay Time	0.85 ns
[ ]	RAM Bits	294912

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