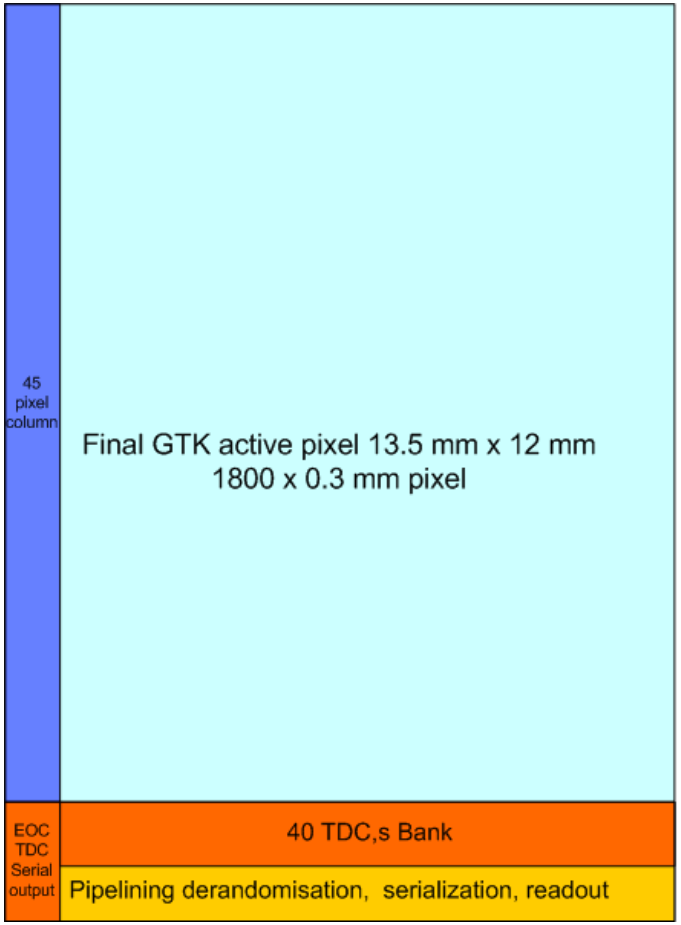
Agenda

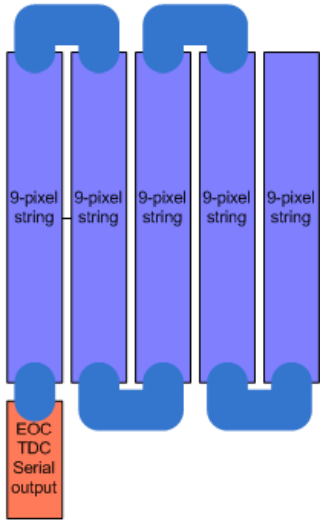
1. Demonstrator scheme
2. Demonstrator specification
3. Design Status
4. Spectre simulation issues
5. schedule

Column Demonstrator circuit

5-Folded 45-pixel column

Representing one long final column

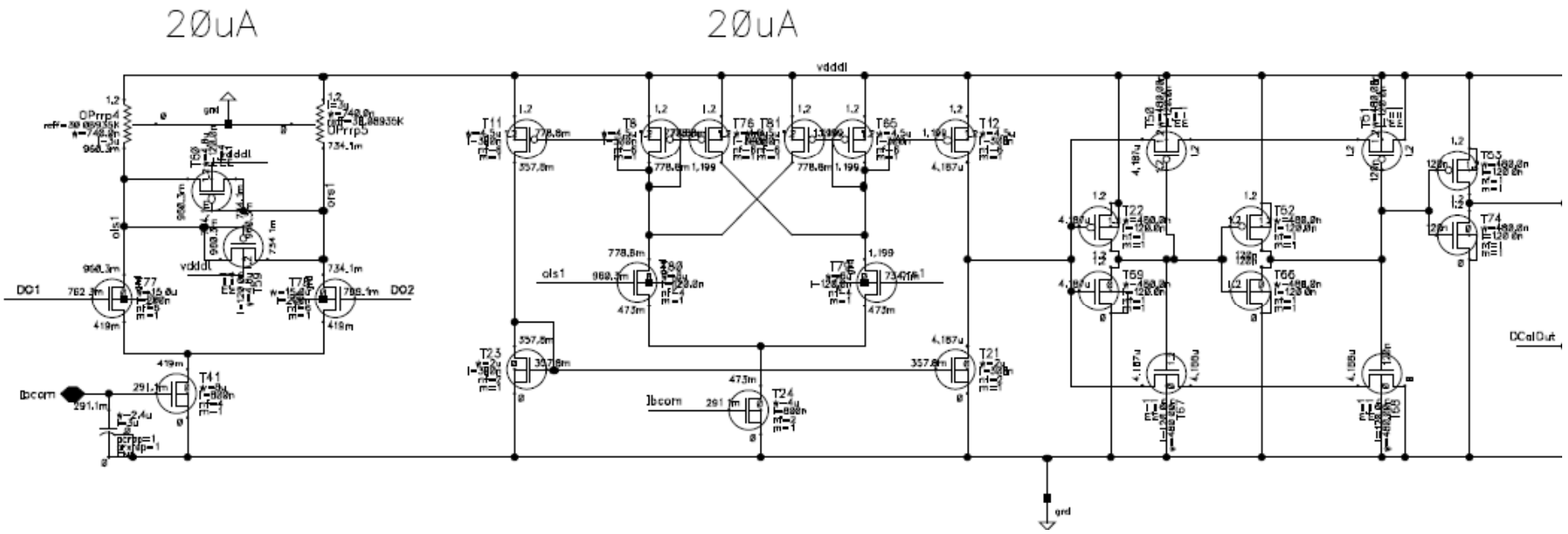




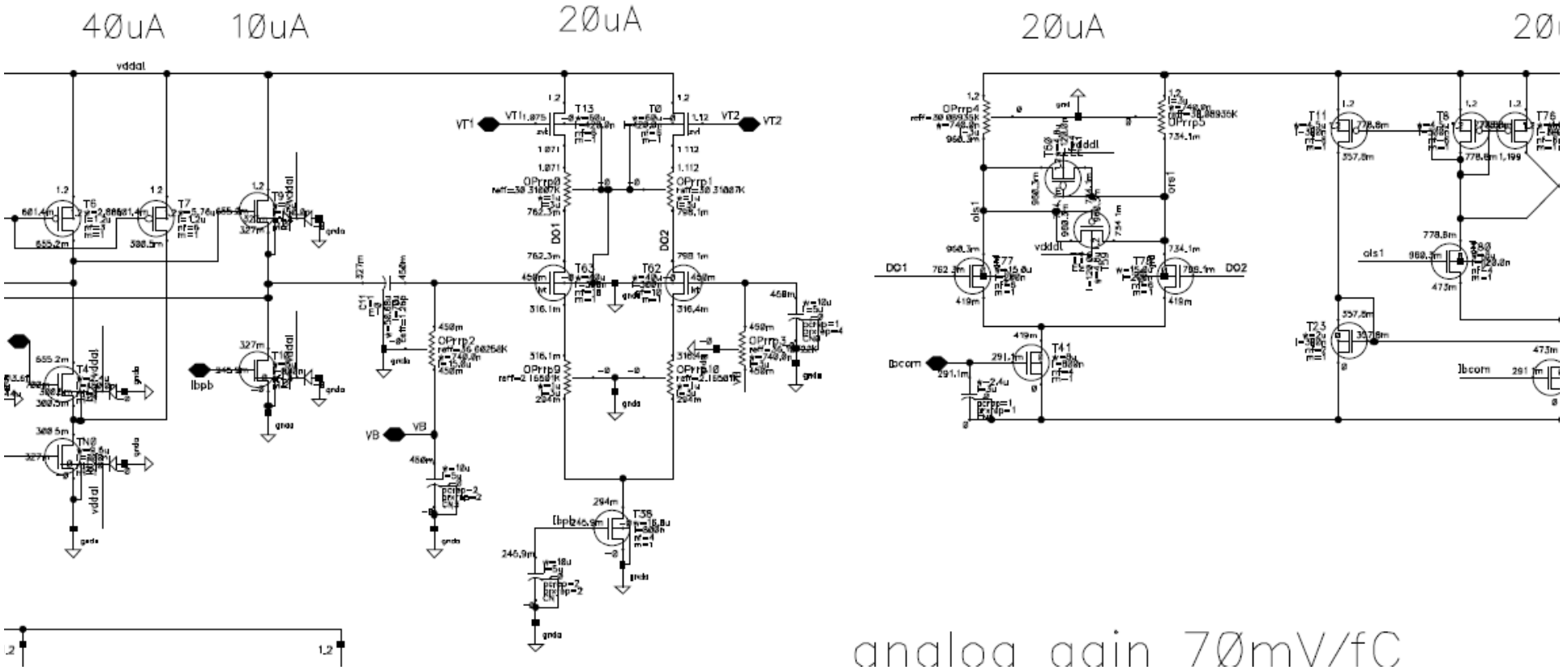
Simulation problems

- 9-pixel column works fine in DM
  - Down from preamp to the bus signal is as expected
  - Coplanar WG well balanced, signal transition <100 ps
- 45-pixel column does not work well
  - Distorted preamp signal
  - Painful simulations
    - Long hours
    - Cadence crashes or get stuck …
- Elena started from scratch,
  - So far it is good

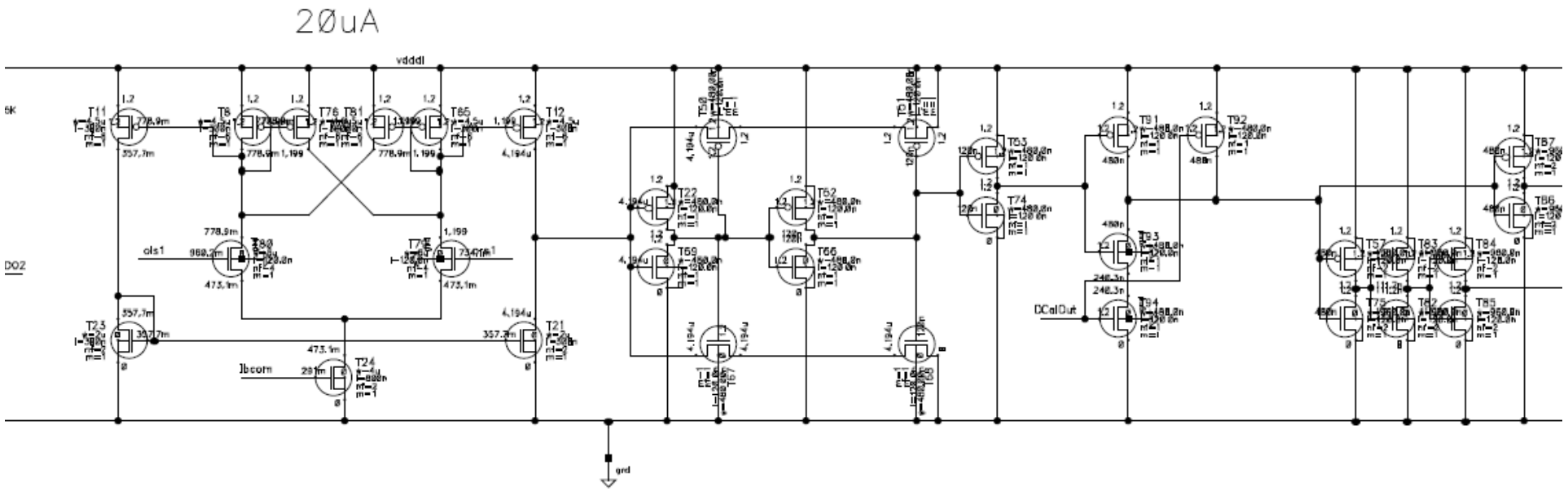
9-pixel top simulation



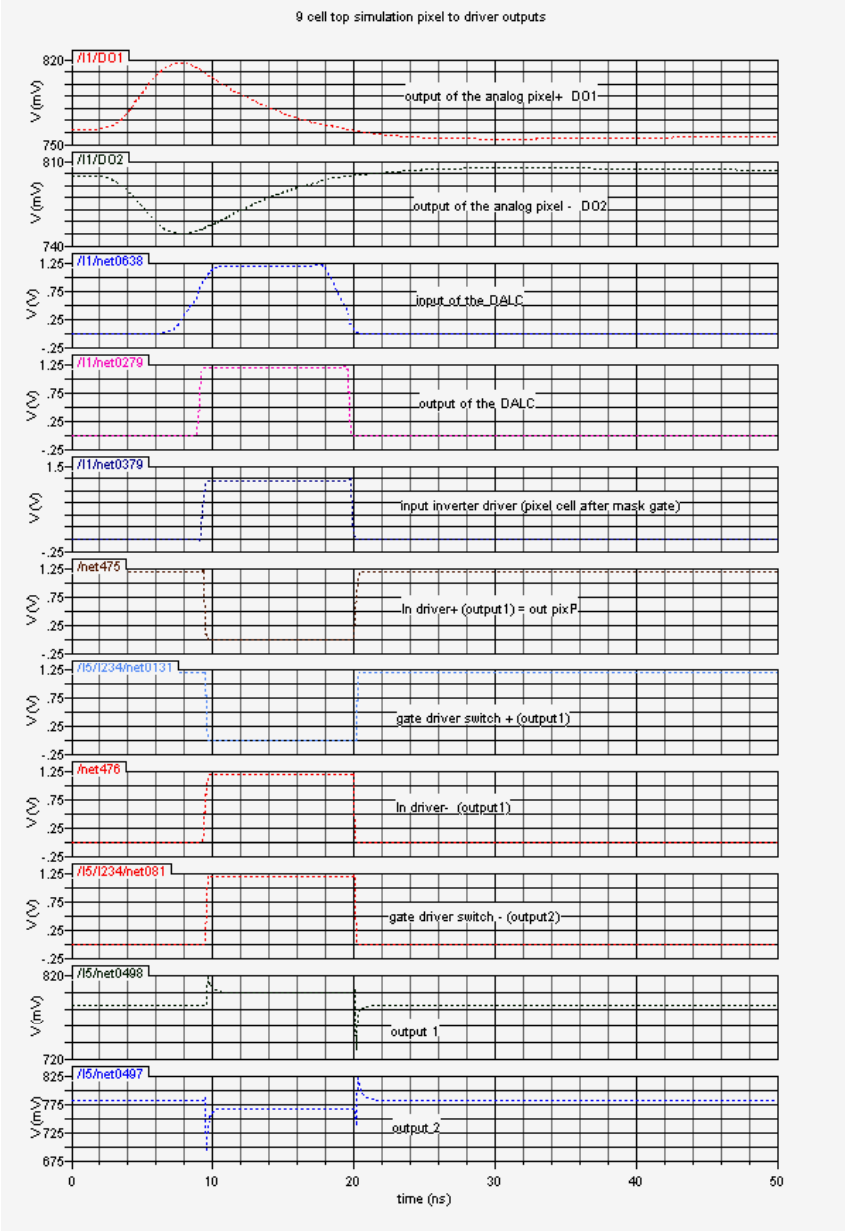
9-pixel top simu preamp



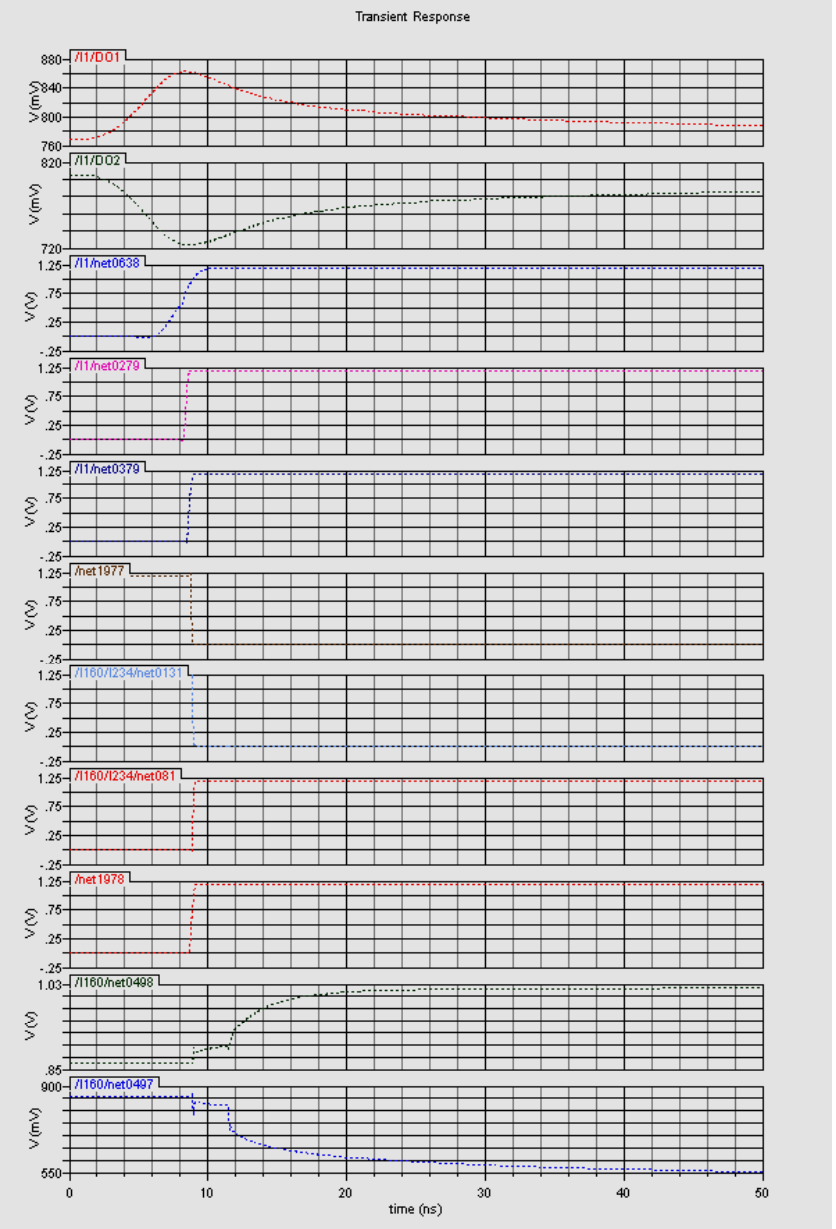
45 pixel column pixel 1 nodes



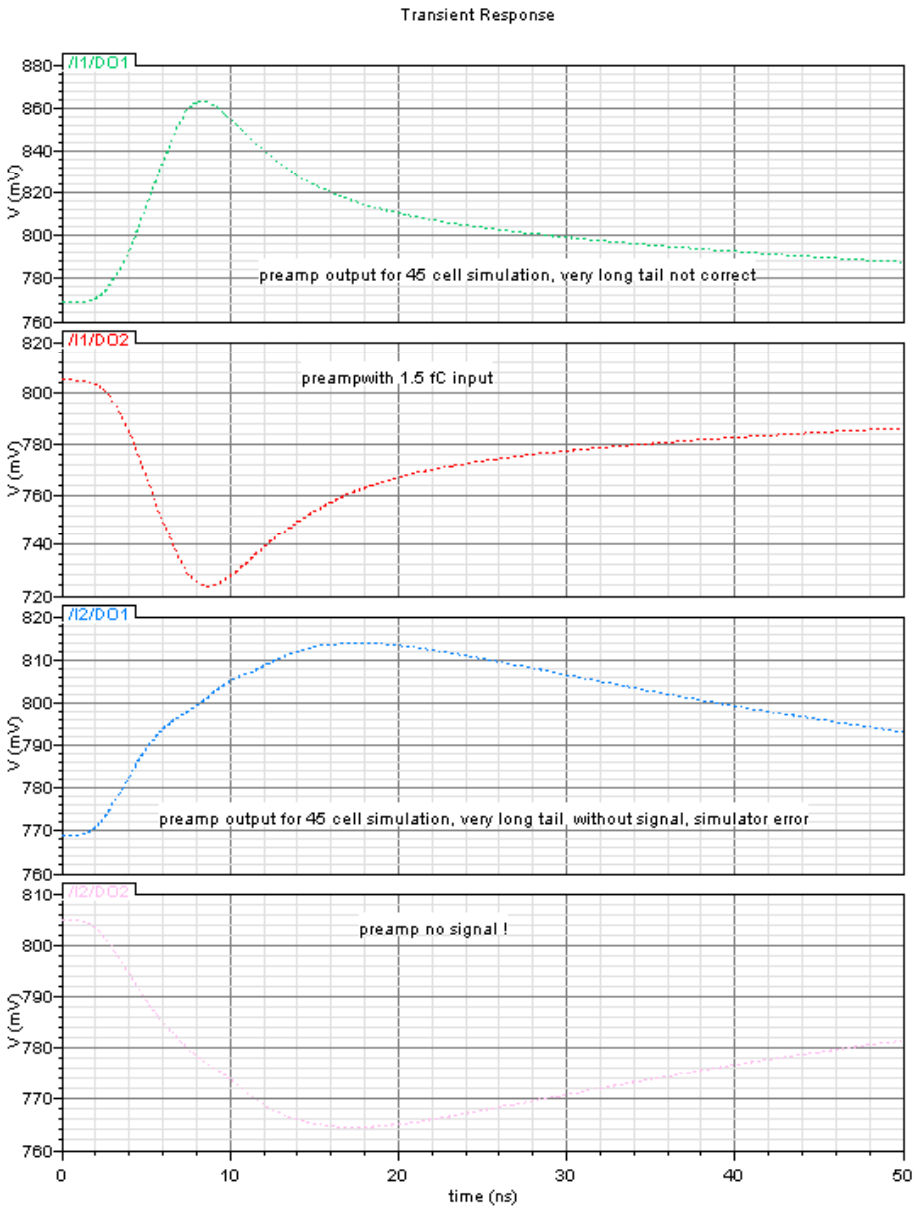
9 pixel top simulation



45 pixel top simulation



45 pixel Spectre crazy results



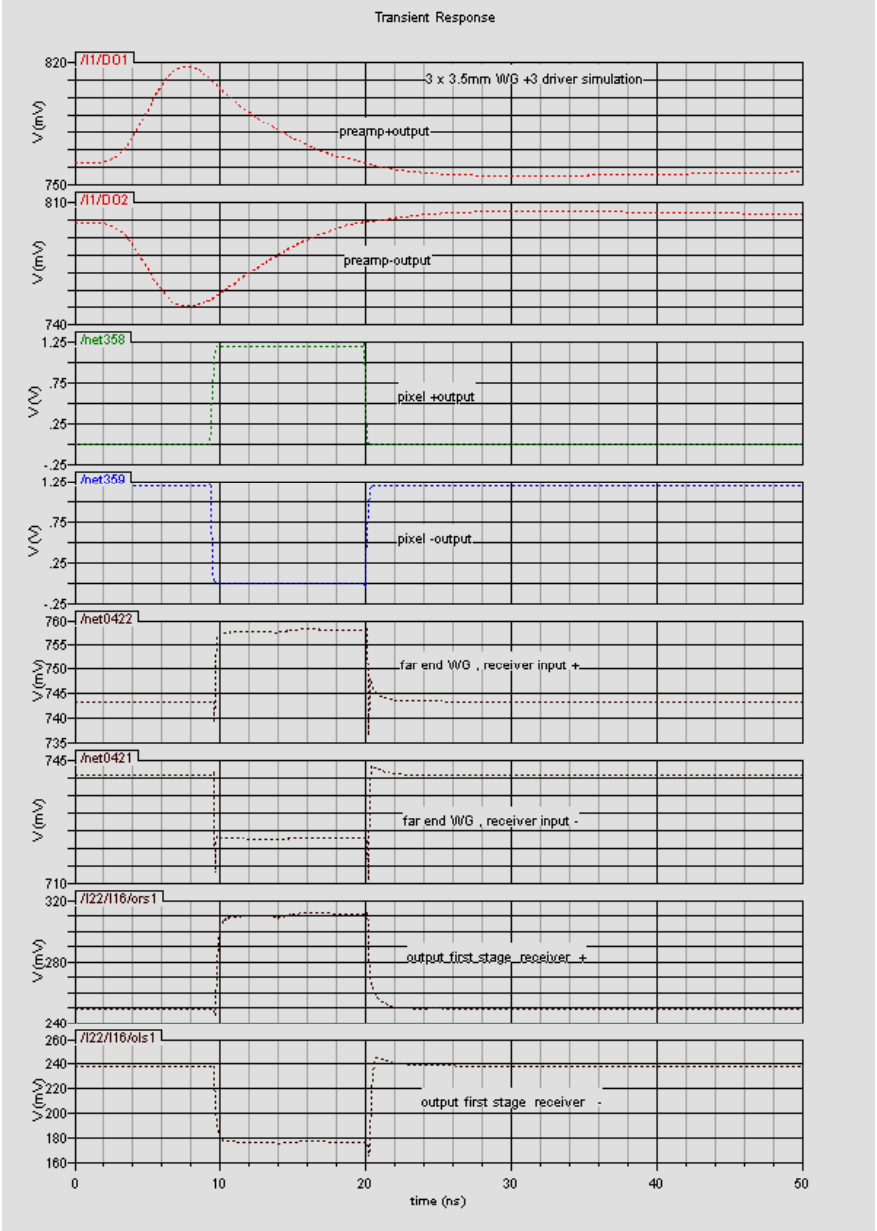
Simulation with a fresh file

From the one 9x9 block , a 2, 3, 4, 5 x9 simulations have been done gain.

Results are now satisfactory, here is for 3x9 bus (10.5 mm)

Input signal is 1.5 fC

From top to bottom:



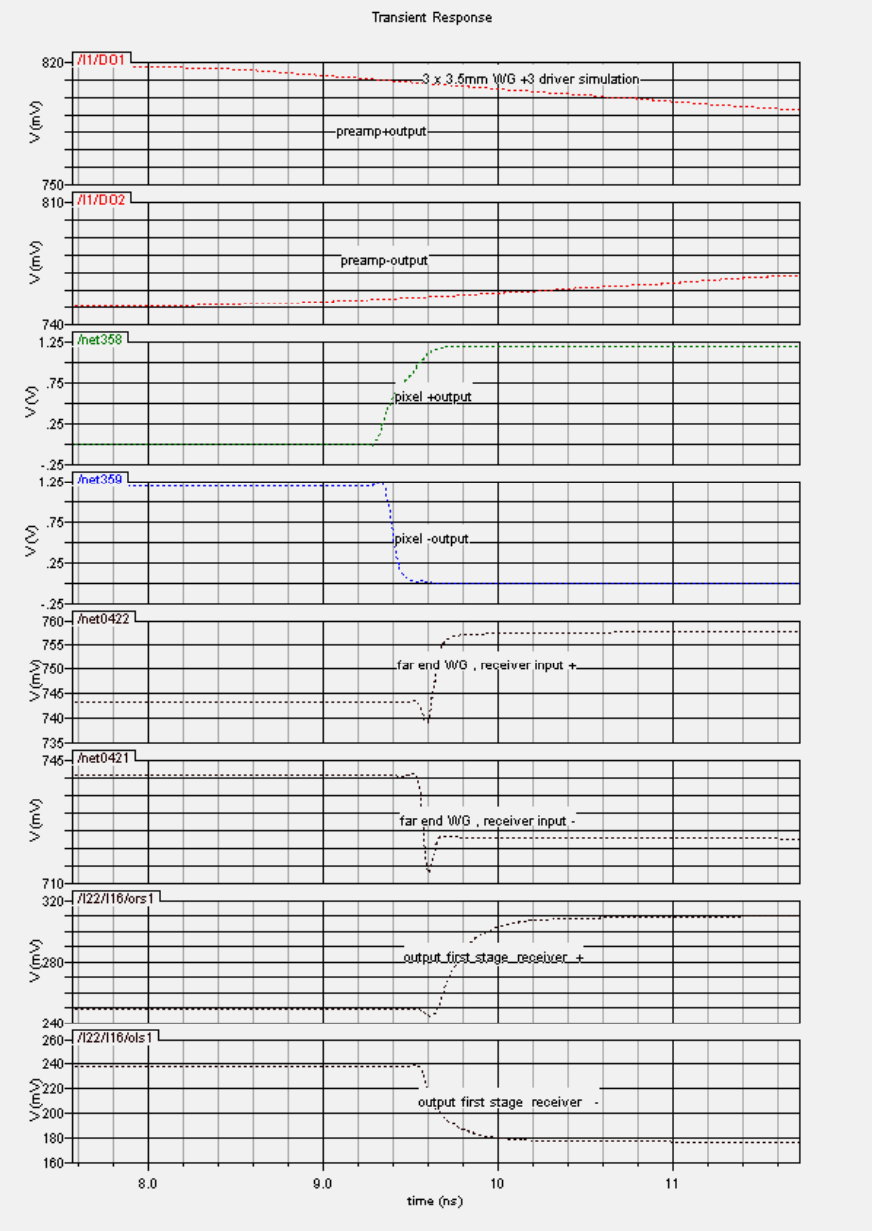
3x9 WG simulation data line

Close up

It turns out the fastest part of the circuit is the low swing waveguide with transition time of 50 ps.

Receiver first stage is 5 times slower.

the choice of the current in the simulation is 60 µA, a decrease to 30 µA might be possible



schedule

- November milestone turns out to be tough
  - Long delay in top analog simulation
  - Digital simulation of the full custom of the end of column TDC circuits needs Verilog modeling
  - Elena has started just now, she needs more than one month to finalize the complete database and finish floor-planning of the demonstrator and its verification.
  - Certainly we should postpone submission in January