Specification ASIC Demonstrator of the End Of Column (EOC) Architecture

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I. Introduction to the NA62 GTK EOC demonstrator

The basic principle of the end of column (EOC) architecture is that only the analog front-end, a time-over-threshold discriminator and a signal line driver is located in the pixel cell. The line driver sends the signal of each pixel to the EOC logic where the signal is processed in digital cells. The time measurement circuit is performed with DLL based TDCs. The time walk compensation is done via the measurement of the time-over-threshold. This architecture avoids the distribution of a clock signal over the entire pixel matrix. The line drivers are switching only when the corresponding cells are hit. This scheme allows a effective separation of digital and analog domain.

The final chip will contain 45 columns x 40 rows of 1800 300 µm x 300 µm pixels. Additional to test circuitry the core of the demonstrator comprises one full column of 45 pixels. 5 pixels share one line driver and one TDC hit register. Consequently 9 line drivers and 9 hit register banks are required. 5 pixels share are connected to one address line driver (see figure 1).

The two main goals of the EOC ASIC demonstrator are to assess the feasibility of a low noise pixel architecture based on a bus system using RF transmission lines for the communication between pixels and the end of column circuits, and demonstrate the feasibility to pack in the end of column 18 TDC circuits for each column. The choice of this pixel readout architecture was driven by the fact that data stream from pixel hits are entirely readout without being filtered by a trigger signal making the choice between on- pixel and the EOC architecture equivalent in terms of data flow. Besides those specific goals, the ASIC circuit should demonstrate its capability to process sensor signals as low as 1fC with a hit timing precision of 100 ps without being corrupted by induced digital noise. For this reason the architecture design puts the emphasis on minimum digital noise induced in the pixel array by avoiding digital circuits, clocks, and CMOS level in the pixel array to minimize the risk of crosstalk between digital activities and sensor and preamp input. In addition, the pixel circuit uses a TOT discriminator more robust to induced digital HF noise but more demanding in data bandwidth. Such circuit architecture has never been used for pixel readout and a feasibility study is mandatory.

In order to obtain a pixel circuit with a minimum digital noise, analogue front end, discriminator circuit, line drivers and transmission lines are differential. The transmission lines are a cross coupled pair operating at low differential current signal, 20 to 50 µA corresponding to a differential voltage swing of 10mV for an odd impedance of 100 Ω. No digital CMOS circuits are used in pixel cell except the differential line driver based on current switching. However, in order to reach the needed timing precision, it was necessary to compensate the dispersive losses of the resistive transmission lines by

introducing a current pre-emphasis in the current driver stage to force a propagation time down to 100 ps and avoid ns rise time at the receiver input.

The first 2007 test ASIC of the EOC GTK circuit was the NINO stage redesigned in 130 nm for an input capacitance of 250 fF. Though speed and functionality were satisfactory, noise was 3 times too high and no cure was possible since it was caused by the current mode configuration at the input stage. Therefore, a new fast preamplifier was designed from scratch [Jan Kaplon].

The EOC demonstrator circuit permit to characterize several new circuit designs: the fast low noise 5ns-preamplifier based on the Jan's ABCN circuit development, the new time over threshold 100ps-discriminator, partly based on Jan's comparator updated design and on a dynamic asynchronous latch comparator which is entirely new, and the transmission line receiver based on the NINO circuit deeply modified to decrease power consumption. All those analog circuits extending their bandwidth to GHz region are particularly challenging in terms of speed, noise and optimization, and several test structures are included in the design to characterize individual functional blocks. However, circuit characterization will be also challenging, 100 ps time resolution implies time measurement precision of below 50 ps. Furthermore the demonstrator allows the characterization of the DLL based TDC.

II. Content of the EOC demonstrator

1. Column demonstrator of 45 pixel cells bus connected to 9 cross coupled folded transmission lines 13.5 mm long for the data and 5 transmission lines for the pixel address. The readout is performed by 9 end of column TDC banks which are serially readout by 9 shift registers.
2. 9 pixel cells each connected to one 3.5mm transmission line. Readout is also performed by one end of column TDC circuit with serially readout by a shift register.
3. 2 pixel cells each connected to one 3.5mm transmission line, without the EOC TDC circuit. The transmission line output signal is a square pulse corresponding to a hit and is readout after the transmission line receiver with and without a LVDS driver.
4. One transmission line with its driver terminated by a 100 Ω resistance.
5. End of column only with the 18 receiver blocks readout serially. Few receiver inputs are connected to pads to be driven with a differential current from outside for time characterization with the IC tester time measurement unit.
6. Single pixel with analog output after preamp and first stage amplifier with an analog pad driver.
7. Single pixel with digital output, after discriminator followed by the line driver directly connected to pads; driven in current and 100 Ω off chip termination.
8. Set of MOS transistors for noise evaluation of the 130 nm technology.

III. (1) Column demonstrator 45 pixel cells

a. Circuit description

The demonstrator test chip consists of a small pixel array, with a single column bus connected to 9+5 receivers driving the EOC column TDC and pixel address circuits. The bus with a 13.5 mm in length and 45 pixels is folded into 5 smaller columns of 9 pixels connected together. The active pixel area is in this

case 2.7 mm x 1.5 mm forming a 9 x 5 bump pad array. Pixel address decoding is done by one transmission line common to each 9 contiguous pixel of each folded column.

The 45 pixel cells are identical and comprise the preamp, TOT discriminator, the double differential current driver adjustable from 20 µA to 50µA, and the transmission lines. In addition, for each pixel charge canbe injeccted individually with a calibration pulse. The pulse can be controlled with a mask register that is downloaded serially.

The 32 bit DLL runs on a 320 MHz external clock which corresponds to a time bin of 98 ps. In addition two 32 bit course counters provide a dynamic range of 13 seconds. One counter switches on the rising edge and the other on the falling edge of the clock in order to compensate for comprised values due to the asynchronous arrival time of the hit signal. The fine time is used to select one of the two counter offline.

The end of column logic of each of the 9 transmission lines is connected to one TDC bank. One TDC bank consists of two 32-bit hit registers, one for the leading and one for the trailing edge of the TOT signal, capturing the DLL state and thus indicating the fine hit time Furthermore one TDC bank contains 2 32 bit registers to capture the two coarse time counters. The TDC registers of one column are serially readout by line buffers without decoding.

b. EOC column read-out and data format

Upon arrival of a hit to the EOC logic, a rising edge and falling edge trigger are generated with which the hit time and address are captured and copied to the read-out register. In order to assess the influence of the read-out clock on the EOC logic two operation modes are available, the synchronous read-out and the asynchronous read-out.

When using the synchronous read-out a clock signal of up to 320 MHz is applied to this column continuously. The serial output line is low when no hit is available for read-out. Upon reception of a hit the line is set to ‘1’ for one clock cycle and then to ‘0’ for one clock cycle (header bits). Then the 197 bits of hit information (2 x 32 bit fine time, 2 x 2 x 32 bit course information, 5 bit address) are sent out serially. After that the line goes to ‘0’ if no hit has occurred in the meantime or immediately starts again the sequence. Using a 320 MHz clock yields a read-out time/frequency of 622 ns/1.6 MHz.

The asynchronous mode is used when the clock of the output line is not continuously running. The serial output line is set to ‘1’ when a hit arrived. The logic waits until the clock is applied and sends the data in 197 + 2 (header bits) clock cycles out. (see figure 2)

c. I/O Pads

Pads of the 45 pixel-folded column bus

Pad signal	level	number	comment
	Analogue		
Calibration pulse	analog	1	Common with the 9-pixel bus
Cal-Reg CLK	Digital CMOS	1	
Data-cal	Digital CMOS	1	
Comparator Threshold	Analogue voltage	2	VT1, VT2 Common with the 9-pixel bus
Driver bias current	Analogue current	1	Common with the 9-pixel bus
Preamp bias current	Analogue current	1	Iin Common with the 9-pixel bus
Shaper current	Analogue current		Ibpb Common with the 9-pixel bus
Comparator bias	Digital current		Icom Common with the 9-pixel bus
VB	Analogue current		VB Common with the 9-pixel bus
VC	Analogue current		VC Common with the 9-pixel bus
RX Signal Polarity	Voltage 0/ 1.2	2	Common with the 9-pixel bus
RX Threshold current	Analogue current	1	~ 10µA, Common with the 9-pixel bus
RX Gate voltage input	Analogue voltage	1	~ 250 mV, Common with the 9-pixel bus
RX amplifier bias	Analogue current	1	100µA, Common with the 9-pixel bus
	Power		
Digital ground	0	2	GNDD, Common with the 9-pixel bus
Analog ground	0	2	GNDA, Common with the 9-pixel bus
Analog VDD	1.2	1	VDDA, Common with the 9-pixel bus
Digital VDD	1.2	1	VDDD, Common with the 9-pixel bus
LVDS pad power	2.5	1	Common with the 9-pixel bus
	Digital		
9 serial output buffer	LVDS	18	
9 read-out clock	LVDS	(18)	
Clock	LVDS	2	320 MHz
LVDS power supply		2	
Reset CNT	CMOS	1	
Reset DLL	CMOS	(1)	ST7?
Total		**61**	

When possible multiply the power pads (in the corners)

IV. (2) Column demonstrator 9 pixel cells

The 9 pixel column is intended to compare performance with the 45 cell snake structure which corners may add RF signal reflection and deterioration. It is not possible to calculate and simulate with signal pre-emphasis as IBM has no corner modeling. The bias of the data lines of the bus has only one pixel contributing to the input bias current of the receiver whereas normally 5 pixels would bias the receiver input for the standard 45 bus lines. To compensate, an auxiliary bias current (~ 200 µA) is provided at the receiver inputs to get a drain current of at least 250 µA to bias the differential receiver cascode stage. This corresponds to a single ended termination resistance of 200 Ω.

The readout is the same that for the 45-column that uses the end of column TDC block.

Pads of the 9-pixel column

Pad signal	level	number	comment
	Analogue		
Calibration pulse	analog		Common with the 9-pixel bus
Cal-Reg CLK	Digital CMOS	1	
Data-cal	Digital CMOS	1	
Comparator Threshold	Analogue voltage		VT1, VT2 Common with the 9-pixel bus
Driver bias current	Analogue current		Common with the 9-pixel bus
Preamp bias current	Analogue current		Iin Common with the 9-pixel bus
Shaper bias	Analogue current		Ibpb Common with the 9-pixel bus
Comparator bias	Digital current		Icom Common with the 9-pixel bus
VB	Analogue voltage		VB Common with the 9-pixel bus
VC	Analogue voltage		VC Common with the 9-pixel bus
RX Signal Polarity	Voltage 0/ 1.2		Common with the 9-pixel bus
RX Threshold current	Analogue current		~ 10µA, Common with the 9-pixel bus
RX Gate voltage input	Analogue voltage		~ 250 mV, Common with the 9-pixel bus
RX amplifier bias	Analogue current		100µA, Common with the 9-pixel bus
Auxiliary bus bias	Analogue current	1	200µA
	Power		
Digital ground	0		GNDD, Common with the 9-pixel bus
Analog ground	0		GNDA, Common with the 9-pixel bus
Analog VDD	1.2		VDDA, Common with the 9-pixel bus
Digital VDD	1.2		VDDD, Common with the 9-pixel bus
	Digital		
9 serial output buffer	LVDS	18	
9 read-clock	LVDS	(18)	
Clock	LVDS		320 MHz
LVDS power supply			
Reset_CNT	CMOS		
Reset_DLL	CMOS		
Total		**39**	

V. (3) Two Transmission lines connected to 2 pixel cells and receiver

The goal is to optimize the transmission line bus. A change should be done in the pixel, calibration and mask should be suppressed, no shift register for Cal. To characterize the intrinsic properties of the transmission line, optimize the bias of the receiver it comprises one pixel cell driving a 13.5 mm 5 folded transmission line terminated with a receiver with a direct analog output buffered with source follower stages to optimize the transmission lines and a LVDS driver to readout time stamps with the IC test timing measurement unit. This receiver bias current determines this value and then can be adjusted

during the chip characterization to study the optimum load of the transmission line. The input resistance and receiver input voltage of the input cascode stage in weak inversion is,

$Rin = \frac{1}{gms} \cong \frac{nkT}{M.q.Id} =$ and $Vrx \cong Rin.Id \cong \frac{nkT}{q.M} \cong \frac{n.Vt}{q.M} \cong {}^{25mV}/_{5} \cong 5\,mV$, where $Vt = k.\frac{T}{q}$ is the thermal voltage , M is the number of driver connected to the line, Id is the driver current, Rin is the input resistance, Vrx is the input voltage signal which is theoretically independent of the receiver bias. In fact thermal voltage divided by M is the minimum receiver single ended signal swing, it is higher and square root dependent in strong inversion. For a low bias current, that is a low power budget, the response time becomes slower. This is one objective of the characterization of the test structure (3) to find the best trade-off between speed and power. Though the receiver input voltage is almost constant the 1st stage receiver output(1 kΩ) is proportional to the line current, that is 100 mV differential for the logic level adopted of 50µA.

Pad signal	level	number	comment
	Analogue		
Calibration pulse	analog	2	2 separate inputs
Transmission line analog out	Analog	2	
Pixel discriminator	Analogue voltage		VT1, VT2 Common with the 9-pixel bus
Driver bias current	Analogue current	1	
Preamp bias current	Analogue current		Iin Common with the 9-pixel bus
Shaper bias	Analogue current		Ibpb Common with the 9-pixel bus
Comparator bias	Digital current		Icom Common with the 9-pixel bus
VB	Analogue voltage		VB Common with the 9-pixel bus
VC	Analogue voltage		VC Common with the 9-pixel bus
RX Signal Polarity	Voltage 0/ 1.2		Common with the 9-pixel bus
RX Threshold current	Analogue current		~ 10µA, Common with the 9-pixel bus
RX Gate voltage input	Analogue voltage		~ 250 mV, Common with the 9-pixel bus
RX amplifier bias	Analogue current		100µA, Common with the 9-pixel bus
Auxiliary bus bias	Analogue current	1	200µA
	Power		
Digital ground	0		GNDD, Common with the 9-pixel bus
Analog ground	0		GNDA, Common with the 9-pixel bus
Analog VDD	1.2		VDDA, Common with the 9-pixel bus
Digital VDD	1.2		VDDD, Common with the 9-pixel bus
	Digital		
LVDS power supply		2	
LVDS output		4	
Total		**12**	

VI. (4) one transmission line with its driver without receiver

The objective of this test structure lay out in a 5-folded snake 13.5 mm structure is to characterize the intrinsic speed property of the transmission line by on chip termination with 100 or 200 ohm. The line has its current driver and an auxiliary. Line is driven by its driver and input of the receiver has an auxiliary bias x4 driver current.

Pad signal	level	number	comment
	Analogue		
Calibration pulse	Cal pulse	2	2 separate inputs
Transmission line analog out	Analog	2	
Driver bias current	Analogue current	1	
RX amplifier bias	Analogue current		100µA, Common with the 9-pixel bus
Auxiliary bus bias	Analogue current	1	200µA
	Power		
Digital ground	0		GNDD, Common with the 9-pixel bus
Digital VDD	1.2		VDDD, Common with the 9-pixel bus
Total		**12**	

VII. (5) End of column only with its receiver block

d. Description

It consists of one DLL and one TDC block forming the end of column of a transmission line without a coarse register. TDC's are externally controlled and readout serially with a line buffer 64-bit data and are connected off chip with a LVDS driver.

e. Pads

- Trigger in TDR — ST11
- Trigger in TDF
- TDC's hit input — 2
- Clock 320 MHz — 2
- Serial output LVDS — 2
- Read-out clock LVDS — 2
- Digital GND and VDD connected internally
- Reset — ST13
    - Total — **8**

VIII. (6) Single pixel with analog output (preamp)

f. Description

It consists of a bump pad connected to the preamplifier followed by a driver to go off chip. The objective of the test structure is to measure the preamp noise only.

g. I/O signals

Analog pads

- Calibration input 20 fF, 1
- Analog signal outputs 2
- Bias currents common with column
- Power lines connected to the main column
    - Total **3**

IX. (7)Single pixel with digital output, after discriminator

h. Description

It comprises a bump pad connected to the preamp and to the discriminator. The objective is to measure the output of the NINO LCO discriminator to evaluate the entire characteristics of the pixel channel, noise, gain, speed, walk, etc...

i. I/O pads

Analog pads

- Calibration input 20 fF, 1
- Bias currents common with column
- Power lines connected to the main column

Digital pads

- Output NINO LCO with LVDS driver 2
- Digital output ground return 1
    - Total **4**

X. Set of MOS transistors for noise evaluation

j. Description

It comprises 2 PMOS and 2 NMOS of different size with common source. It is intended to characterize the noise of 130 nm technology.

k. Pads

- One common source NMOS 1
- One common source PMOS 1

-	Gate1 NMOS	1
-	Gate2 NMOS	1
-	Gate1 PMOS	1
-	Gate2 PMOS	1
-	Drain1 NMOS	1
-	Drain2 NMOS	1
-	Drain1 PMOS	1
-	Drain2 PMOS	1
	Total	**10**

If too many pads then put only NMOS transistors

XI. Pad rings

in MIC three bonding pad designs exist, one developed by Paulo 113 µm width (large), one developed by Raphael, 75 µm width (narrow), and one used by Matthieu, 87.5 µm width. If one uses for analog pads 75 µm pad, on the height of 3mm (3.5 –corners), one can put 40 pads. On the width of 3 mm, one can put 40 narrow, or 26 large ones. To arrange 77 pads, we should use only the narrow ones, unless to resize the demonstrator chip.

Arranging the pads in double rows in considered. However, it must be verified that the pad lengths is sufficient for wire bonding.

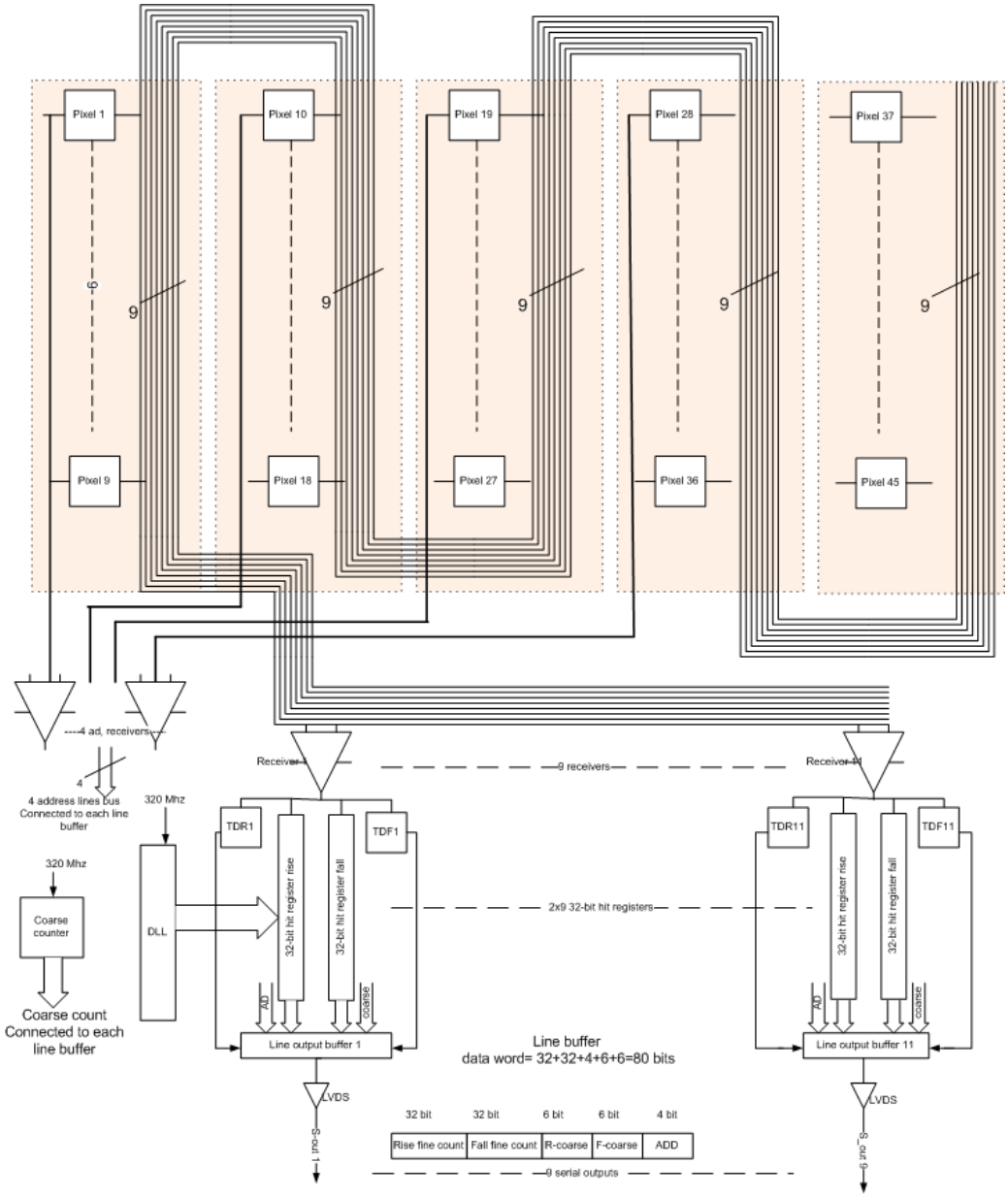

Figure 1 block diagram of the 45 pixel column demonstrator

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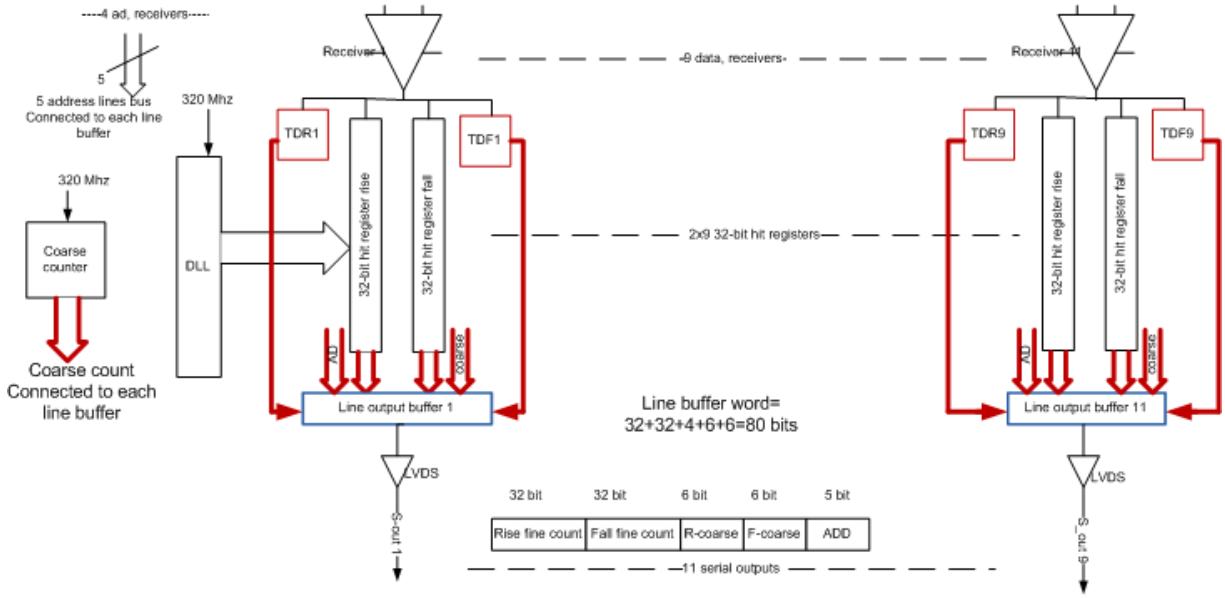
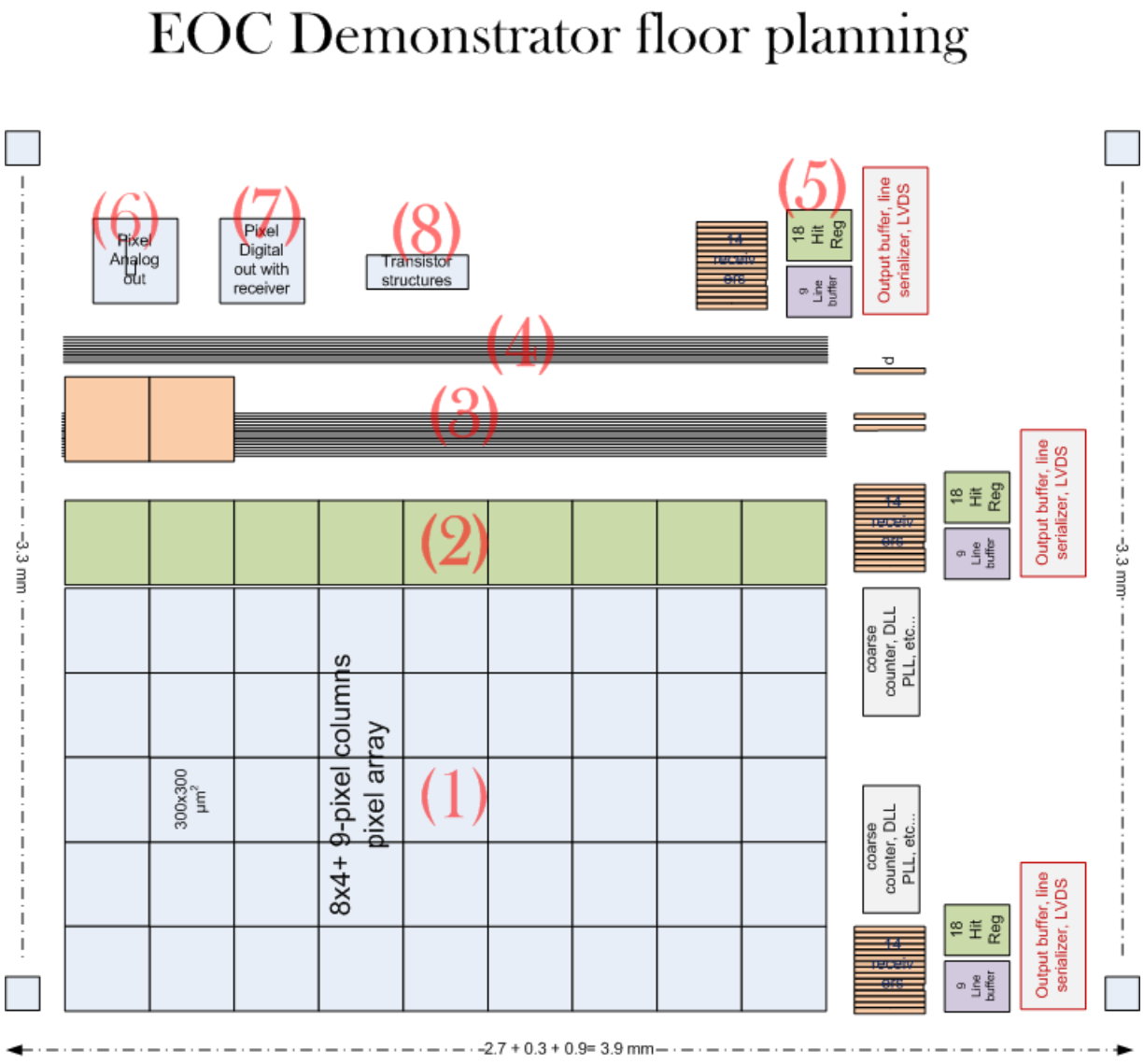
Figure 2 Readout interface, in red lines is the serial readout circuit, LVDS block, the coarse counter is changed to 20 bits format.


----4 ad. receivers-----
5
5 address lines bus
Connected to each line buffer
320 Mhz
320 Mhz
Coarse counter
Coarse count
Connected to each line buffer
DLL
Receiver 1
-9 data, receivers-
Receiver 11
TDR1
TDF1
TDR9
TDF9
32-bit hit register rise
32-bit hit register fall
2x9 32-bit hit registers
AD
coarse
Line output buffer 1
Line output buffer 11
Line buffer word=
32+32+4+6+6=80 bits
LVDS
S_out 1
S_out 9
32 bit
32 bit
6 bit
6 bit
5 bit
Rise fine count
Fall fine count
R-coarse
F-coarse
ADD
11 serial outputs

Layout



1. Column demonstrator of 45 pixel cells bus connected to 9 cross coupled folded transmission lines 13.5 mm long for the data and 5 transmission lines for the pixel address. The readout is performed by the end of column TDC circuit which is serially readout by a shift register.
2. 9x 3.5mm transmission lines, each connected to one pixel, readout is also performed by the end of column TDC circuit which is serially readout by a shift register.
3. 2x 3.5mm transmission lines each connected to one pixel, without the EOC TDC circuit, output signal a square pulse corresponding to hits is readout after the receiver with and without a LVDS driver
4. One transmission line with its driver and terminated by 100Ω resistance
5. End of column only with the 18 receiver block readout serially. Few receiver inputs are connected to pads to be driven with a differential current from outside for time characterization with the IC tester time measurement unit.
6. Single pixel with analog output after preamp and first stage amplifier with an analog pad driver.
7. Single pixel with digital output, after discriminator followed by the line driver directly connected to pads; driven in current and 100Ω off chip termination.
8. Set of MOS transistors for noise evaluation of the 130 nm technology.

Q&A

Why do you mention now 3.5 mm, how large are the lines in point1?

I mentioned in (1) 13.5mm a full column folded in 5 segments of 3.5 mm. line (2) is this segment of 3.5 mm

How is it driven and read-out?

It is driven with 2 anti-phase CMOS voltage pulse signal off chip that simulate the pixel cell outputs, the readout is done by readout out the voltage signal of the 100 ohm termination. The test should be performed by the IC tester.

What does it mean?

The structure uses the line driver as an output buffer which provides anti-phase 50 uA signals that are pull down with a off chip resistor, 100 ohm or higher. This test is foreseen to be done with the IC tester

How can that be adjusted?

The bias current of the line drivers, 2 separate for address driver and data driver as supposed to be supplied off chip and then are adjustable

How would you send the inputs?

Just as a separate pads internally or externally terminated with 50 ohm and connected to the input with an on chip 200 fF capacitor.

What is the difference between TDR/TDF and TDC hit input?

The TDR and TDF are supposed to be generated from leading and trailing edges of the output of the receiver by a monostable circuit that calibrated pulse width to 2 or 3 ns. This circuit is inspired from asynchronous digital memory, it is usually called Address Transition Detector (ATD).