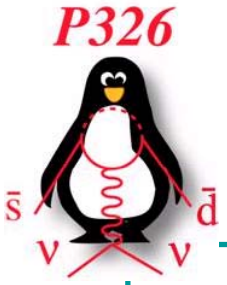


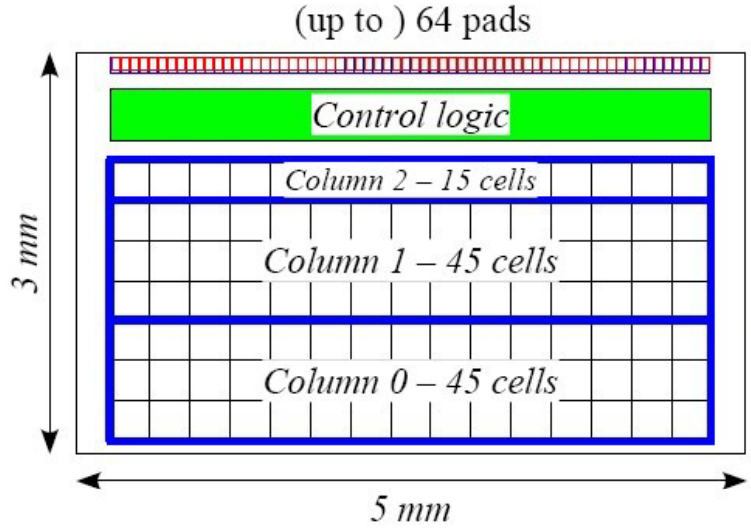
INFN Torino
Istituto Nazionale di Fisica Nucleare

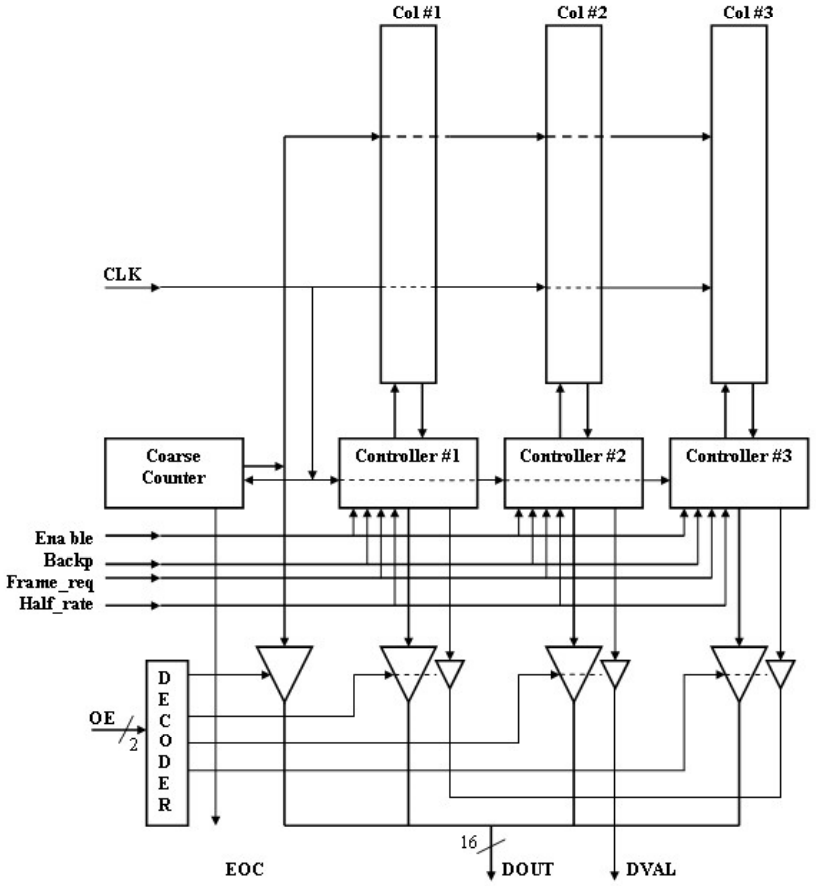
ON-pixel TDC End of Column circuit

Giulio Dellacasa

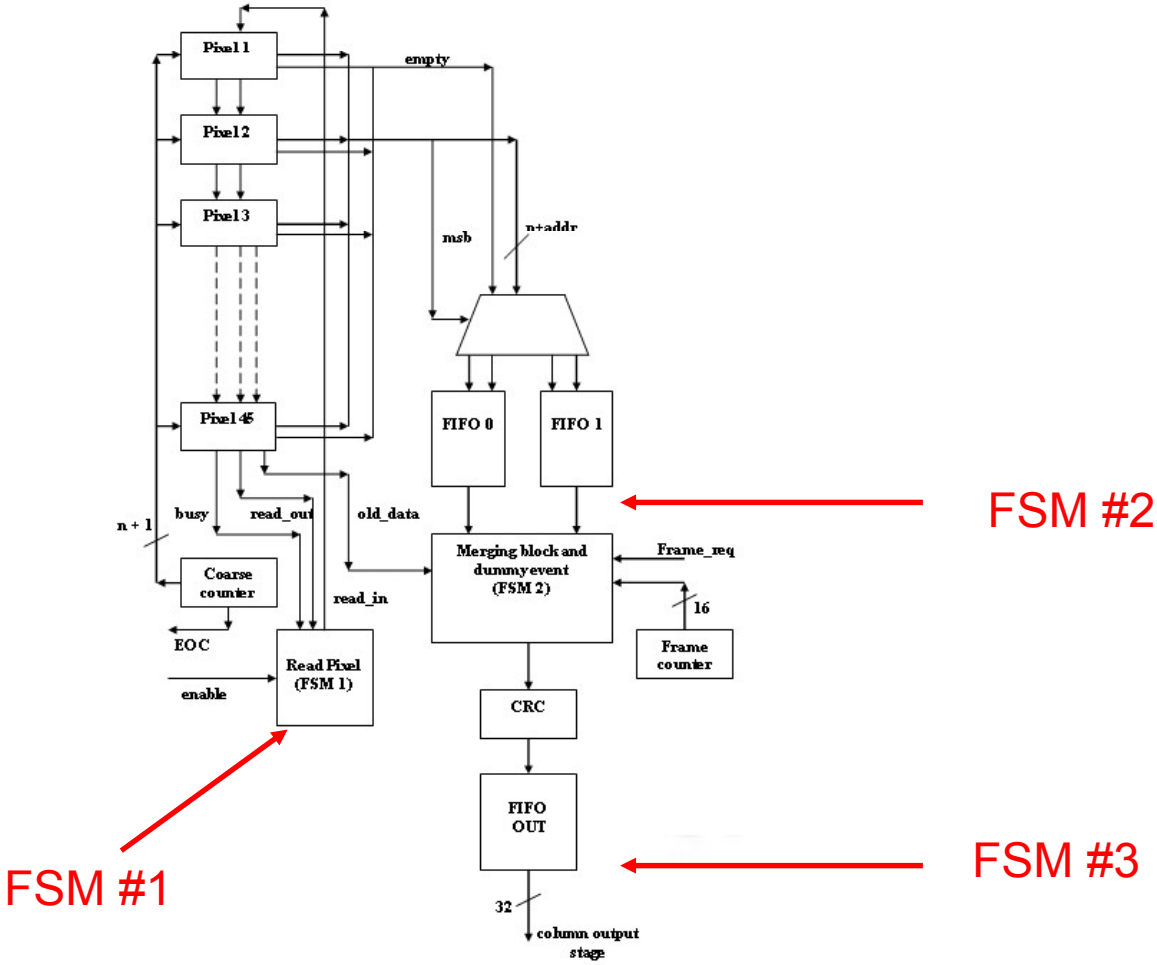
Design review of the NA62 GTK ASIC demonstrator circuits

Demonstrator chip

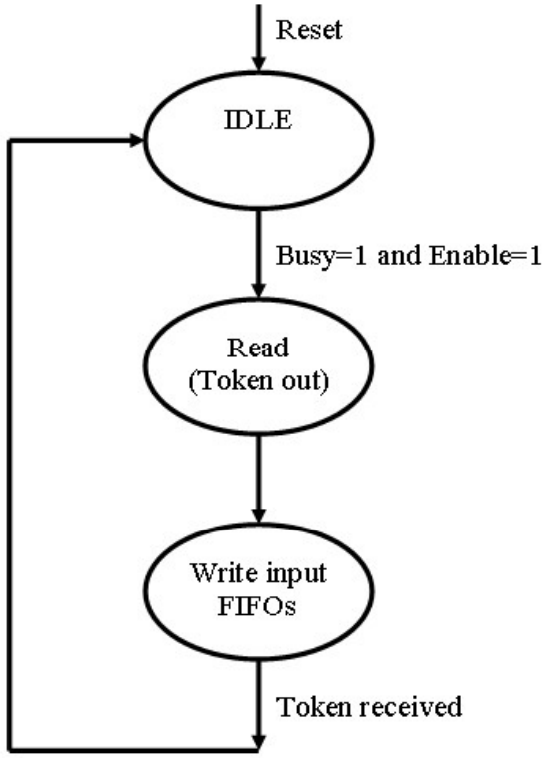




End of Column

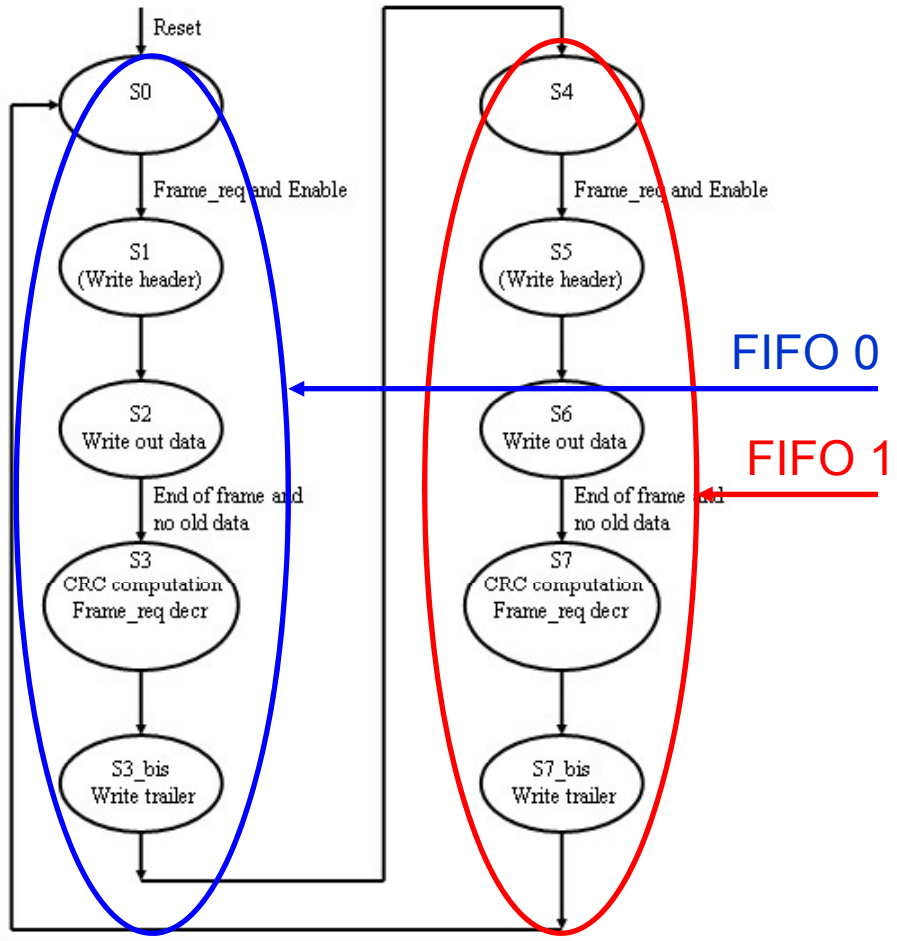


FSM #1



- Idle state: waits for at least 1 data in the pixels column (busy =1)
- Read State: sends out the token
- Write state: write the input FIFOs Empty from pixels (negated) is used as FIFO write enable and Coarse counter MSB used for FIFO selection (0 or 1)
- Write state is hold until the token is received back from the pixels column

FSM #2



- FSM #2 which is responsible of data formatting, is full symmetric for FIFO 0 and FIFO 1
- Frame request issue: without any frame request data are still written in the two interchanging FIFOs but not sent to the output FIFO. So the use of this signal is not trivial in order to avoid data mixing between different frames

EoC Data Format

Frame header

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1						Frame number																							

Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				Column address				Pixel address						Coarse measure										Fine measure									

Frame trailer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0						Word counter								CRC-16															

- Data are grouped in Frames
- Definition of Frame: all the data which belong to the same turn of the Coarse Counter (6,4 μs)

CRC (Cyclic Redundancy Check)

$$p(x)/g(x) = q(x) + r(x)$$

$$m(x) = p(x) + r(x)$$

CRC

Where:

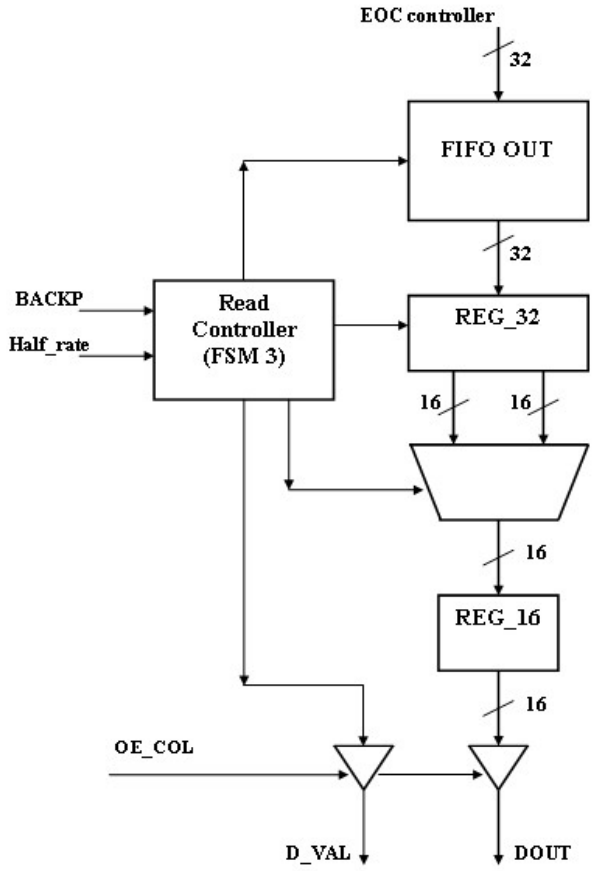
- p(x) message to transmit (our data)
- g(x) polynomial
- r(x) reminder
- m(x) transmitted message

- CRC operation is performed word by word, updating the CRC value each step
- In our case, for the Trailer word the CRC is calculated forcing the CRC field to 0 and then the correct value is appended

CRC: polynomial

- The selection of polynomial is crucial, but its goodness is based on the experience. So a standard poly is recommended
- CRC-16: selected polynomial is $X^{16}+X^{15}+X^{2}+1$
- IBM and USB standards, also used in the CMS DAQ
- CRC-16 detects: single errors, double errors and burst errors (lower than 16 bit), odd number of errors. In total 99.9984 % of errors can be detected (for data length less than 2^{15} bit, so 1024 words of 32 bit)

The output stage

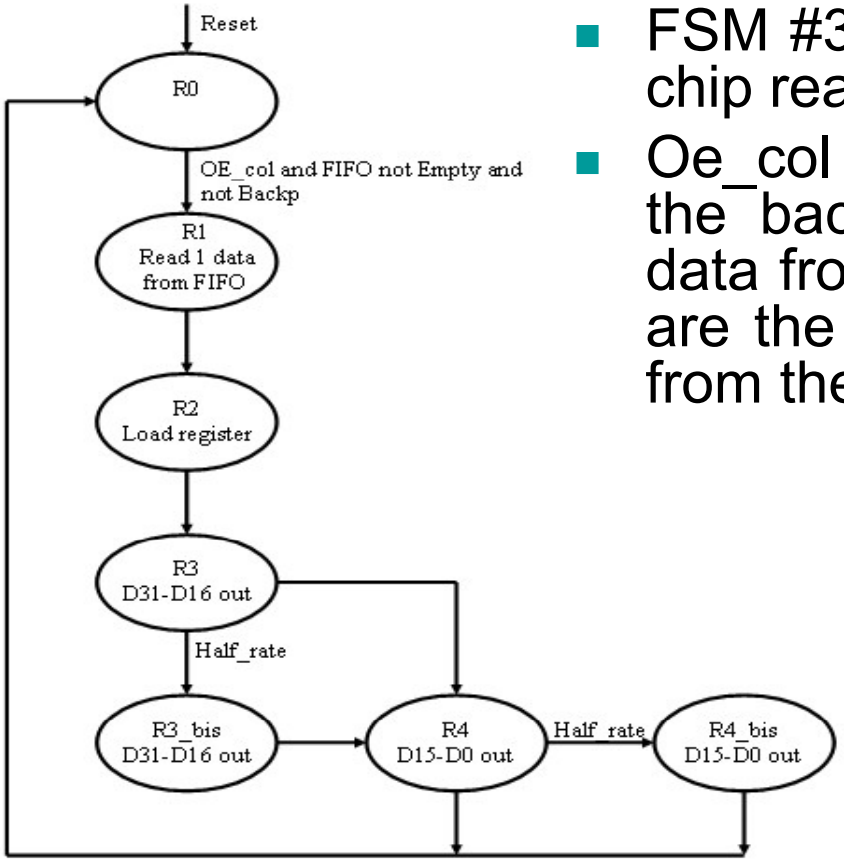


Readout Options

In order to slow down the output bus speed and to simplify the test/debug operations a set of options is provided:

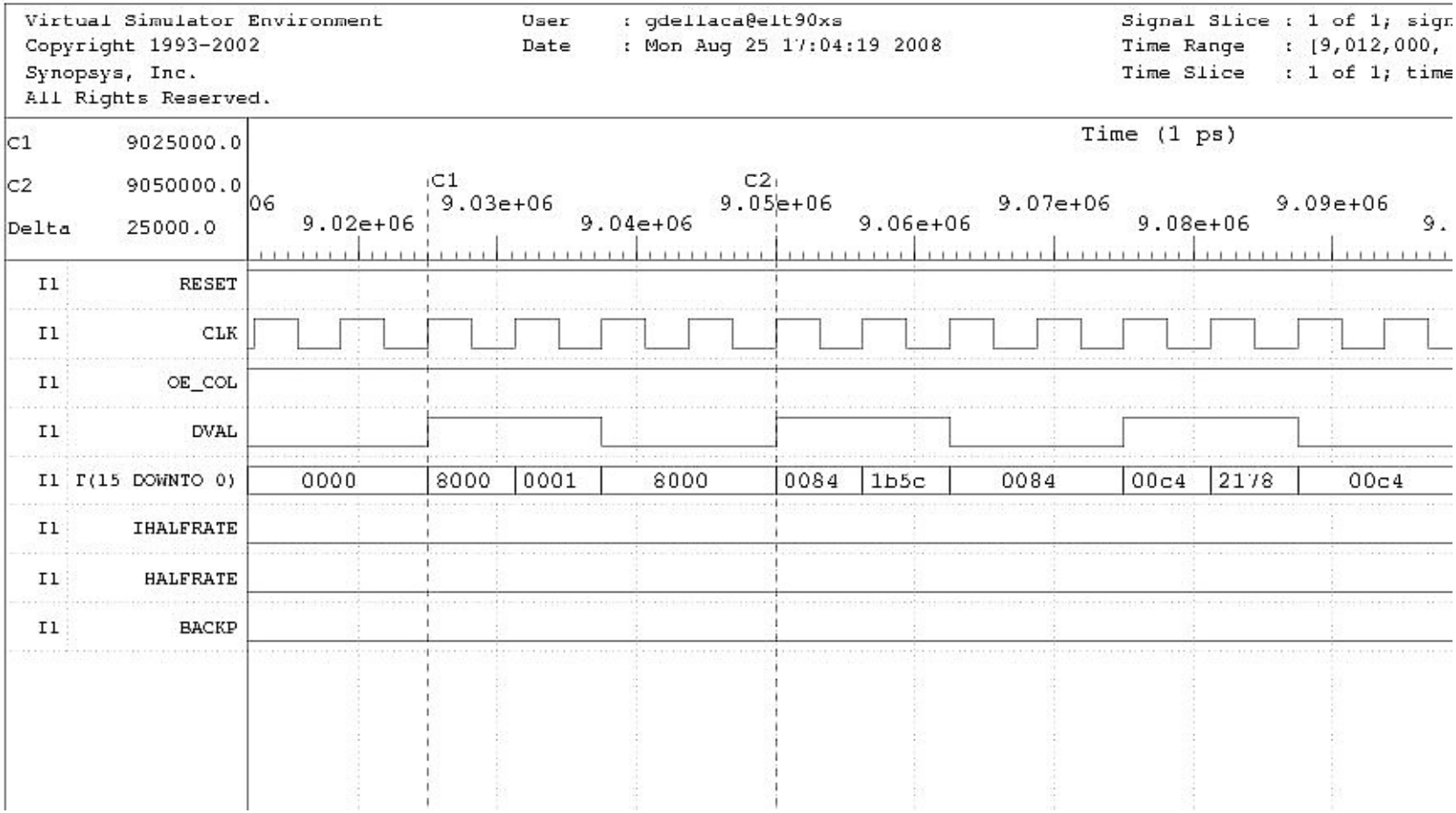
- Frame request: when asserted (H with a pulse width: 1÷16 clock cycles) ONLY ONE frame is transmitted to the output FIFO. If it is asserted for a longer time, ALL the frames are transmitted to the output FIFO, until the signal is released. If the signal is always down nothing is sent to the output FIFO
- Back pressure. When this signal is asserted (H) all the read operations are stopped (no data on the output bus, but still sent to the output FIFO)
- Half rate: when asserted (H) the output bus (and its Dval flag) can be synchronized with an external 80 MHz clock

FSM #3

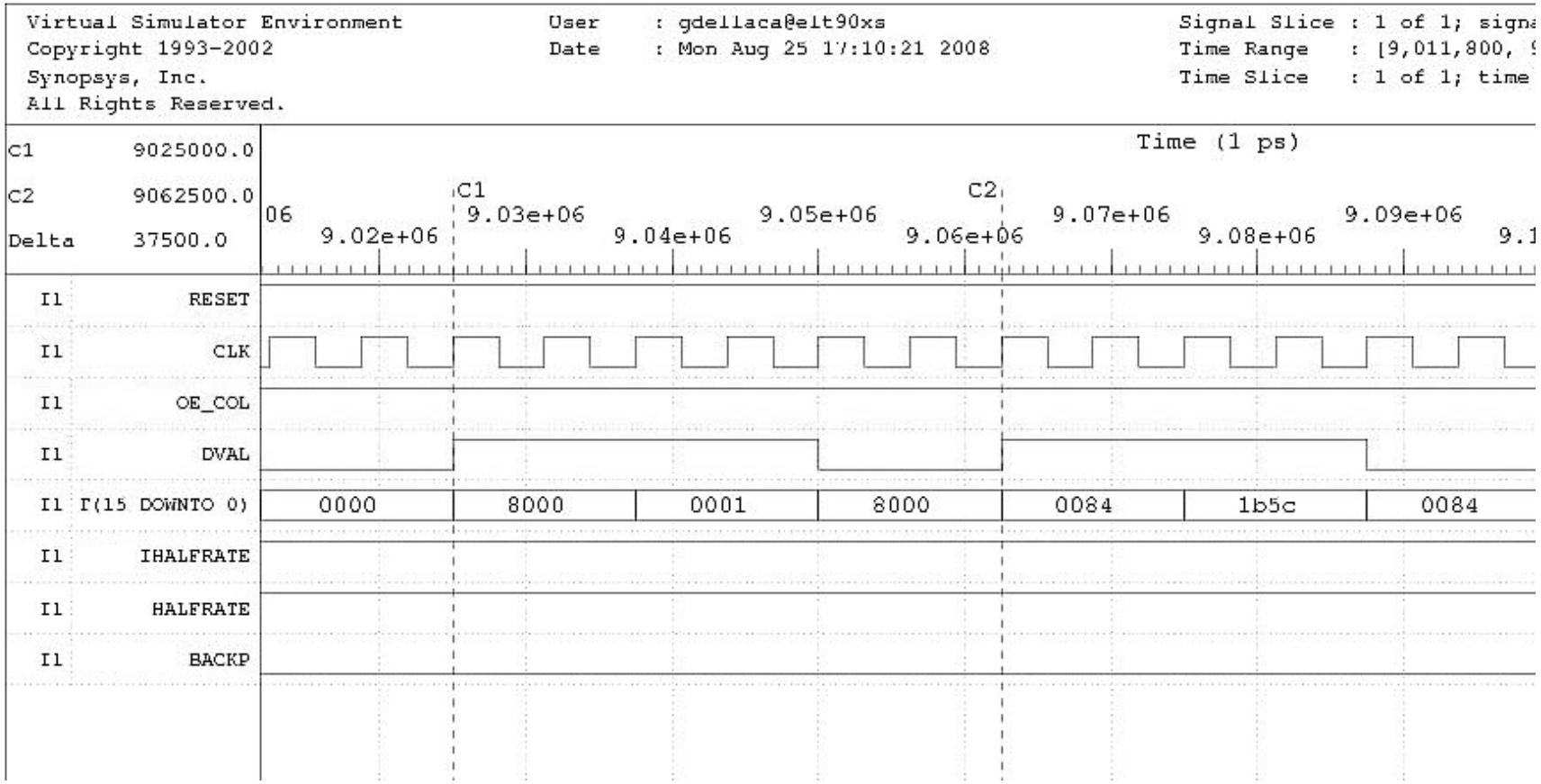


- FSM #3 is responsible of the off-chip read-out
- Oe_col is used in conjunction with the backpressure to extract one data from the output FIFO. Those are the two only controls to drive from the external

Half Rate off



Half Rate on


Virtual Simulator Environment
Copyright 1993-2002
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All Rights Reserved.
User : gdellaca@elt90xs
Date : Mon Aug 25 17:10:21 2008
Signal Slice : 1 of 1; signa
Time Range : [9,011,800,
Time Slice : 1 of 1; time
C1 9025000.0
C2 9062500.0
Delta 37500.0
Time (1 ps)
C1
C2
06
9.02e+06
9.03e+06
9.04e+06
9.05e+06
9.06e+06
9.07e+06
9.08e+06
9.09e+06
I1 RESET
I1 CLK
I1 OE_COL
I1 DVAL
I1 I(15 DOWNTO 0)
0000
8000
0001
8000
0084
1b5c
0084
I1 IHALFRATE
I1 HALFRATE
I1 BACKP

Probable critical issues

- Synchronization between pixels cells and EoC circuit
- Synchronization between EoC output bus and DAQ board
- For those reason clock distribution is crucial along the whole chip, in order to avoid skews between different parts of the circuit

Used tools

- VHDL simulations: Synopsys Scirocco VCS-MX v.2006.06
- Synthesis: Synopsys Design Vision v.2006.06
- Digital routing: Cadence Encounter 6.2
- Post-layout simulations: Cadence (Verilog)

Simulations

FIFOs Depth	N. Events @140 kHz	Max.words	Lost Evt. Dead time	Lost Evt. FIFO full	Theory
4	10000	3	~0,25%	0	0,008 %

$$P_{Lost}(n) = 1 - \sum_{0}^{n} \frac{\rho^n e^{-\rho}}{n!}$$

ρ=λT=0.108 (freq. x Conv. Time)

Hits rate (kHz)	**Dead time lost events**	**Coarse FIFO lost events**	**Output FIFO lost events**
140	18	0	0
160	18	0	0
180	19	0	0
200	25	1	0
220	22	0	0
240	26	1	0
260	28	3	0
280	31	4	0