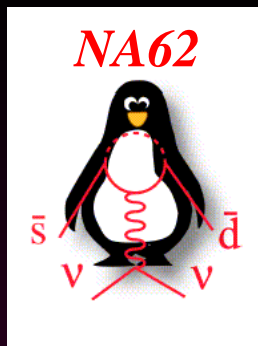


# GTKpix design review



Sezione di Torino

- On chip digital circuits
- Column buses



# GTKpix design review

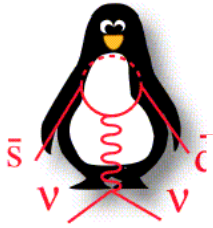


Sezione di Torino

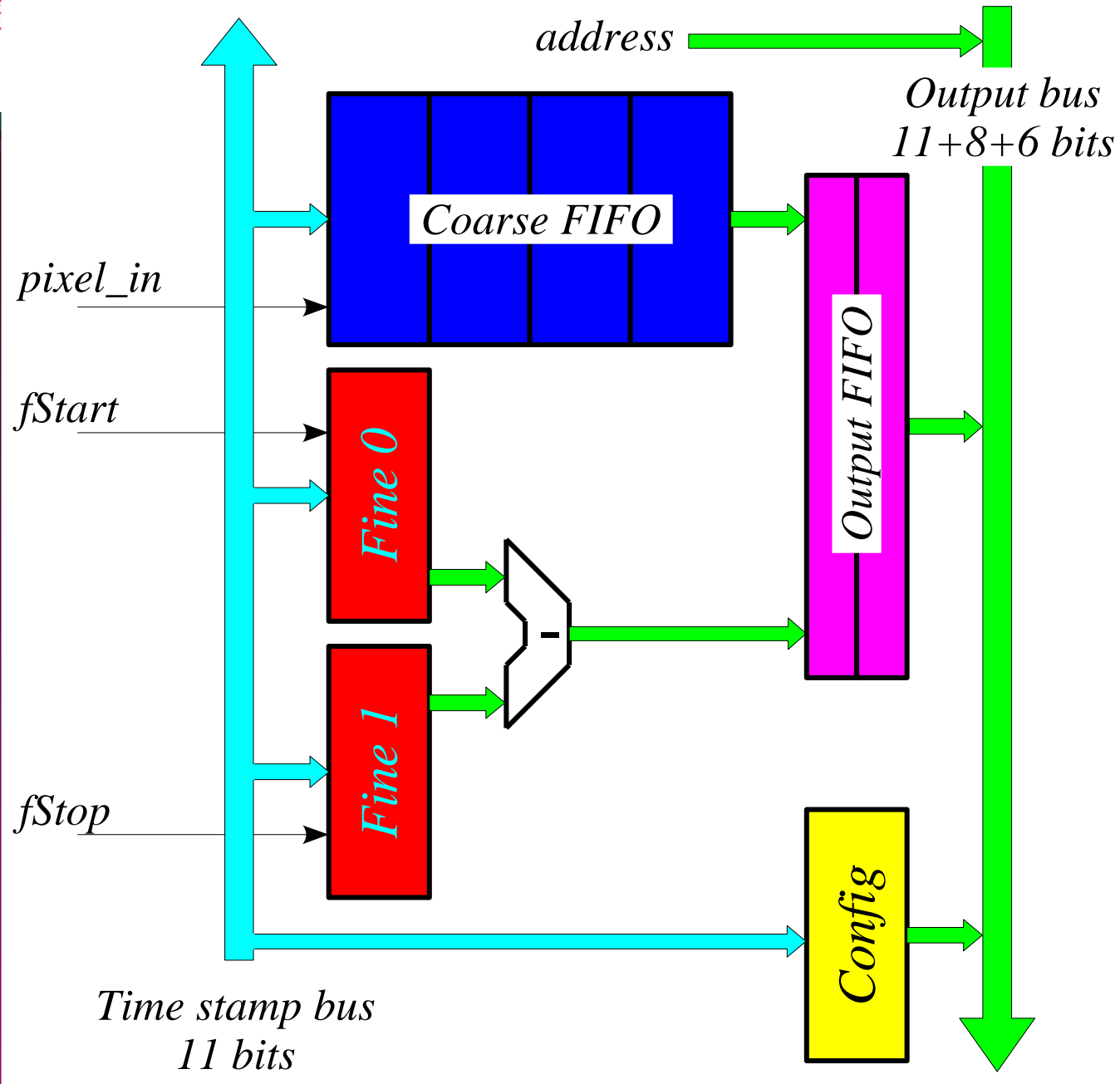
→ On chip digital circuits

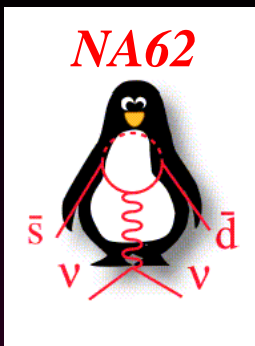
→ Column buses

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# Pixel logic





# Registers



- \* Hamming-protected (SEC) registers with reload of the correct data at the next clock cycle
- \* Coarse time FIFO : 4x11 bits, 4x15 dFFs (15,11 encoding)
- \* Fine time registers : 2x8 bits, 4x12 dFFs (12,8 encoding)
- \* Configuration registers : 2x4 bits, 2x7 dFFs (7,4 encoding)

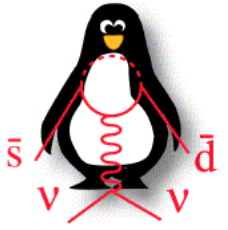


# Control logic



- \* Hamming encoded state machines for SEU tolerance
- \* Automatic synthesis and P&R
- \* ARM standard cell libraries
- \* Estimated size :
  - ➔  $150 \mu\text{m} \times 290 \mu\text{m}$  @ 66% occupancy
  - ➔  $130 \mu\text{m} \times 290 \mu\text{m}$  @ 74% occupancy
  - ➔  $110 \mu\text{m} \times 290 \mu\text{m}$  @ 88% occupancy

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# Hamming encoding



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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	P <sub>0</sub>	P <sub>1</sub>	D <sub>0</sub>	P <sub>2</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	P <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	P <sub>4</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>
P <sub>0</sub>	X		X		X		X		X		X		X		X		X		X
P <sub>1</sub>		X	X			X	X			X	X			X	X			X	X
P <sub>2</sub>				X	X	X	X					X	X	X	X				
P <sub>3</sub>								X	X	X	X	X	X	X	X				
P <sub>4</sub>																X	X	X	X

$$n \leq 2^k - k - 1$$

$$D_{n-1} \dots D_0$$

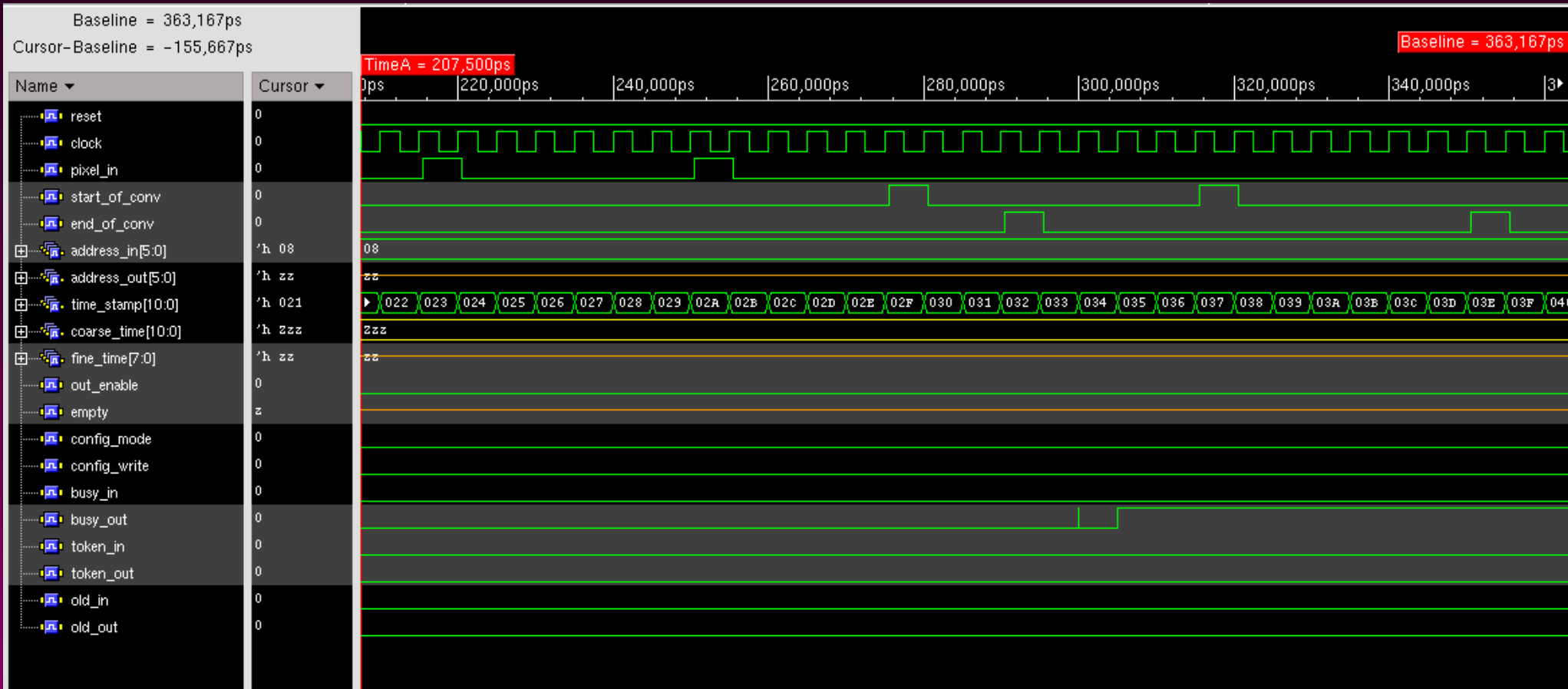
$$P_{k-1} \dots P_0$$



# Event acquisition



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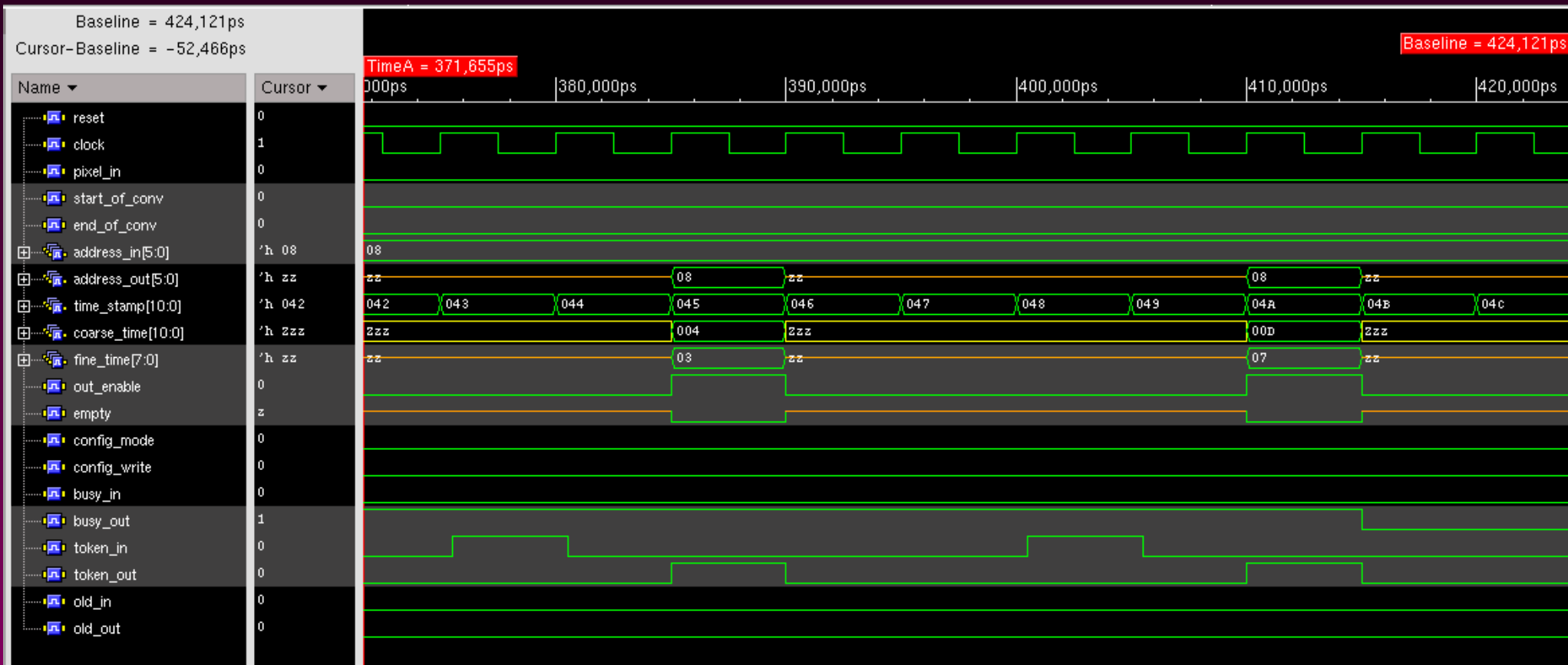




# Event transmission



Sezione di Torino



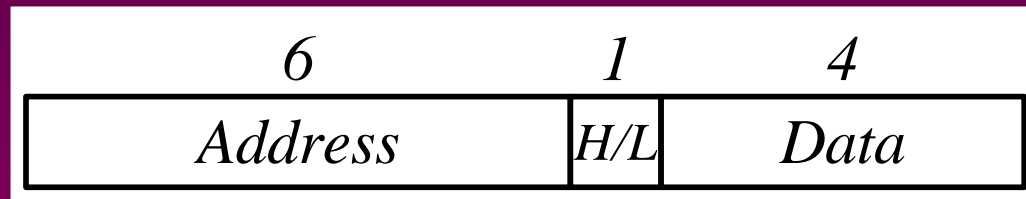


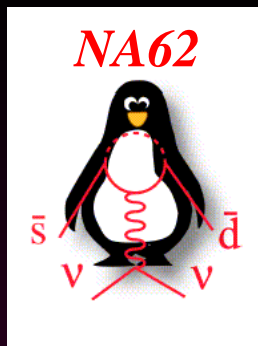


# Configuration mode



- \* Data sent on the time stamp bus
- \* Two 4 bits registers
- \* Two control signals : *config\_mode* and *config\_write*
- \* No hit accepted when *config\_mode* is high
- \* Packet format :

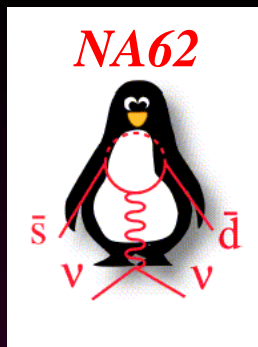




# GTKpix design review



- On chip digital circuits
- Column buses



# Signal types



Sezione di Torino

- \* Input common signals
- \* Local I/O signals
- \* Output common signals
- \* fastOR-chained signals



# Input signals



i. reset

ii. clock

← *most critical signal !*

iii. time\_stamp

← *bus, 11 bits*

iv. config\_mode

v. config\_write

- \* Transmission via pseudo differential CMOS levels
- \* DCVSL receivers



# Clock transmission



Clock is the most critical signal ( jitter  $< 100$  ps )

Clock line options :

- \* Current mode differential line with low impedance termination ( high power )
- \* Clock tree with CMOS buffers ( layout complexity )
- \* Local clock regeneration in each pixel ( pixel-dependent delay can lead to synchronization problems )

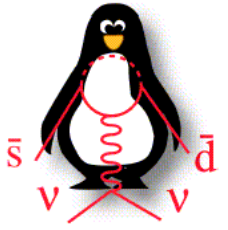


# Rough calculations



- \* Minimum size and space MG with MA backplane
- \*  $R = 0.04 \text{ m}\Omega/\square \cdot 300 \mu\text{m} / 0.4 \mu\text{m} = 30 \text{ m}\Omega/\text{pixel}$
- \*  $C = (0.0402 + 0.0734 \cdot 2) \text{ fF}/\mu\text{m} \cdot 300 \mu\text{m} = 56.1 \text{ fF}/\text{pixel}$
- \*  $R_{\text{COL}} = 1.35 \Omega, C_{\text{COL}} = 2.5 \text{ pF}$
- \*  $T_{\text{RISE}} = 200 \text{ ps} \cdot 0.22 \cdot 2 \cdot \pi \cdot R_{\text{T}} C_{\text{COL}}$  for 20%-80%
- \* Distributed RC  $\rightarrow$  factor of 2 gain  $\rightarrow R_{\text{T}} = 100 \Omega$
- \*  $I_{\text{DRV}} \approx 5 \text{ mA}$  every two column (67  $\mu\text{W}/\text{pixel}$ )

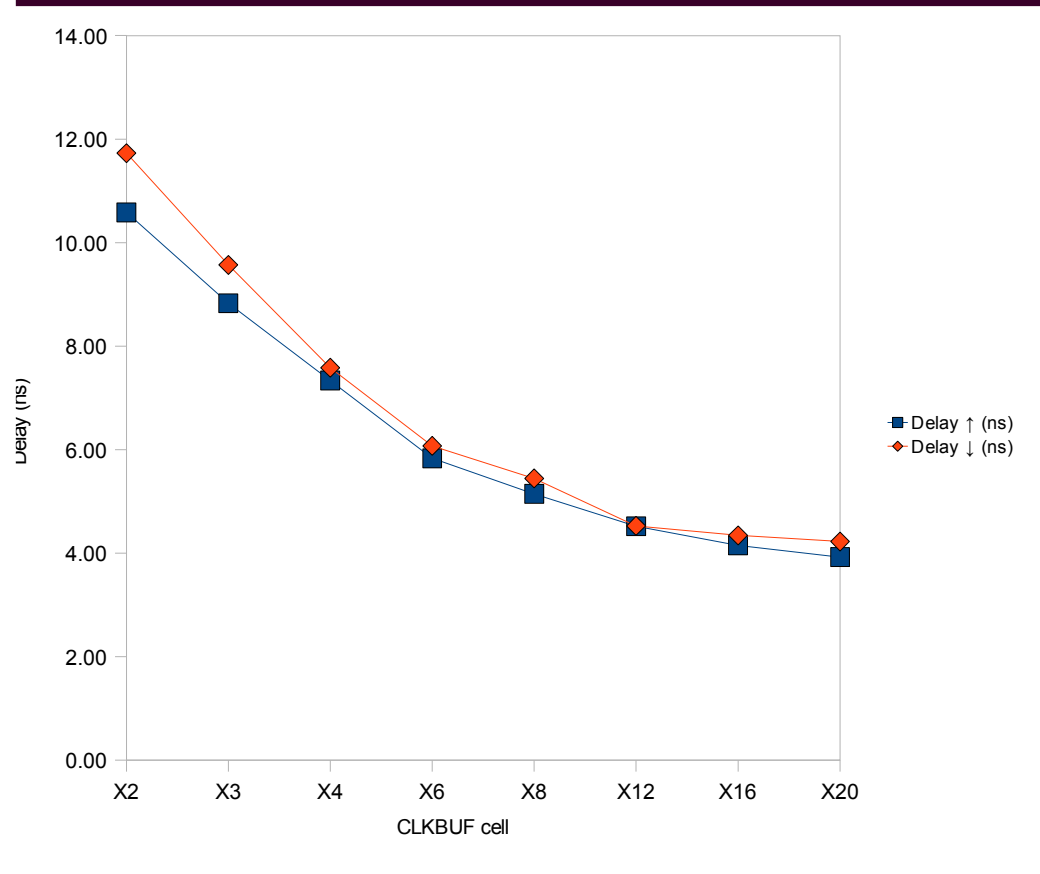
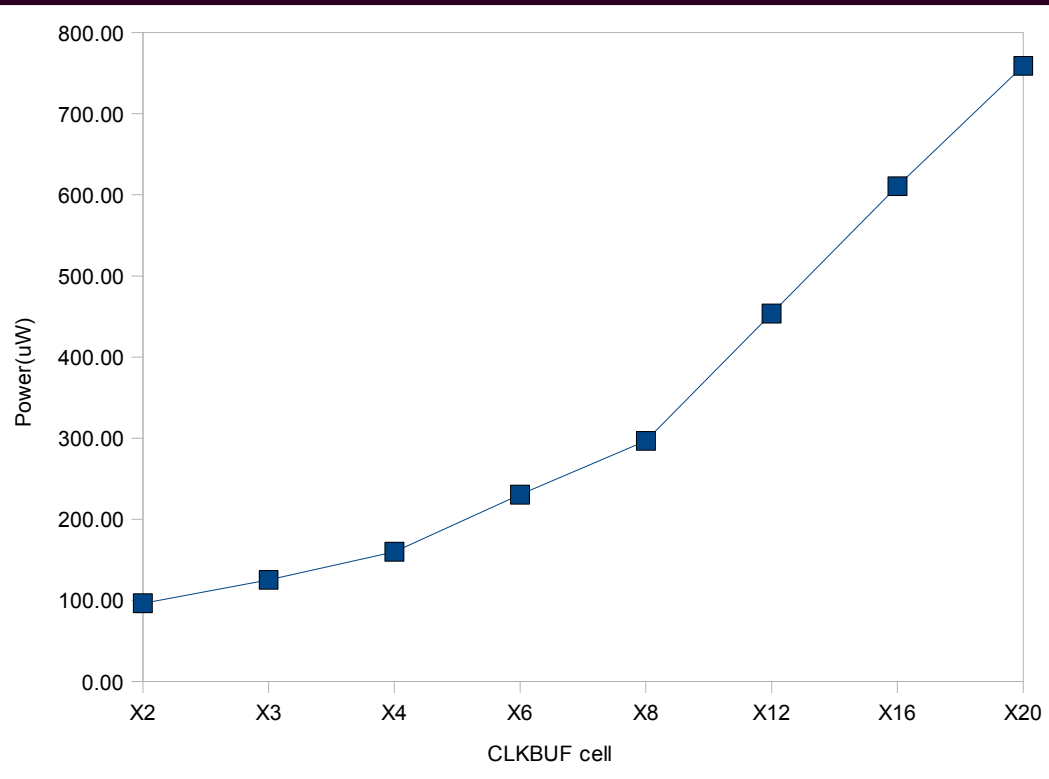
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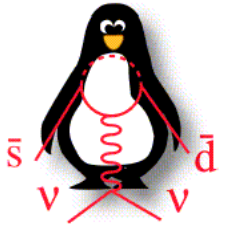
# Cell delays & power



Sezione di Torino



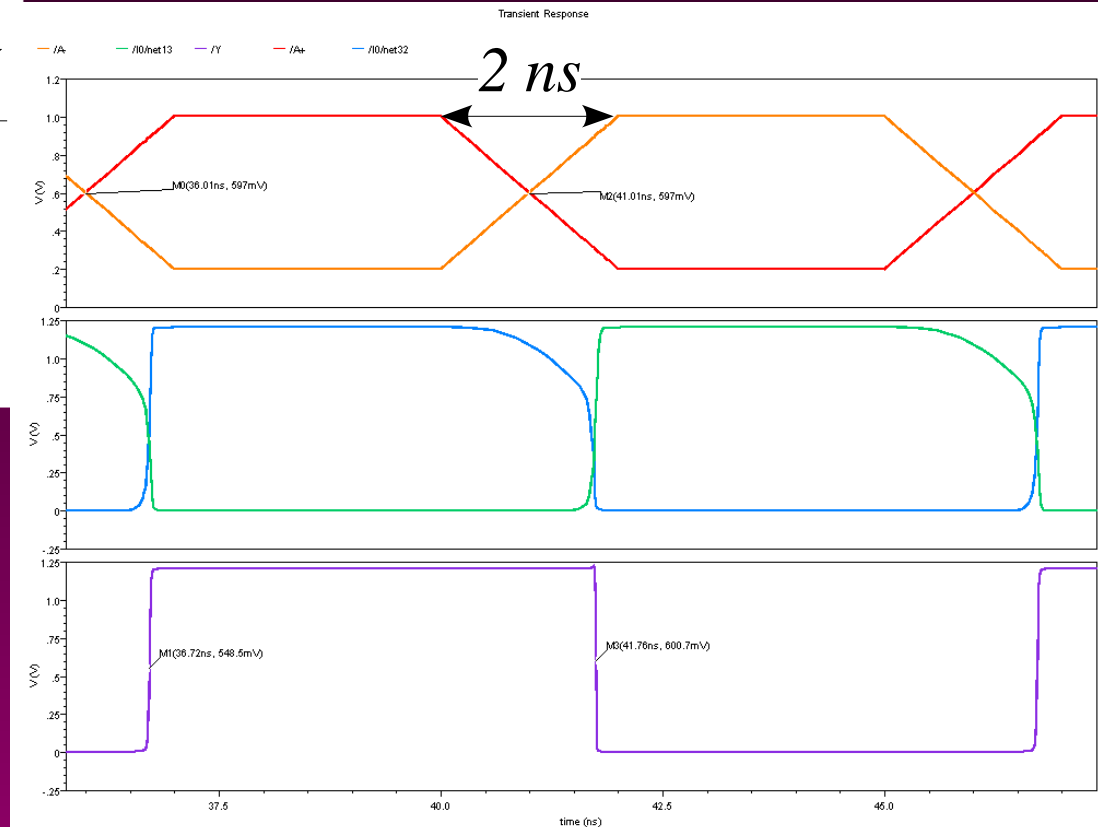
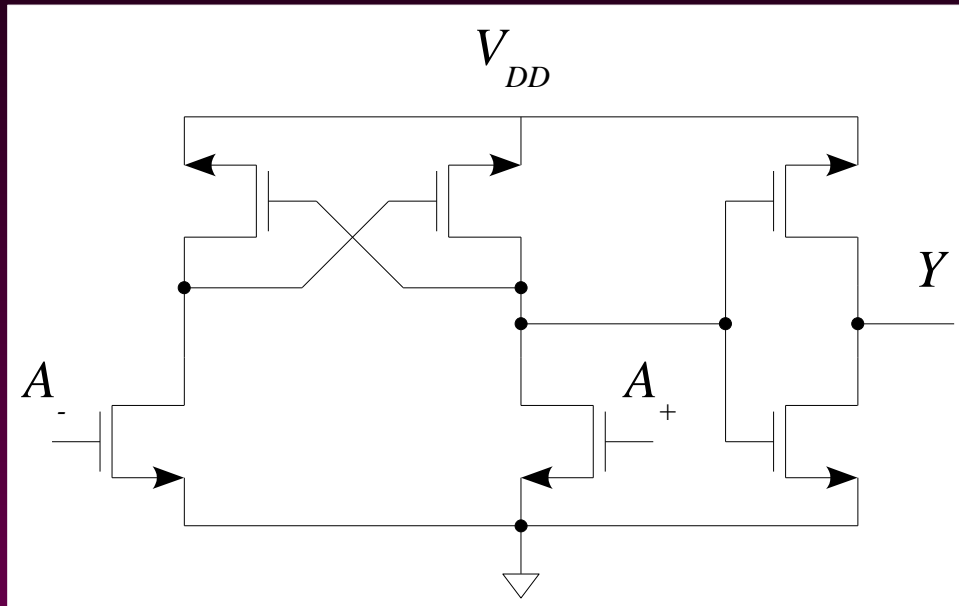
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# DCVSL receiver



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# Local I/O signals



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- i. pixel\_in : *from CFD*
- ii. start\_of\_conv : *capacitor discharge start*
- iii. end\_of\_conv : *capacitor discharge stop*
- iv. address\_in : *bus, 6 bits, hardwired*
- v. write\_ptr : *FIFO write pointer*
- vi. read\_ptr : *FIFO read pointer*
- vii. out\_enable : *3-state enable*



# Output signals



- i. address\_out ← *bus, 6 bits*
  - ii. coarse\_time ← *bus, 11 bits*
  - iii. fine\_time ← *bus, 8 bits*
  - iv. empty
- \* Pseudo differential lines with CMOS levels.
  - \* End of column sense amplifier to increase the speed



# OR-chained signals



- i. busy : pixel ready to be readout
  - ii. old : pixel with previous frame data
  - iii. token : token for readout enable
  - iv. SEU\_error : SEU\_error on registers or FSM
- \* Local signals are propagated down to the column by putting in OR the local and the previous pixel output



# Sense amplifier



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