Demo Read-out protocol

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Demo read-out protocol

- **Demonstrator data read-out protocol:**
- **inputs**
  - 1 read-out clock (LVDS) up to 320 MHz
  - 9 enable_readout (CMOS)
- **outputs**
  - 9 serial_out (LVDS)

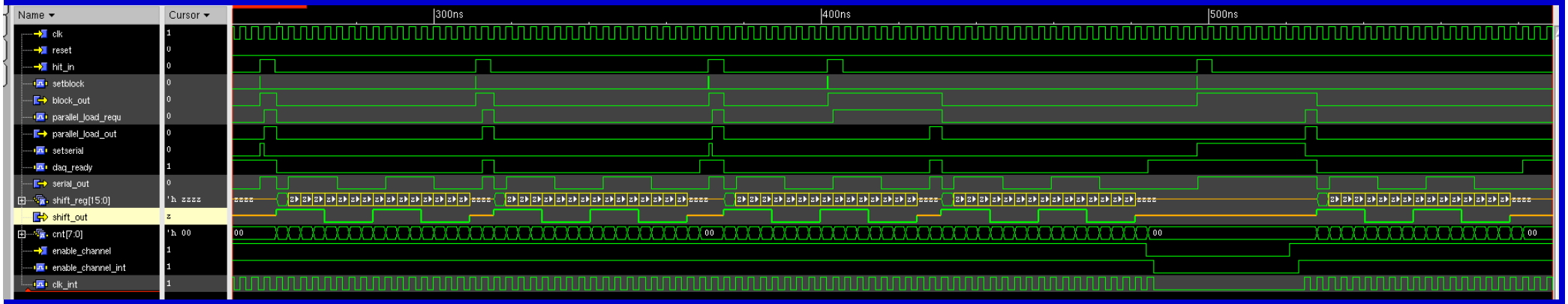
Demo read-out protocol

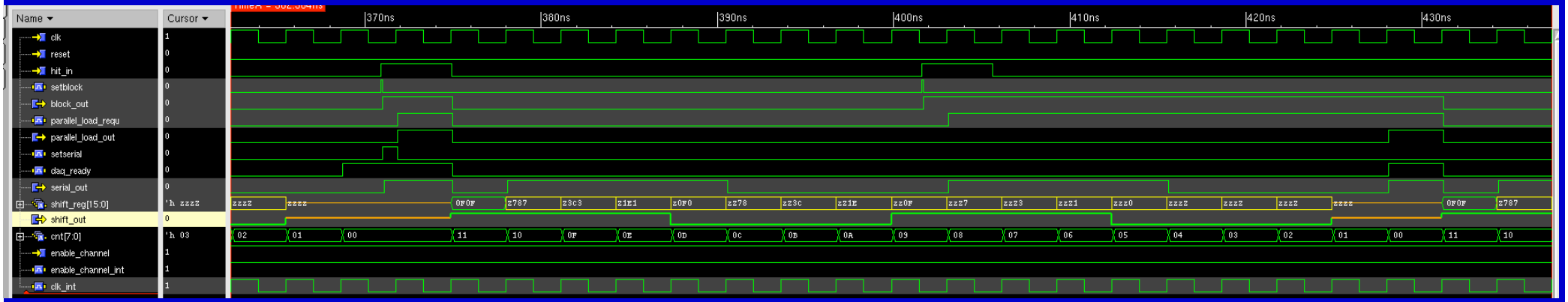
- **If enable_readout is ‘1’:**
  - if no hit is available in column
    - corresponding serial_out is ‘0’
  - if hit in column arrives corresponding serial_out
    - goes ‘1’ asynchronously
    - goes ‘1’ for one clock cycle
    - goes ‘0’ for one clock cycle
    - then 197 bits are shifted out
    - goes ‘0’ of no hit arrived in the meanwhile, otherwise restarts with goes ‘1 for one clock cycle

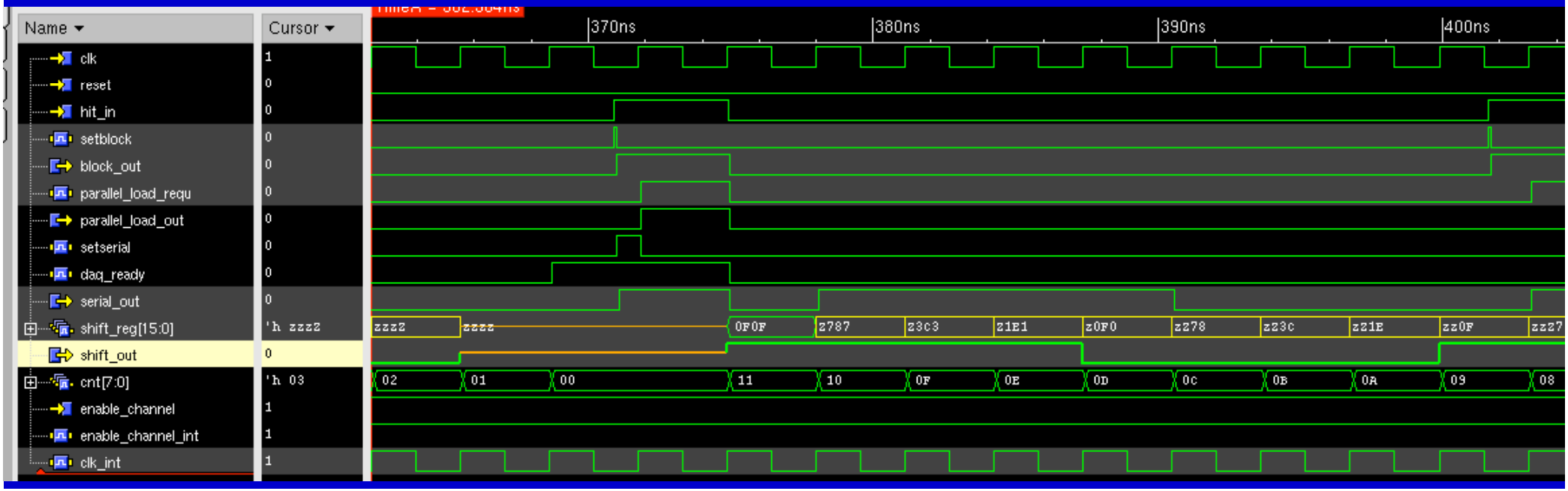
Demo read-out protocol

- **If enable_readout is ‘0’:**
  - if no hit is available in column
    - corresponding serial_out is ‘0’
  - if hit in column arrives corresponding serial_out
    - goes ‘1’ asynchronously and stays ‘1’ until enable_readout is ‘1’
    - goes ‘1’ for one clock cycle
    - goes ‘0’ for one clock cycle
    - then 197 bits are shifted out
    - goes ‘0’ of no hit arrived in the meanwhile, otherwise restarts with goes ‘1 for one clock cycle

- 197 bits are
  - 32 bits DLL data fine time leading edge
  - 32 bits DLL data fine time trailing edge
  - 32 bits coarse counter pos. clock edge leading edge
  - 32 bits coarse counter neg. clock edge leading edge
  - 32 bits coarse counter pos. clock edge trailing edge
  - 32 bits coarse counter neg. clock edge leading edge
  - 5 bit address
- running with 320 MHz -> 0.6 µs or 1.6 MHz


Name
Cursor
300ns
400ns
500ns
clk
reset
hit_in
setblock
block_out
parallel_load_requ
parallel_load_out
setserial
daq_ready
serial_out
shift_reg[15:0]
shift_out
cnt[7:0]
enable_channel
enable_channel_int
clk_int


Name
Cursor
370ns
380ns
390ns
400ns
410ns
420ns
430ns
clk
reset
hit_in
setblock
block_out
parallel_load_requ
parallel_load_out
setserial
daq_ready
serial_out
shift_reg[15:0]
'h zzz2
shift_out
cnt[7:0]
'h 03
enable_channel
enable_channel_int
clk_int


Name
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370ns
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400ns
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setblock
block_out
parallel_load_requ
parallel_load_out
setserial
daq_ready
serial_out
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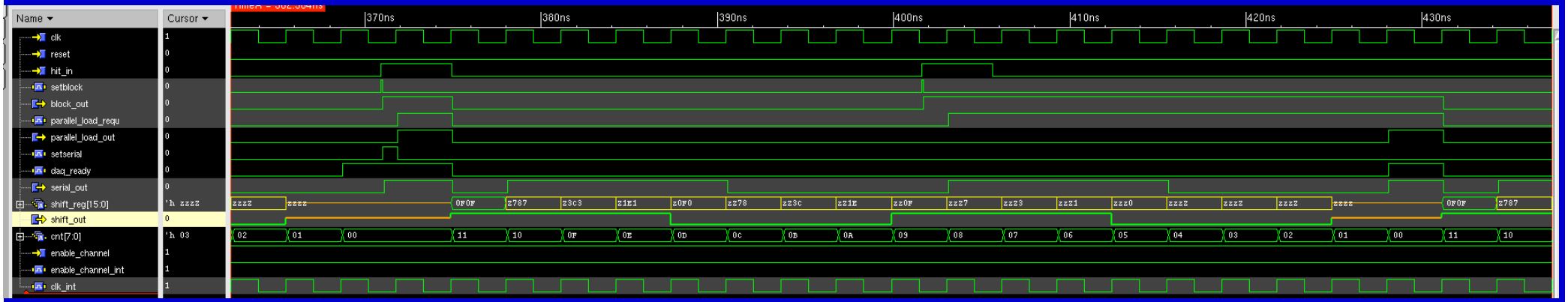
'h zzz2
shift_out
cnt[7:0]
'h 03
enable_channel
enable_channel_int
clk_int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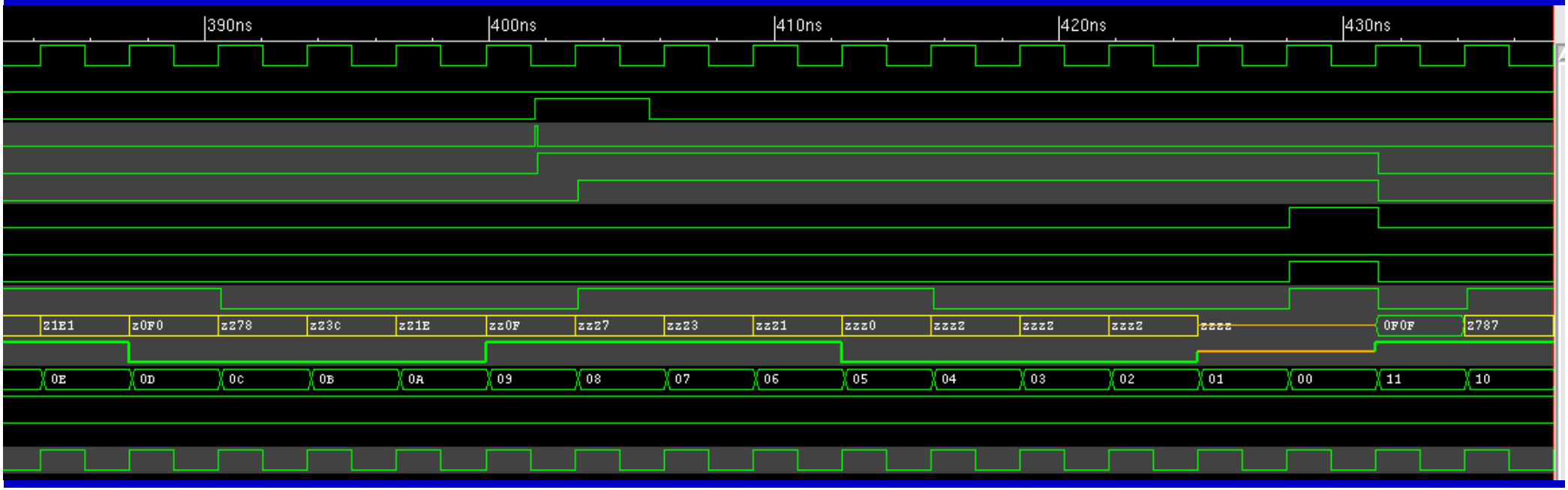
enable_channel
enable_channel_int
clk_int
'h zzz2
'h 03
zzz2 zzzz 0F0F z787 z3c3 z1E1 z0F0 z278 z23c z21E z0F zz27 zz23 zz21 zzz0 zzz2 zzz2 zzz2 zzzz 0F0F z787
02 01 00 11 10 0F 0E 0D 0c 0B 0A 09 08 07 06 05 04 03 02 01 00 11 10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0E 0D 0c 0B 0A 09 08 07 06 05 04 03 02 01 00 11 10