Gigatracker Demostrator Design review

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Scope

- System introduction
- Specifications
- Design options

27-60 Beam size & pixel matrix

- Beam geometry size -> 27 x 60 mm
- 3 stations: each 5 x 2 ASICs + 1 sensor
- Active pixel matrix size per chip: 13.5 x 12 mm
- 45 rows x 40 columns = 1800 pixels
- Each pixel 300 µm x 300 µm
- Time stamping: < 200 ps rms in one station

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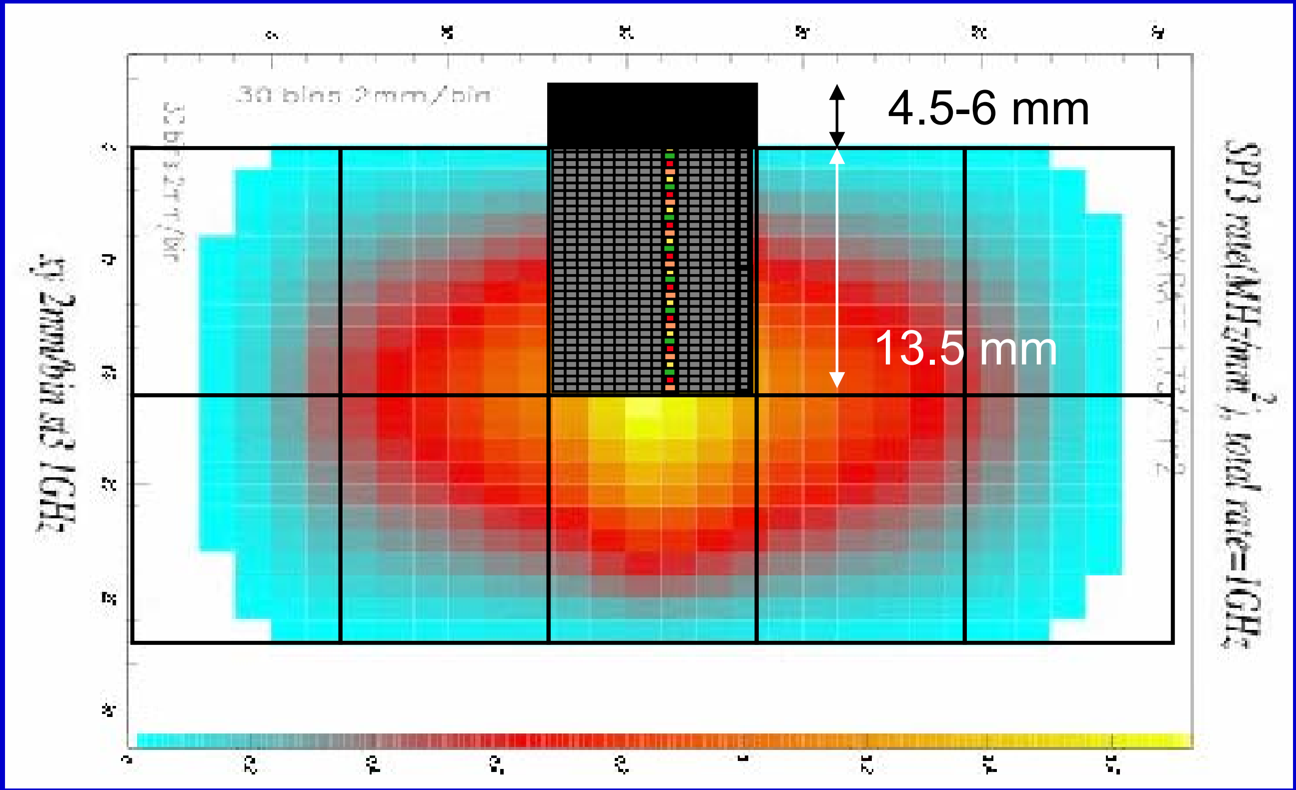
Configuration

60 mm



27 mm

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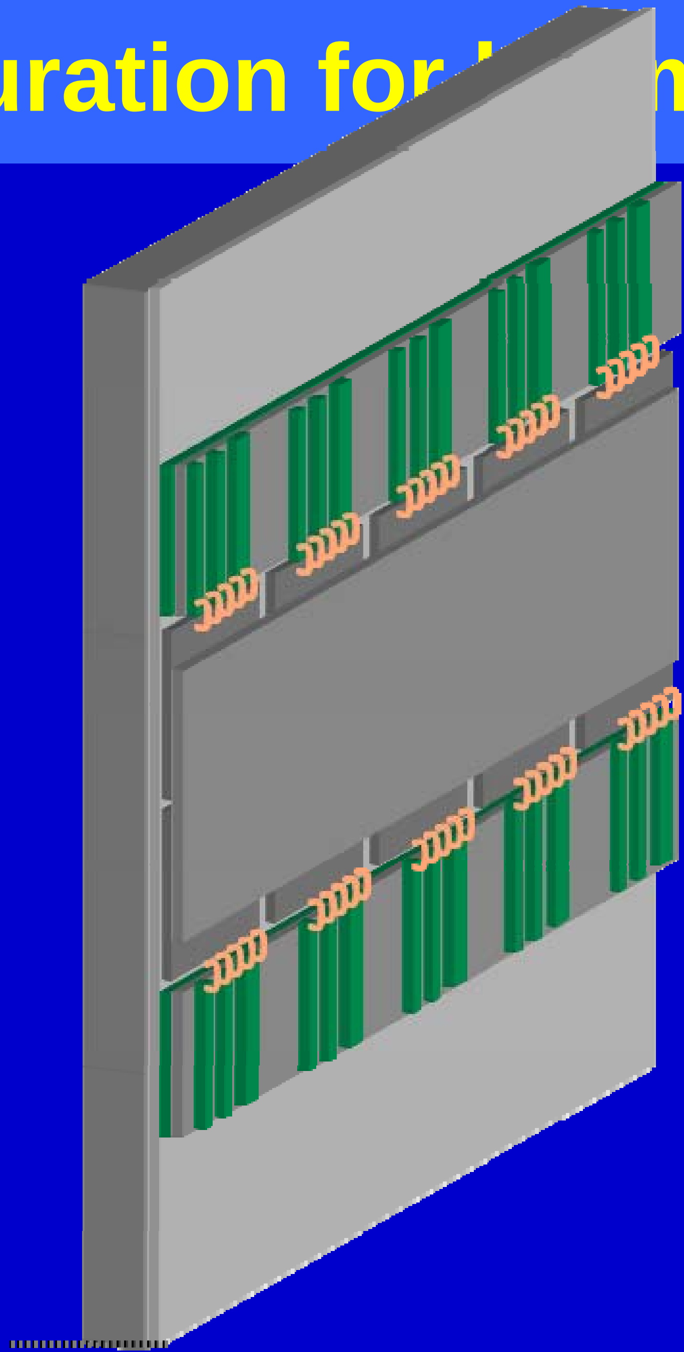
Configuration for … m 27-60



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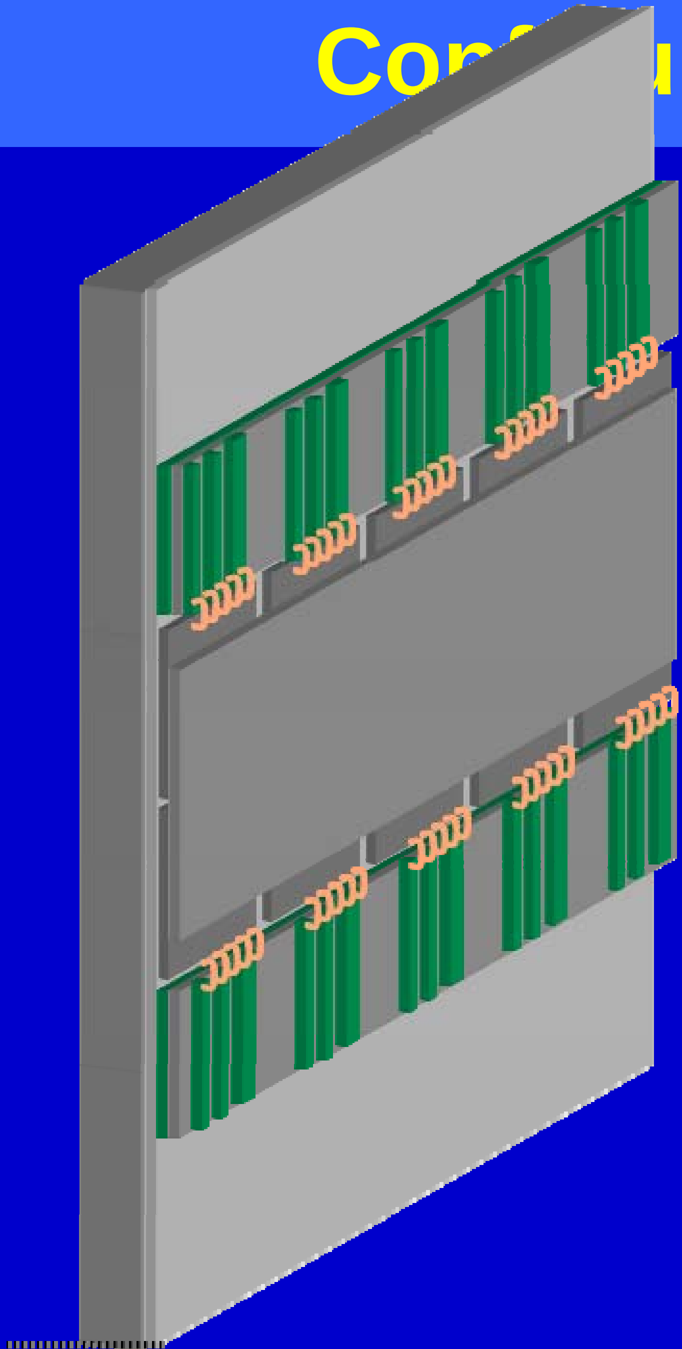
Configuration for beam 27-60



- **Sensor&bonds: 0.24% X_0 (200 µm Silicon)**
- **RO chip: 0.11% X_0 (100 µm Silicon)**
- **Structure: 0.10% X_0 (100 µm Carbon fiber)**
- **Total: 0.45% X_0 uniform**

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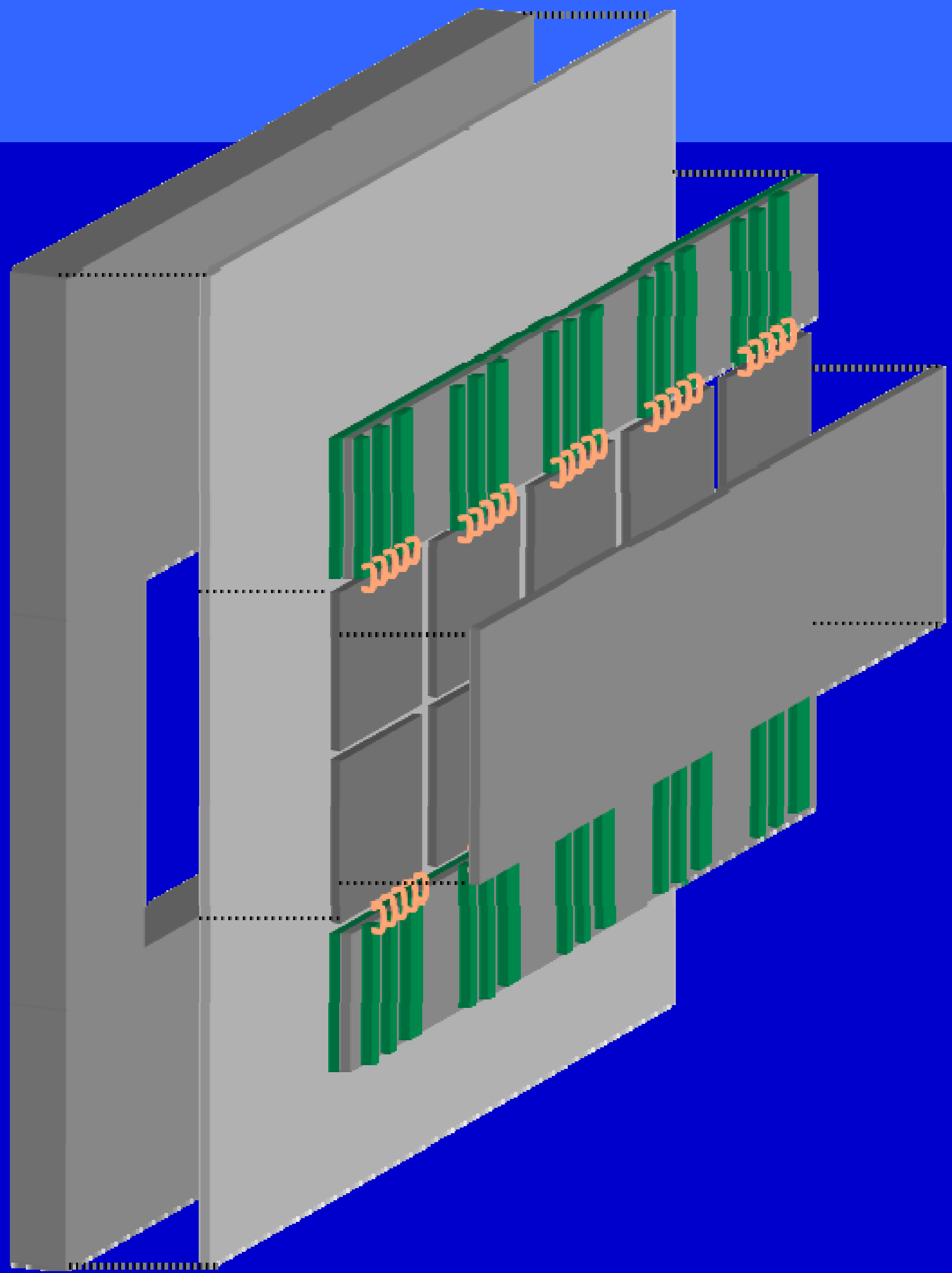

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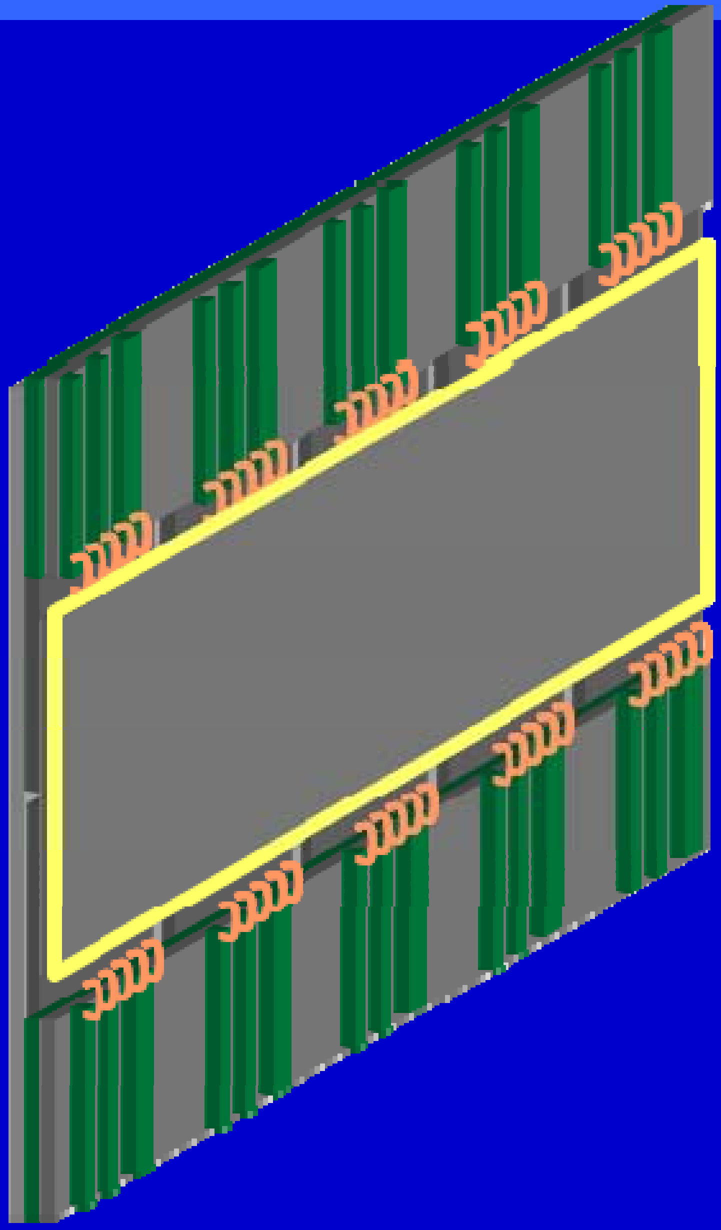
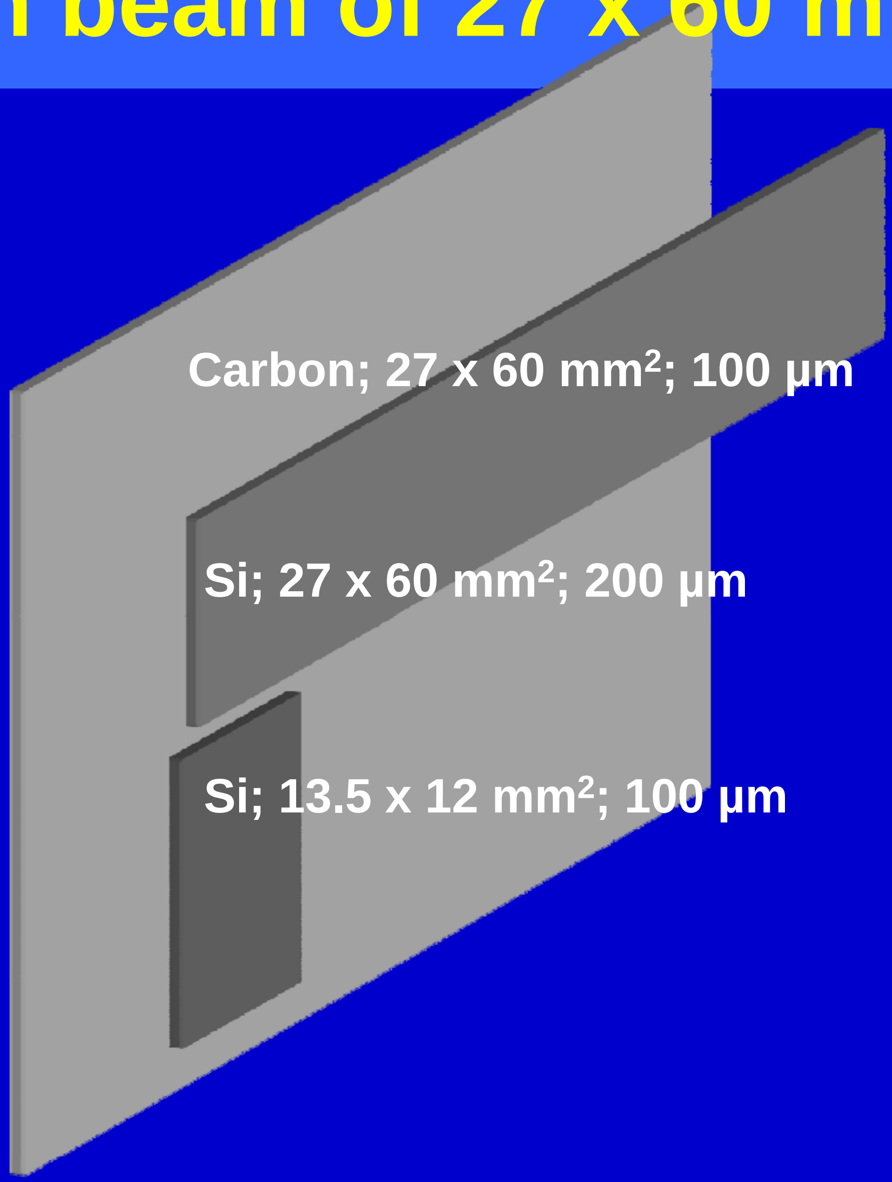
Components in beam of 27 x 60 mm





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General: System Specifications

Number of stations	3
Number of pixels per station	18000
Active area per station	60 mm x 27 mm = 1620 mm^2
Number of chips per station	2 rows x 5 columns
Number of pixels per chip	1800
Rows and columns on chip	45 x 40
Size of pixels	300 µm x 300 µm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
Time resolution of GTK	150 ps (rms)
Time resolution of one station	< 200 ps (rms)
Chip design time resolution	100 ps (rms)

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General: System Specifications

Size of active sensor area	60 mm x 27 mm = 1620 mm^2
Thickness of sensor	200 µm
Type of sensor	p in n
Thickness of read-out chip	100 µm
Dynamic input range	5000 – 60000 electrons
Particle rate per station	800 MHz
Average particle intensity per station	0.5 MHz/mm^2
Design particle rate per chip	130 MHz
Rate of center pixel	140 kHz
Rate of center column	~ 3.3 MHz or 0.82 MHz/mm^2
Average rate per pixel	73 kHz

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General: System Specifications

Number of trigger levels	1
Latency	> 1 µs up to 1 ms
Trigger window	≥ 10 ns
Maximum dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	~ 10^5 Gy
Neutron flux in 100 days	2×10^{14} 1 MeV neutron equivalent cm^{-2}
Material budget	0.5 % X_0 per station
Power dissipation per station	≤ 2 W/cm^2, 32 W
Operating temperature per station	< 0 ºC

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Chip size/data rate

- **Rate of center column = chip design rate:**

  3.3 MHz/column
  3.3 MHz/(1.35 cm * 0.03 cm)
  ~ 82 MHz/cm^2

  – => avg rate 73 kHz/pixel
  – => 132 MHz/chip
  – => 132 MHz/chip * ~ 32 bit = ~4.2 Gbit/s
  – => max rate in beam center 140 kHz/pixel

  – Example data word (11 bit address, 5 bit fine time, (5 bit fine time trailing), 11 bit coarse time)

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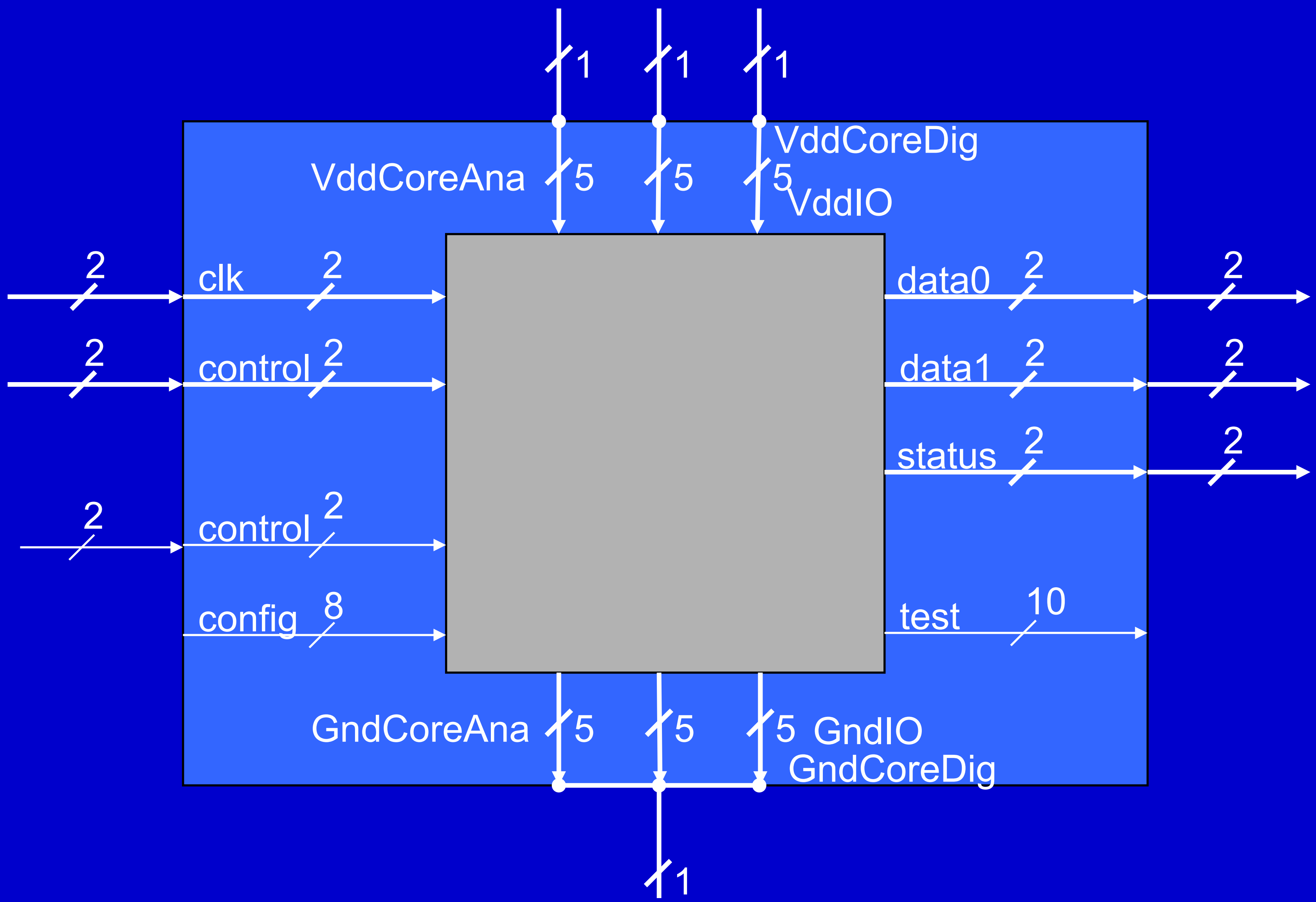
I/O block diagram of chip



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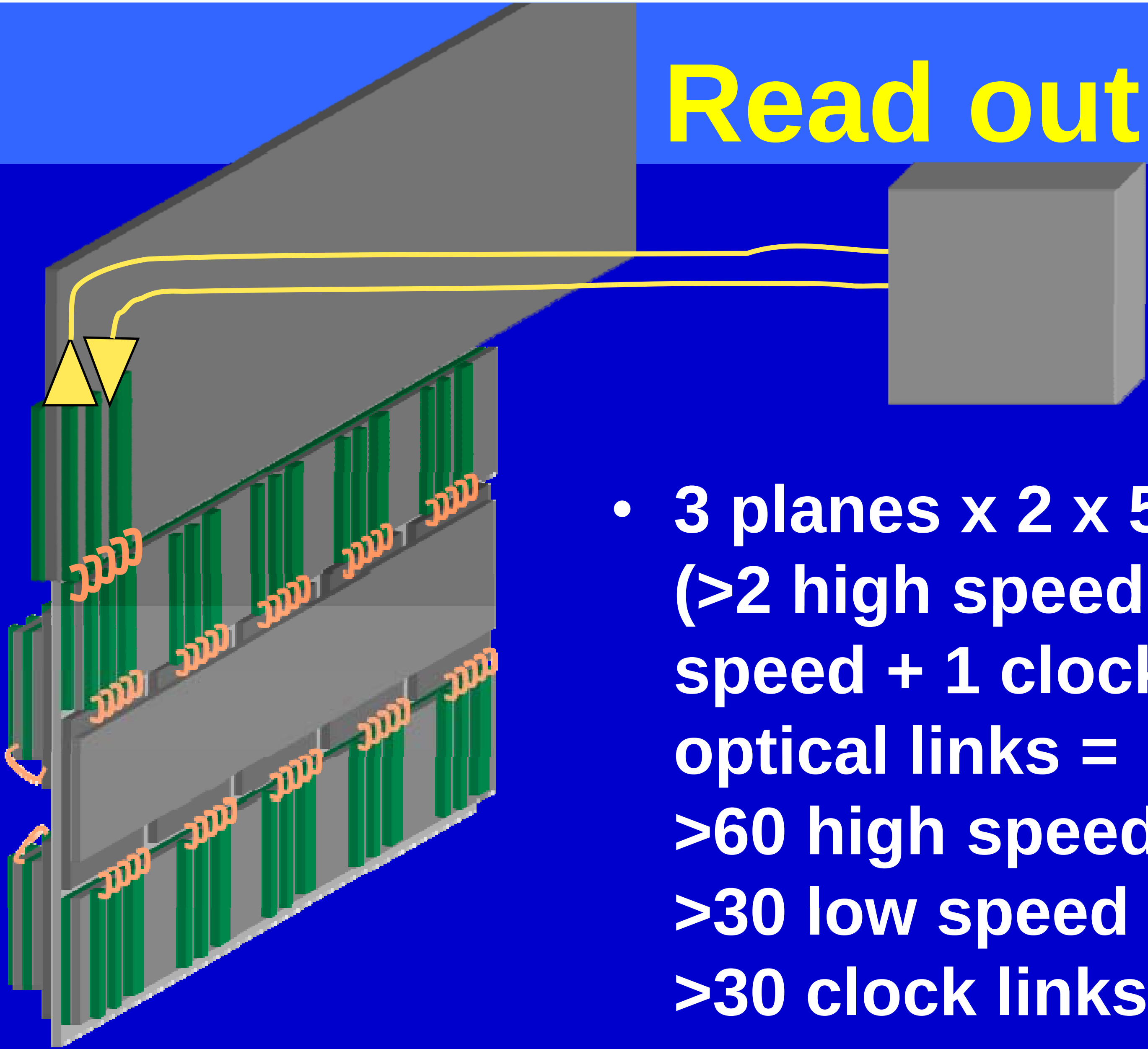
Read out



- 3 planes x 2 x 5 chips x (>2 high speed + >1 low speed + 1 clock) optical links =
  >60 high speed links +
  >30 low speed links+
  >30 clock links
- On-detector is trigger-less

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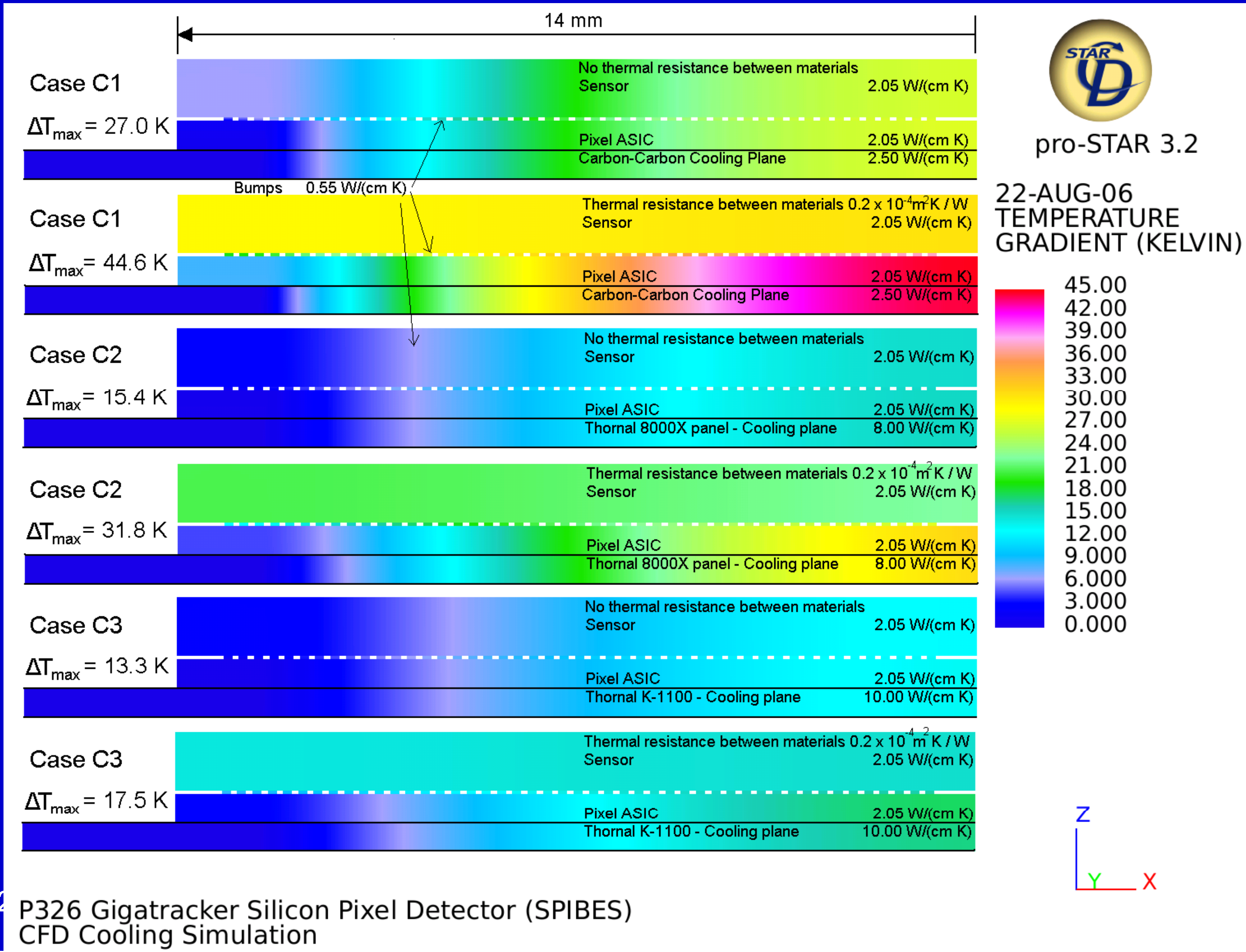
Thermal drop: ideal contact between materials (Thomas Kuhn)

https://edms.cern.ch/document/761753/1



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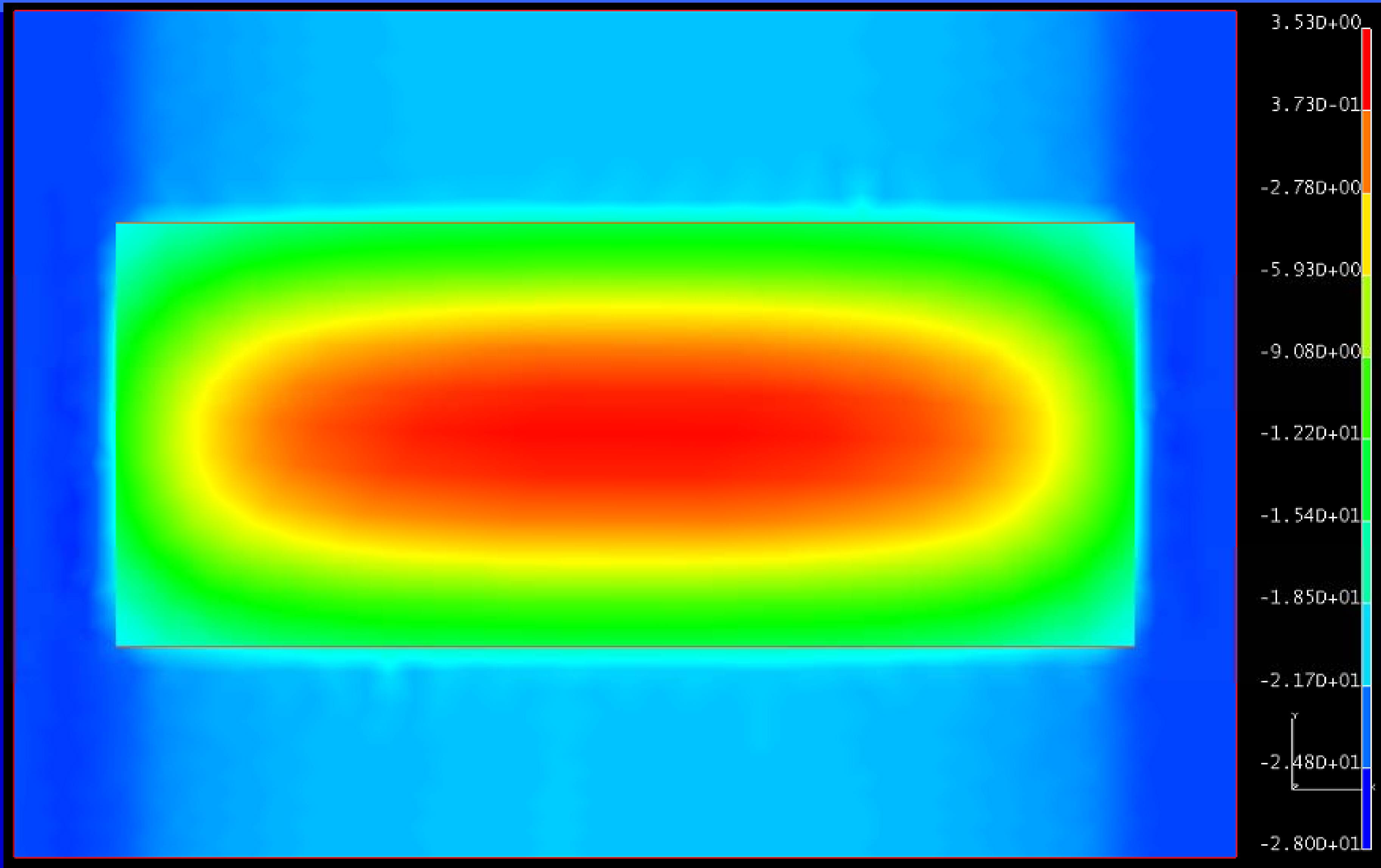
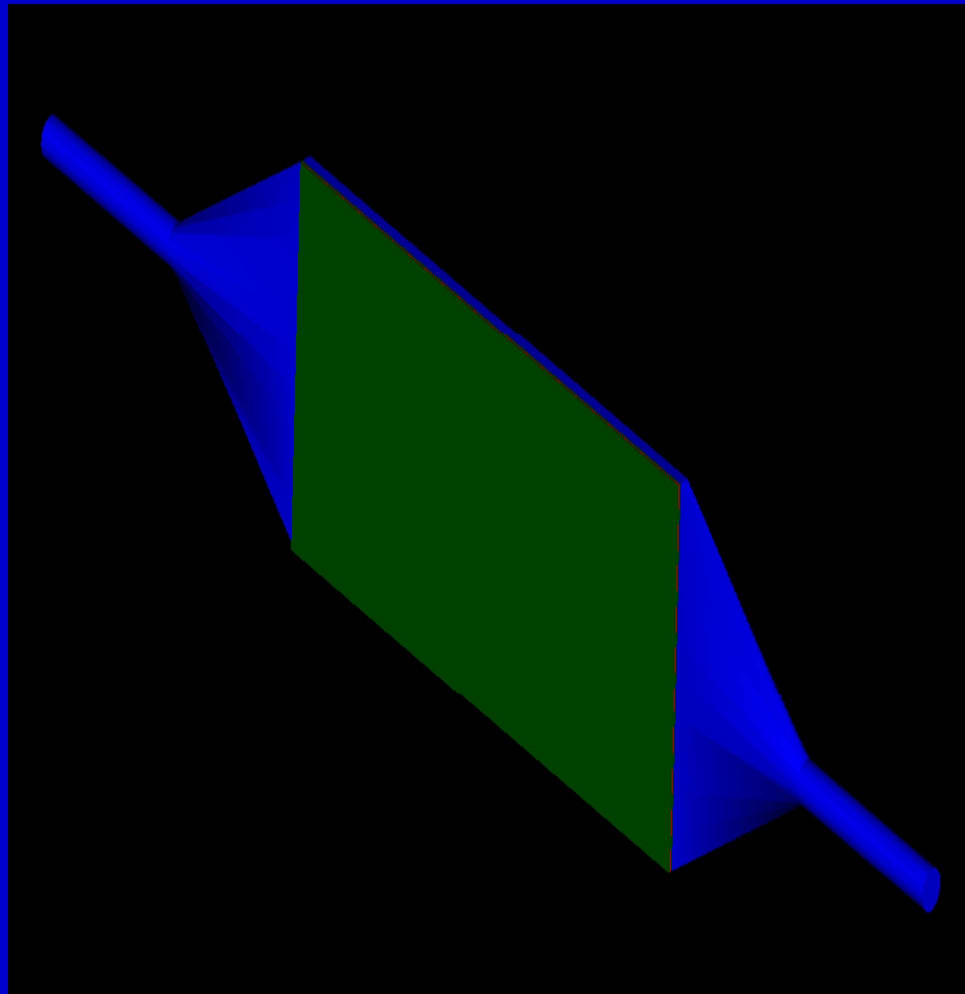
CONFIGURATION 1 – TEMPERATURE DISTRIBUTION



CONFIGURATION 2 – COOLING ANALISYS

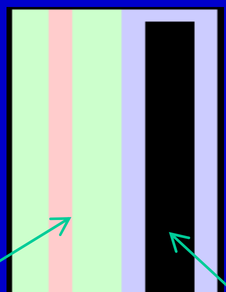
COOLING FLUID : NITROGEN		K	°C
Delivery temperature	Ti	100	-173
Wall temperature	Tw	273	0
Mean temperature	Tm = (Ti + Tw)/2	186,5	-86,5

NITROGEN PROPERTIES @ Tm and atmospheric pressure		
Specific weight (Kg/m^3)	ρ	1,79
Specific heat (J/KgK)	Cp	1041
Thermal conductivity (W/mK)	λ	0,024
Kinematic viscisity (m^2/s)	v	1,34E-05



GENERATED POWER (W)
Q = q x A = (2E+04) x (27E-03 x 60E-03) = 32,4

COOLING CIRCUIT SURFACE (m^2)
S = 27E-03 x 60E-03 = 1,62E-03



Vittore Carassiti - INFN FE

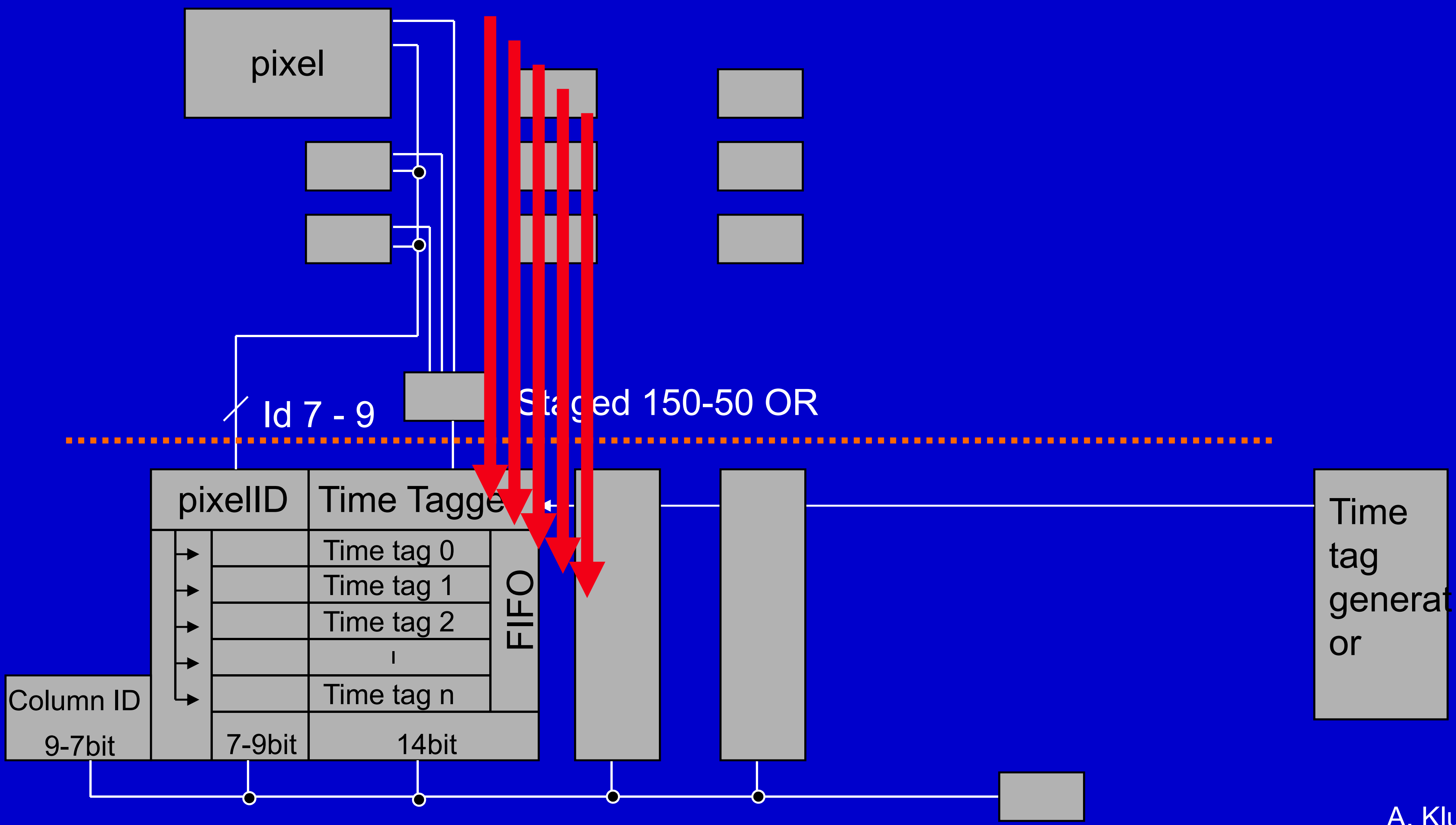
MAX dT (°C) (sensors side)	conf 1 23,5	conf 20,2

General architecture

- Small signal, time walk <-> timing precision
  Low noise <-> digital electronics, high data rate

- Pixel segmentation
  Efficiency <-> dead time

Precise pixel signal to TDC



Precise pixel signal to TDC

- Many low jitter signals are routed over the chip and over pixel cells
  to central high frequency time tag TDC
- Long low jitter signal lines
- Digital electronics in periphery
  Noise separation, SEU

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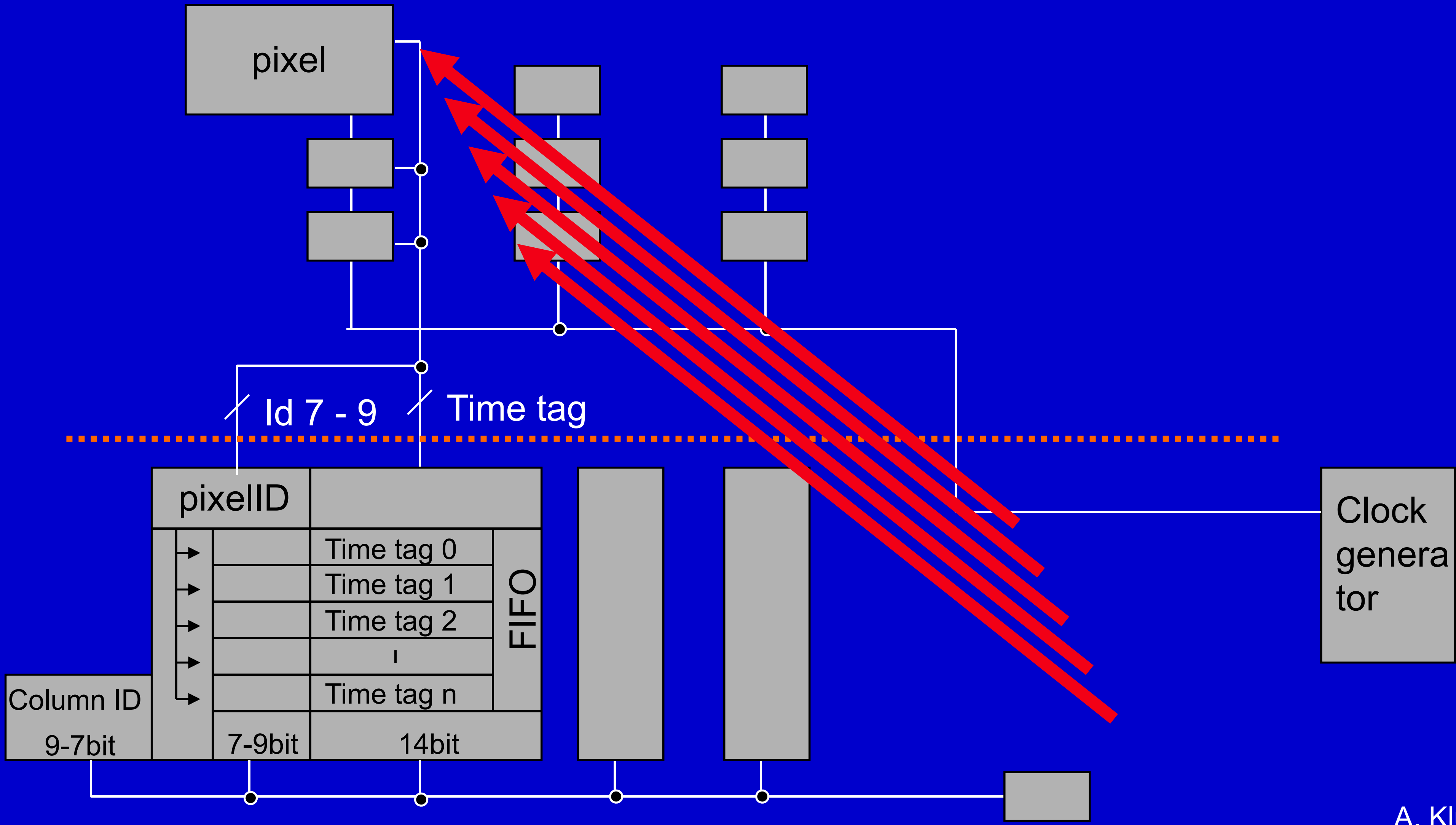
TDC in pixel cell



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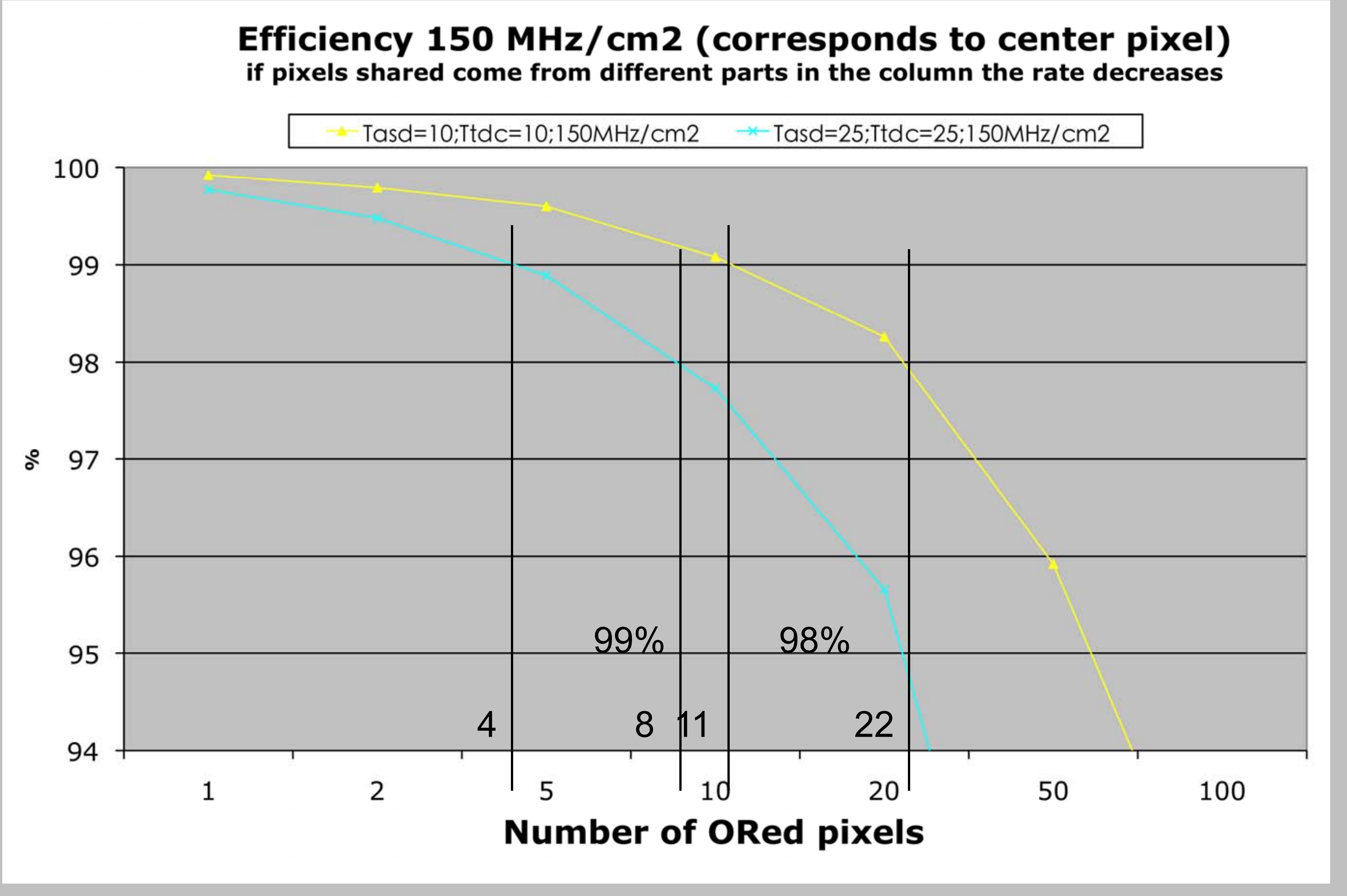
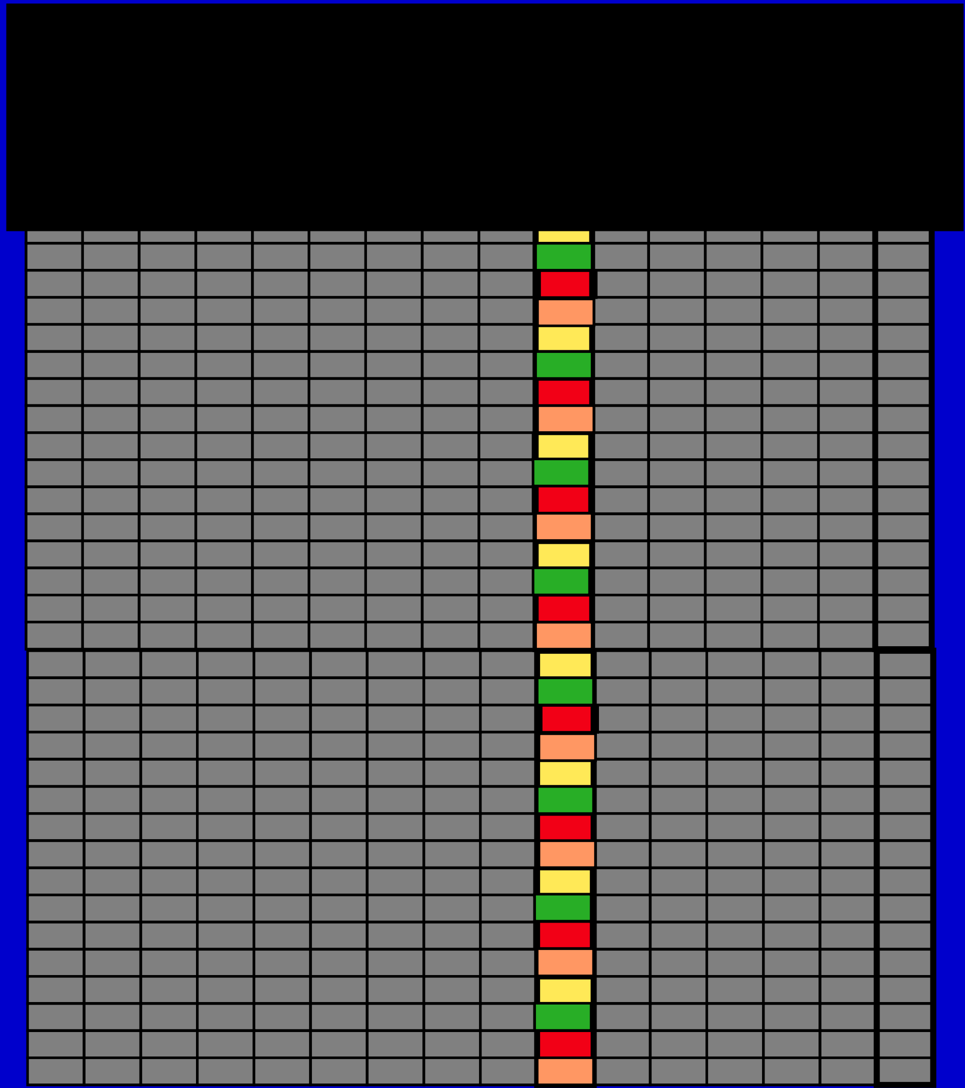
TDC in pixel cell

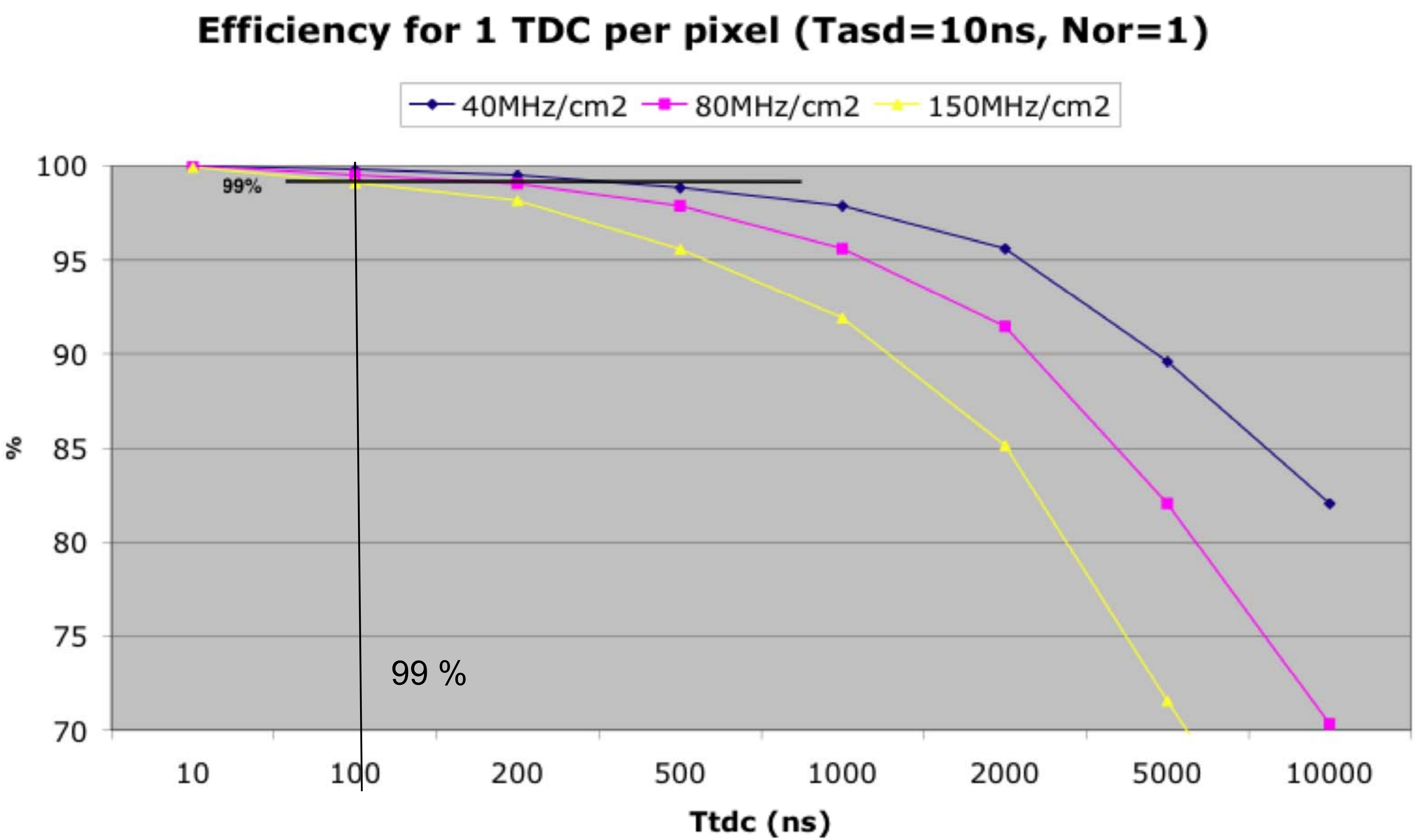
- Low jitter reference clock routed to each pixel cell on entire chip.
- Activity in pixel cell.
- Radiation

Pixel segmentation



Rate sharing along a column





Efficiency for 1 TDC per pixel (Tasd=10ns, Nor=1)
40MHz/cm2
80MHz/cm2
150MHz/cm2
100
95
90
85
80
75
70
%
99%
99 %
10
100
200
500
1000
2000
5000
10000
Ttdc (ns)

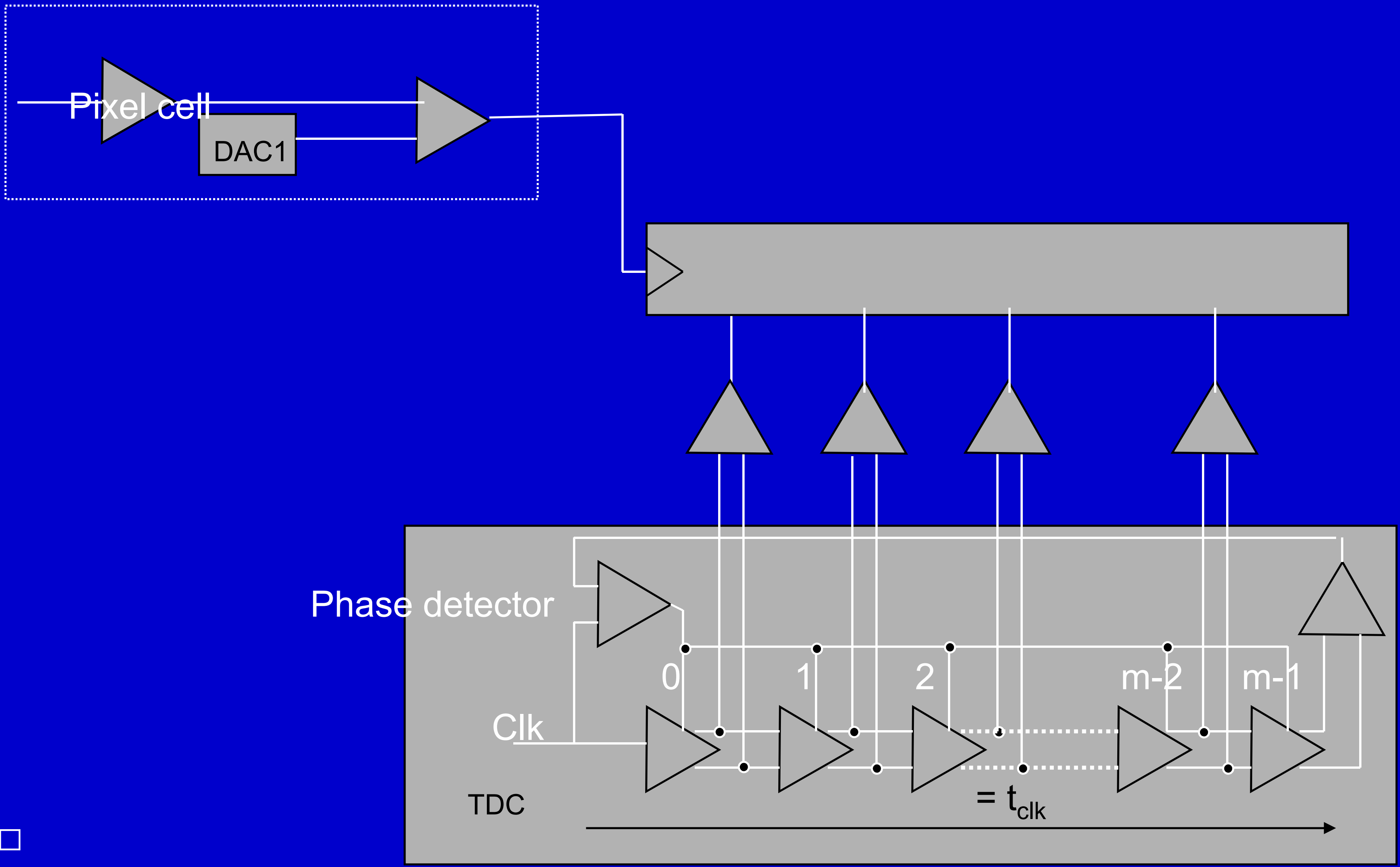
Question

- How can we find a solution which allows to:
- provide timing resolution, sufficient low noise and high data rate

Design options

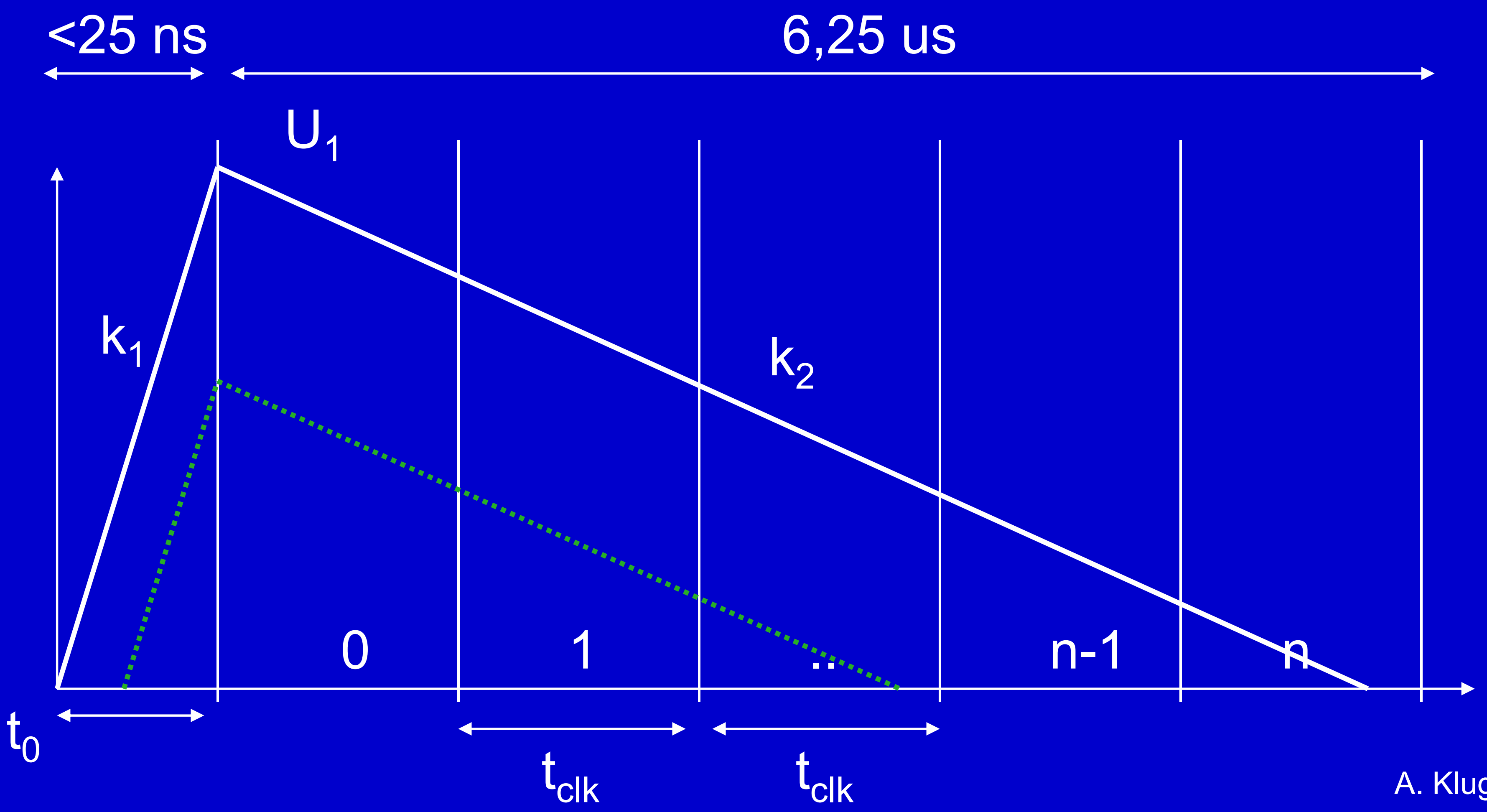
- **Amplifier, Discriminator, time walk compensation:**
  – CFD,
  – TOT
- **TDC**
  – Wilkinson (TDC per pixel)
  – DLL (TDC in end of column)

HPTDC principle



TDC (Wilkinson-dual slope)

$T_0 = n\ T_{clk}\ k_2\ /\ k_1$



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Demonstrator

- **needs to answer at least following questions:**
  – Can we provide a time resolution of 100 ps rms?
  – Is this also true when we read-out the data?
  – Is front-end robust enough?
  – Is noise separation between analog and digital good enough?
- **What do we need to measure and how?**

Conclusion

- Specifications
- Design options and why?