Overview of the EOC architecture

EOC architecture, Bus system,
Low swing signaling, cross-coupled lines, noise
SNR, TOT discriminator,
TDC, readout

Motivation to develop EOC architecture

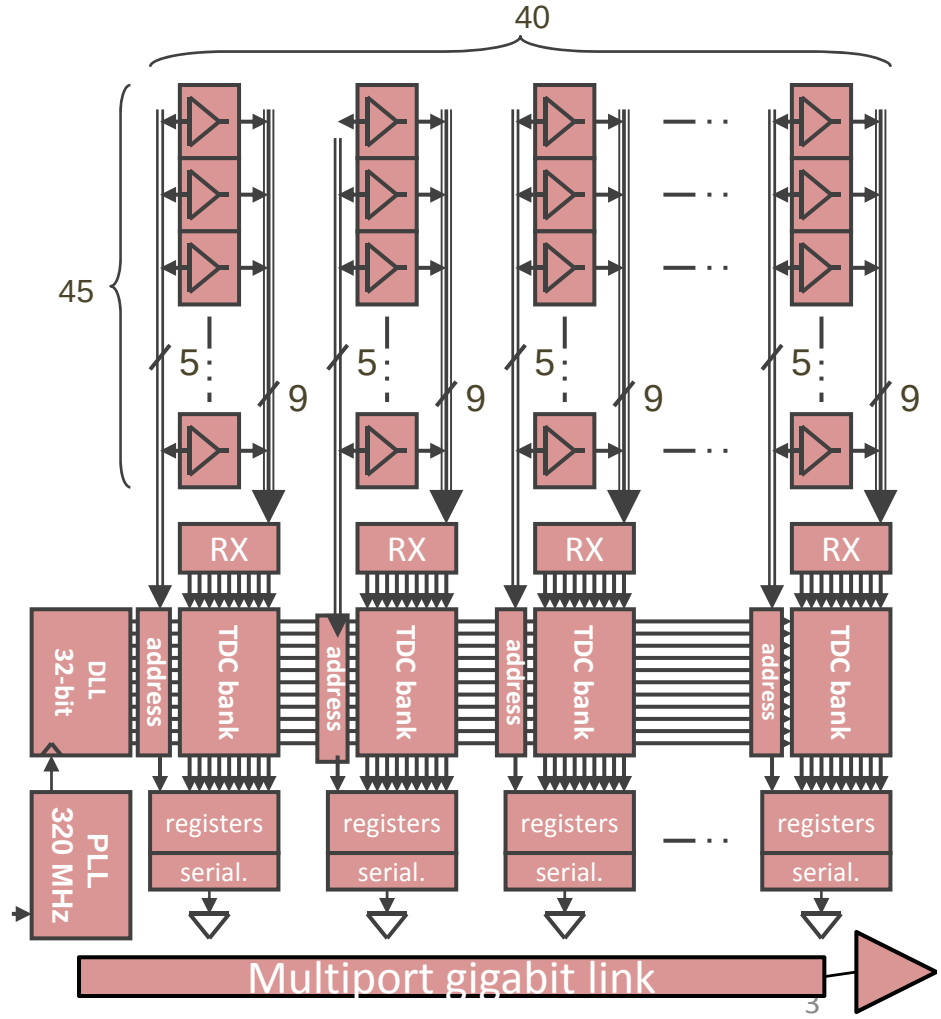
- Minimize digital noise in the pixel area
  - Why?
    - Severe risk of coupling between analog/digital in GHz domain
      - Exist already in working pixel detectors
    - Asynchronous hit events with readout clock makes noise rejection tougher than LHC pixel
      - Simultaneous read/write
    - No hit data reduction
      - All hits are readout making no difference between on-pixel and off-pixel processing
  - Precautions taken in the EOC ASIC
    - No digital circuits in the active beam area,
    - No clock “ “ “
    - Push all digital circuits in the end of column TDC circuits only
    - Bus system using differential current drive and very low voltage swing 15 mV at the far end TDC end of column circuit
    - Use a TOT discriminator having a smaller analog bandwidth than a CFD stage
      - But a larger digital bandwidth if no time walk calculation is done on-chip
- Profit from the existing TDC development in 130 nm
  - TDC in the end of column bank is a 100 ps version of Christian ‘s design

Overall EOC-TDC architecture

EOC architecture

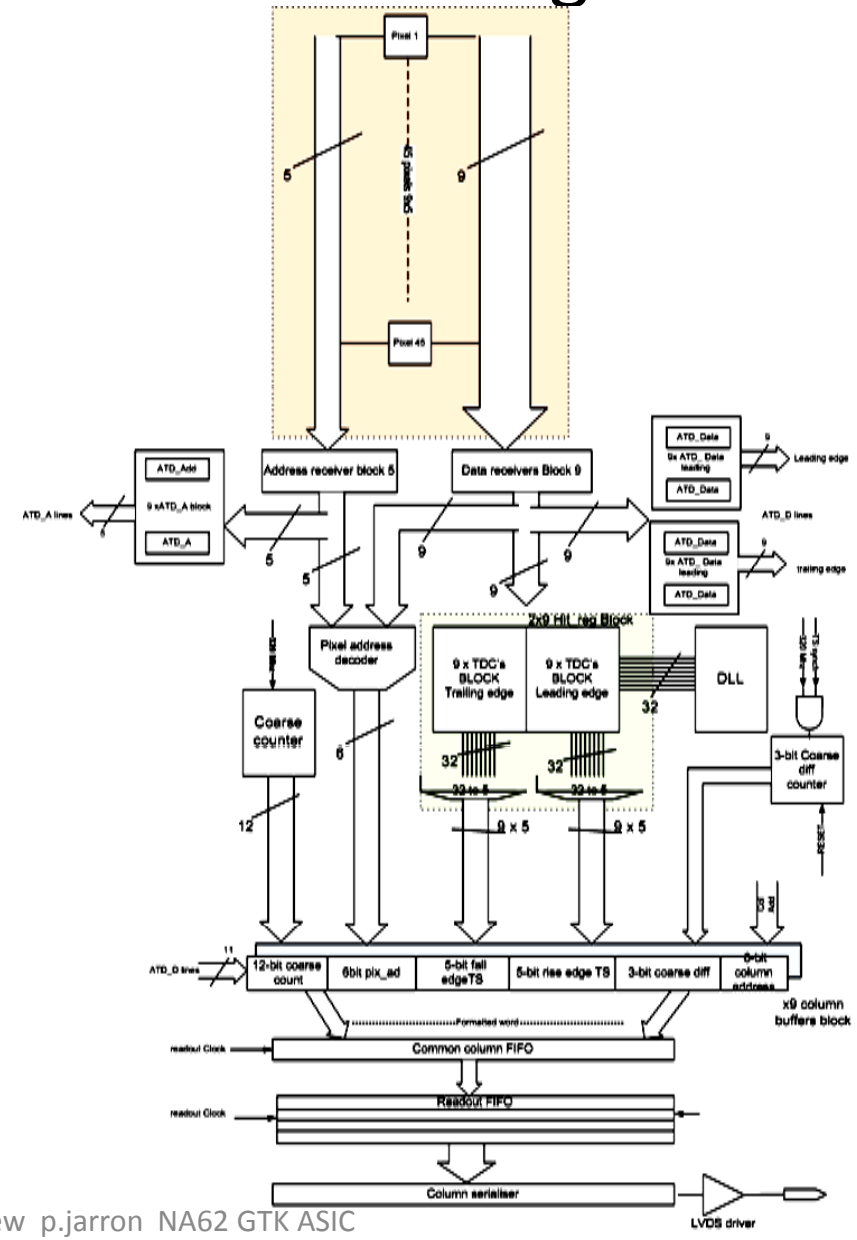
- No digital processing in pixel
- TDC, Time stamping and data pipelining in end of column
- DLL based digital TDC
- Time walk correction by a time over threshold discriminator
- Column pixel addresses encoded with a 5 x 9 matrix
- Bus system using cross coupled transmission lines, low current swing signal , with pre-emphasis for dispersive loss compensation

40 columns of 14 lines/45 pixels



EOC column circuit

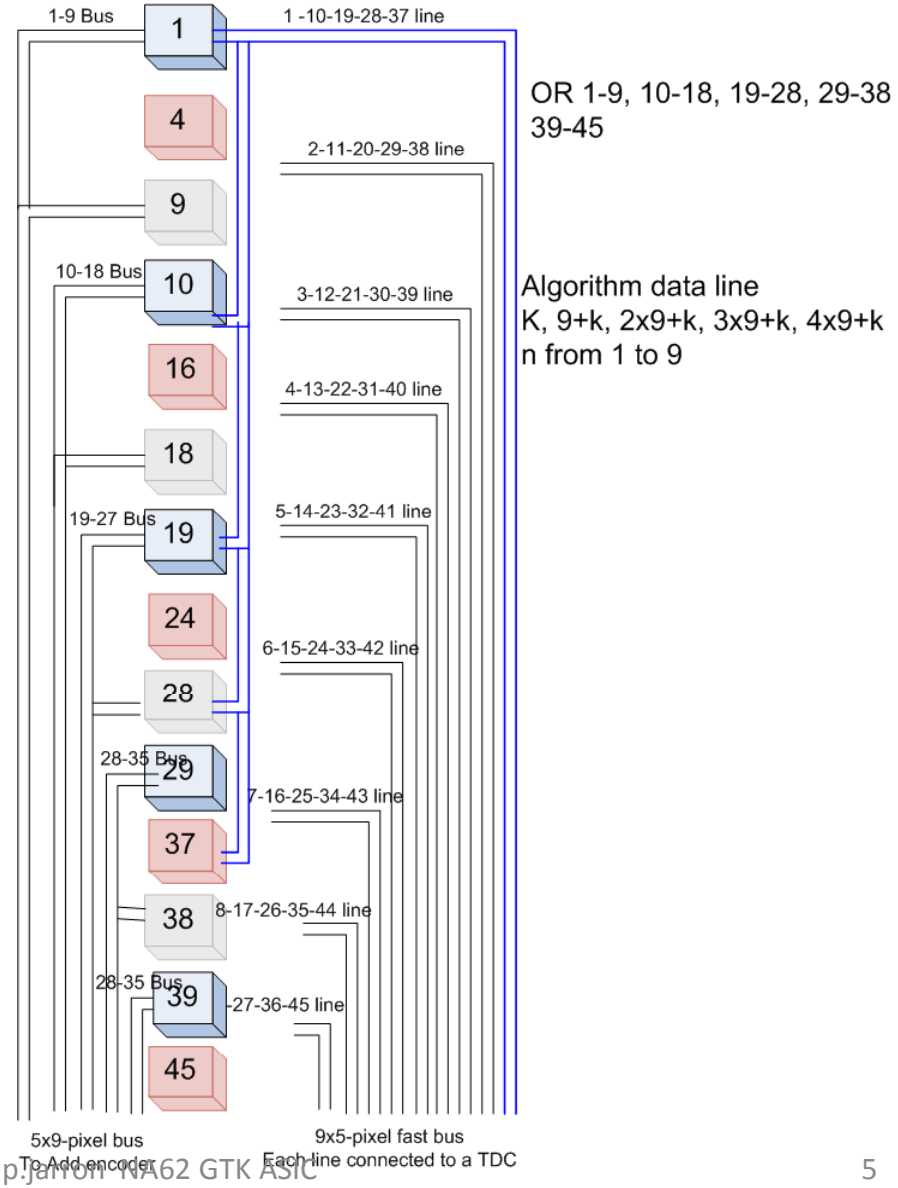
- Column block diagram



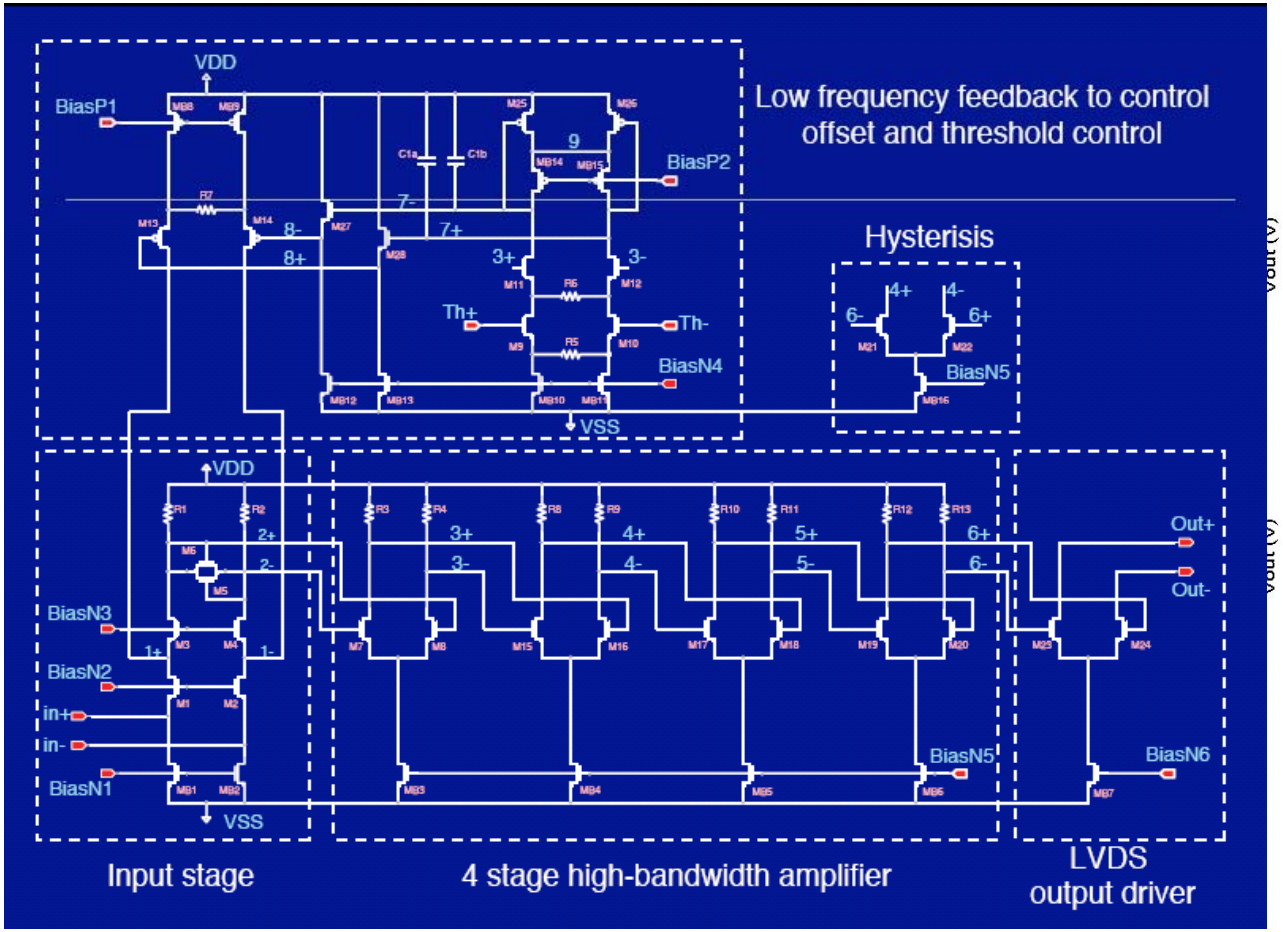
Bus system architecture

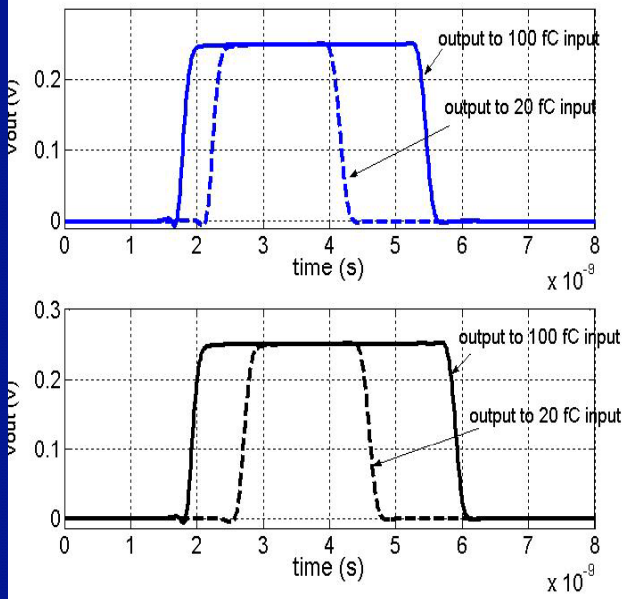
Encoding pixel address

1. Pixel address is encoded by a 5x9 networked bus
2. Decreases the number of TDC from 45 to 9, factor 5 smaller
3. 1800 double-TDC bank to 360 double TDC
4. The only issue is the pile up on data line
5. No problem of pile up for address line



NINO circuit TOT discri



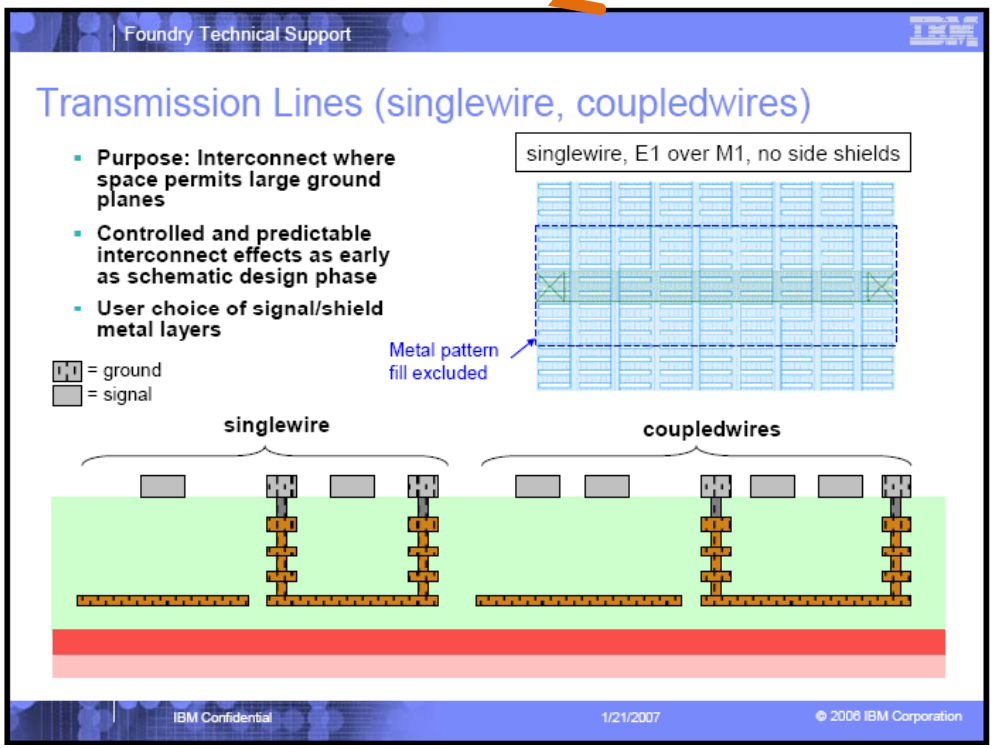


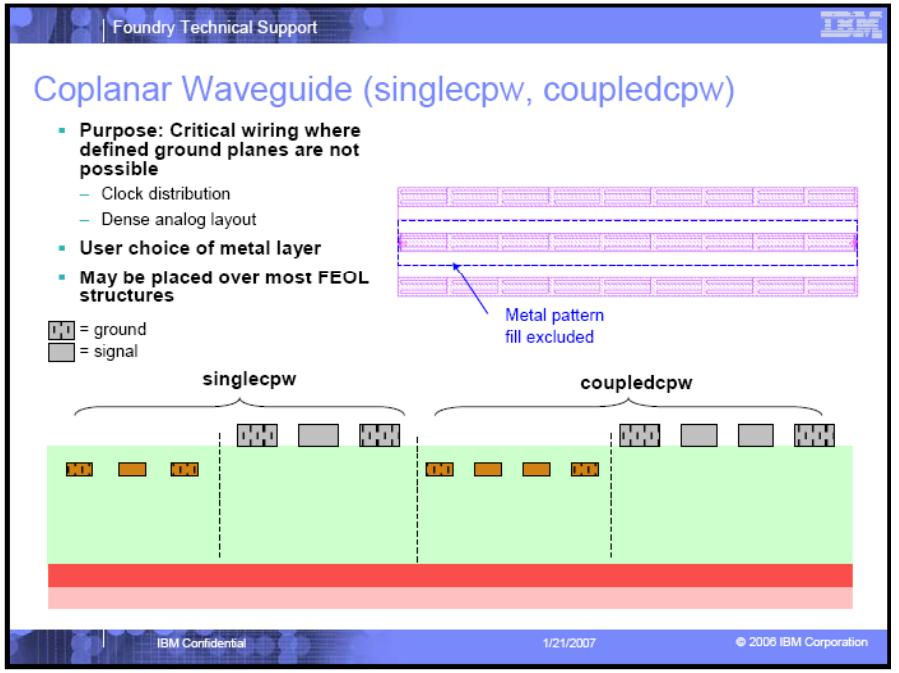
Cross-coupled waveguide

- 14.0.
- Shielded Transmission Line Interconnect Models. The current design kit release includes models for the following topologies:
  - " Straight single wire shielded transmission line, thereafter referred to as SINGLEWIRE.
  - " Two straight wires shielded transmission line, thereafter referred to as COUPLEDWIRE.
  - " Straight single wire coplanar waveguide, thereafter referred to as SINGLECPW.
  - " Two straight wires coplanar waveguide, thereafter referred to as COUPLEDCPW.
- Note: All interconnect models included in the current release are symmetrical and supported for both MA and LM CMRF8SF BEOL metal options.

Transmission line IBM models and layout

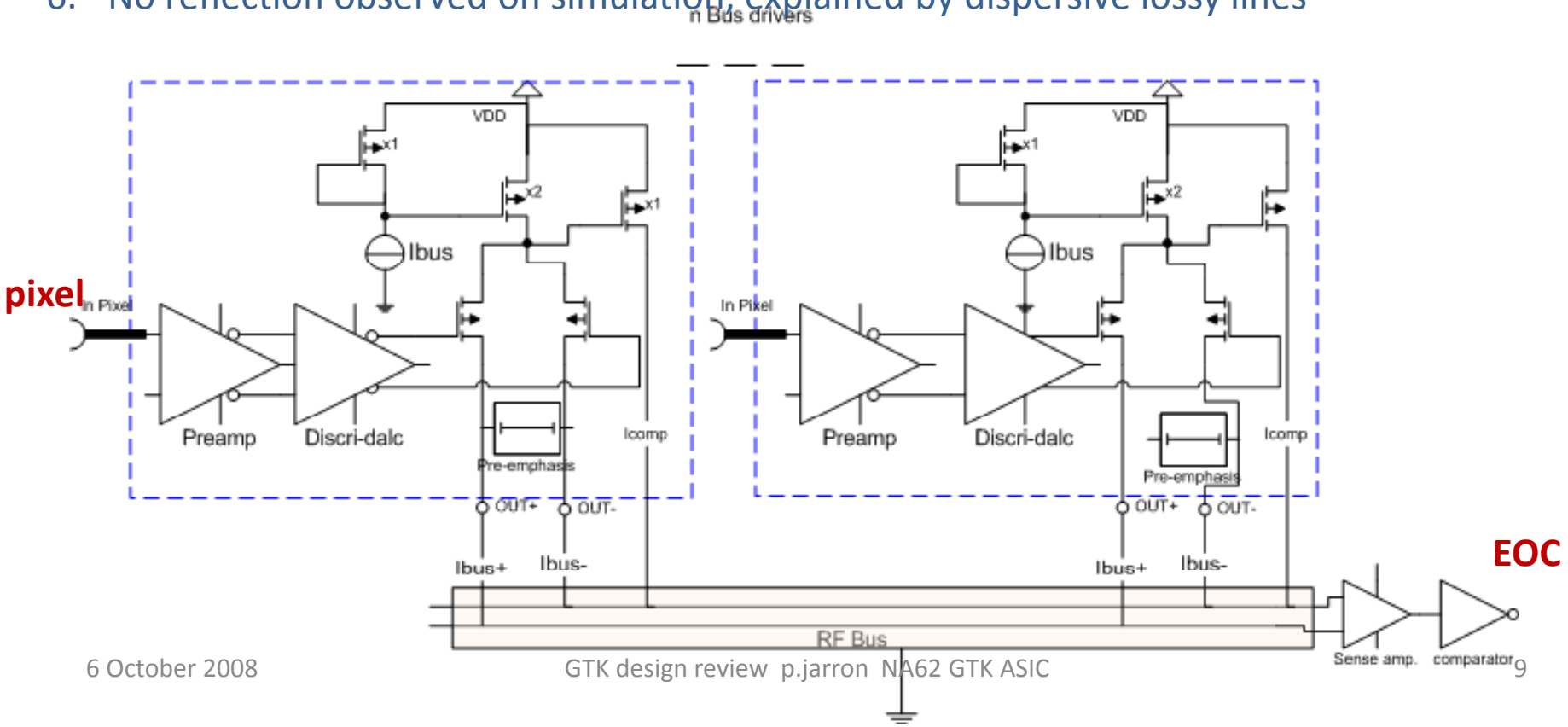
grounded lines has been chosen to avoid crosstalk between bus line





From pixel to end of column

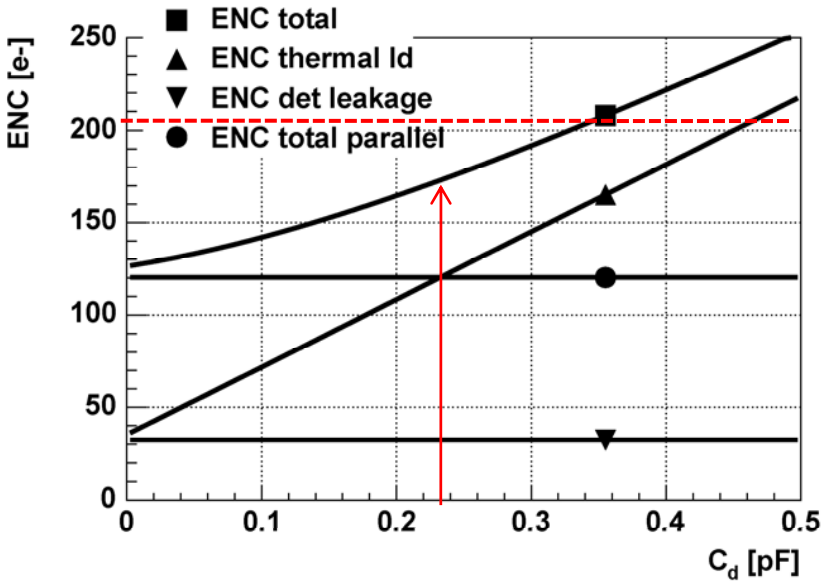
1. 9 Data lines have 5 pixels attached, each driver delivering 50 µA on the line: total 2x 250 µA
2. 5 Address lines have 9 pixels attached, each driver delivering 20 µA, a Total of 2x180 µA
3. Optimization not yet done with pre-emphasis, DC bias current might be lower
4. Transmission line (wave guide) has a odd impedance of about 40 Ω
5. Termination impedance is much higher, in the order of 200/300 Ω
6. No reflection observed on simulation, explained by dispersive lossy lines



130 nm IBM CMOS8RF DM noise analysis, silicon sensor signal

Preamp noise ENC f(Cd)

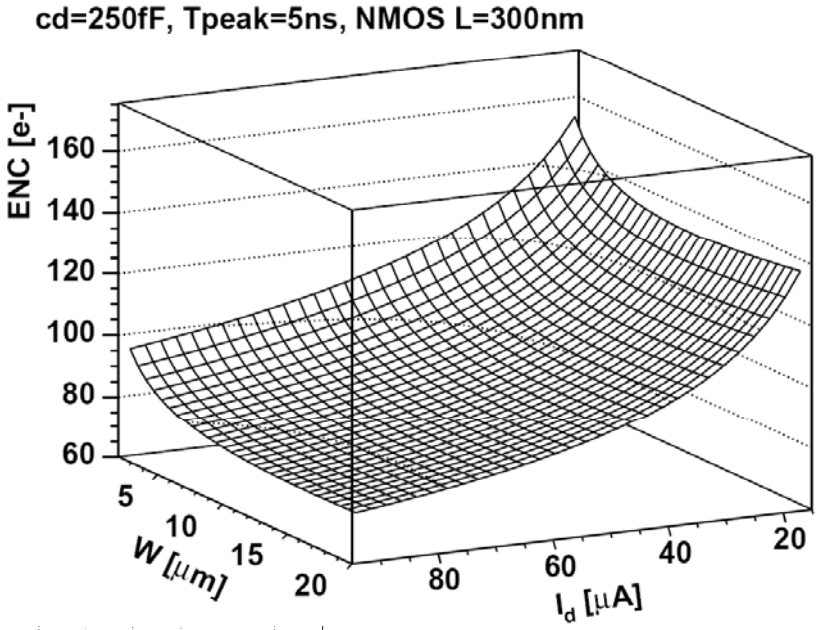
Parallel and series noise
Drain current 40 µA, leakage current 20 nA
5 ns peaking time – shaping equivalent to CR-RC^2

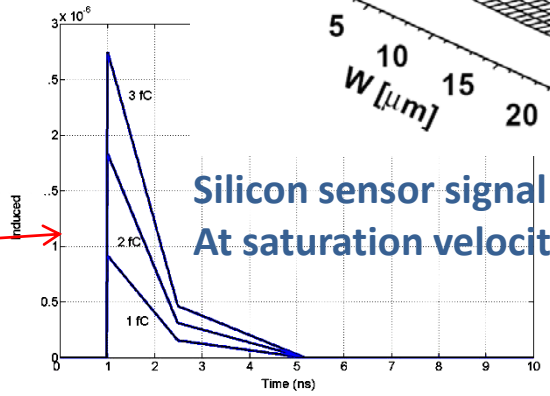


Risk of ballistic deficit

Input transistor optimization

Series noise only

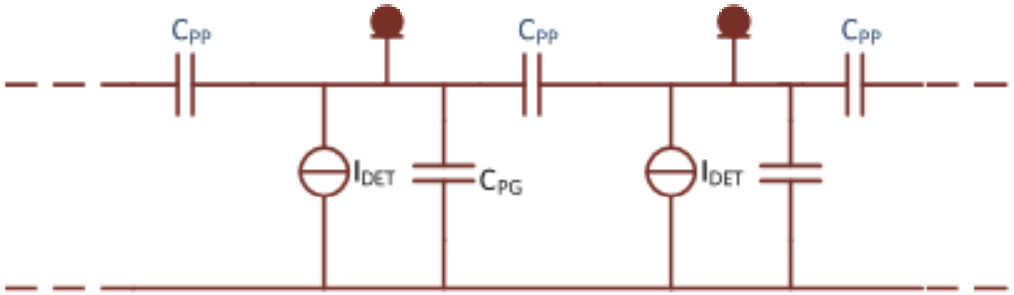




Silicon sensor signal formation
At saturation velocity

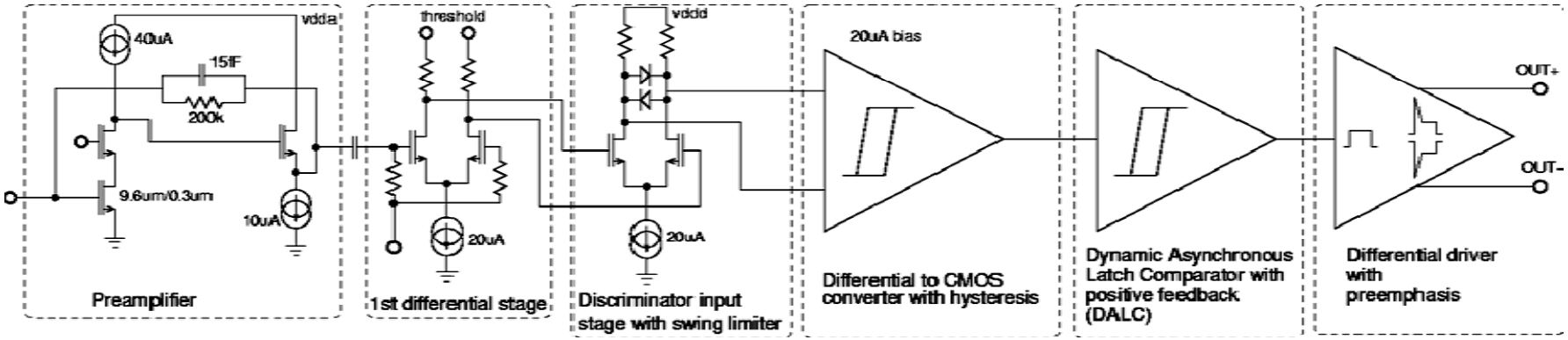
Modeling of the pixel sensor

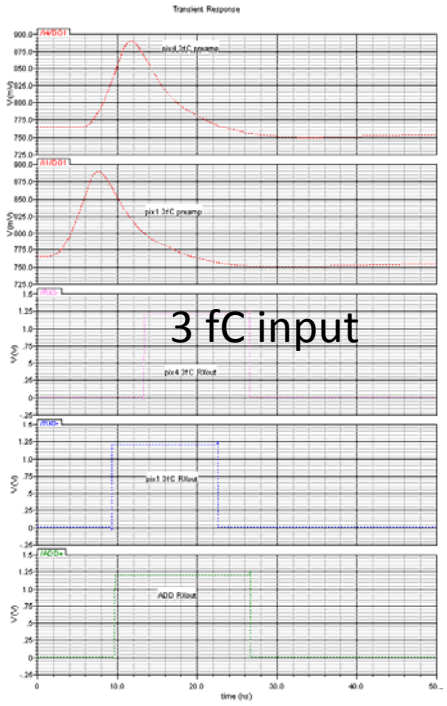
- Silicon sensor
  - Thickness 150 /200 µm
  - Cpp= 60 fF
  - Cpg= 80 fF
  - Idet , 3 ns pulse, from 0.8 to 3.2 fC, > 95% of events
- Diamond sensor
  - ?
- **But**
  - Lot of uncertainty of capacitance
  - Precise modeling would be welcome

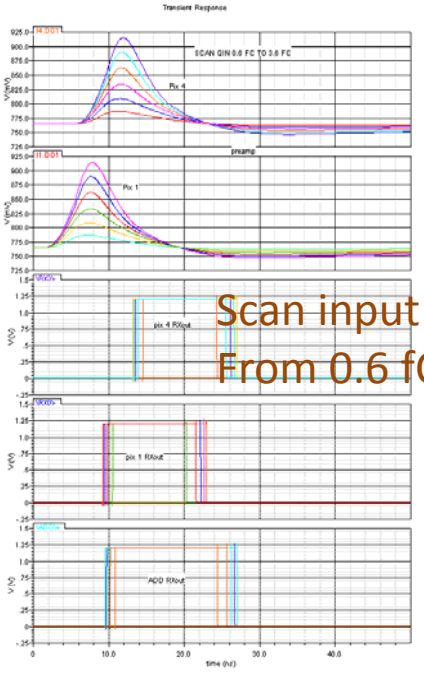


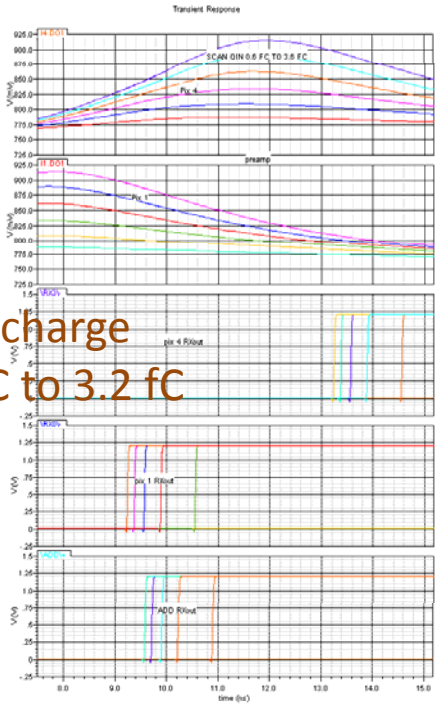
Pixel cell

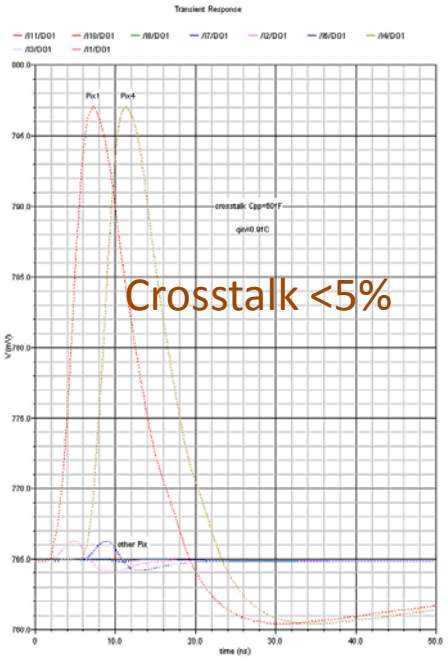
- Analogue, no digital circuit







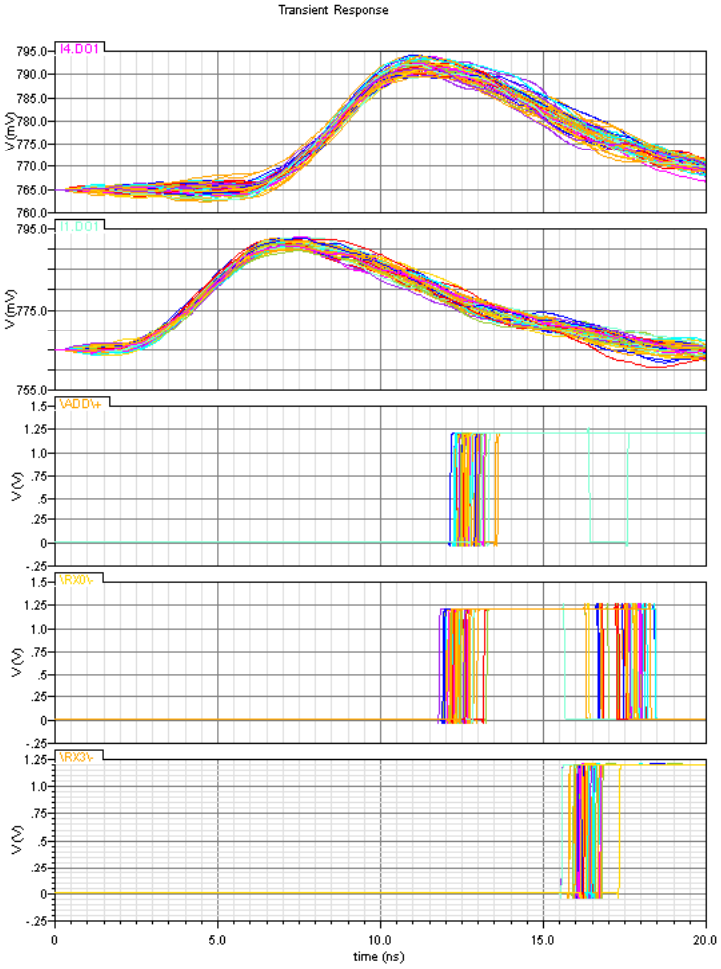




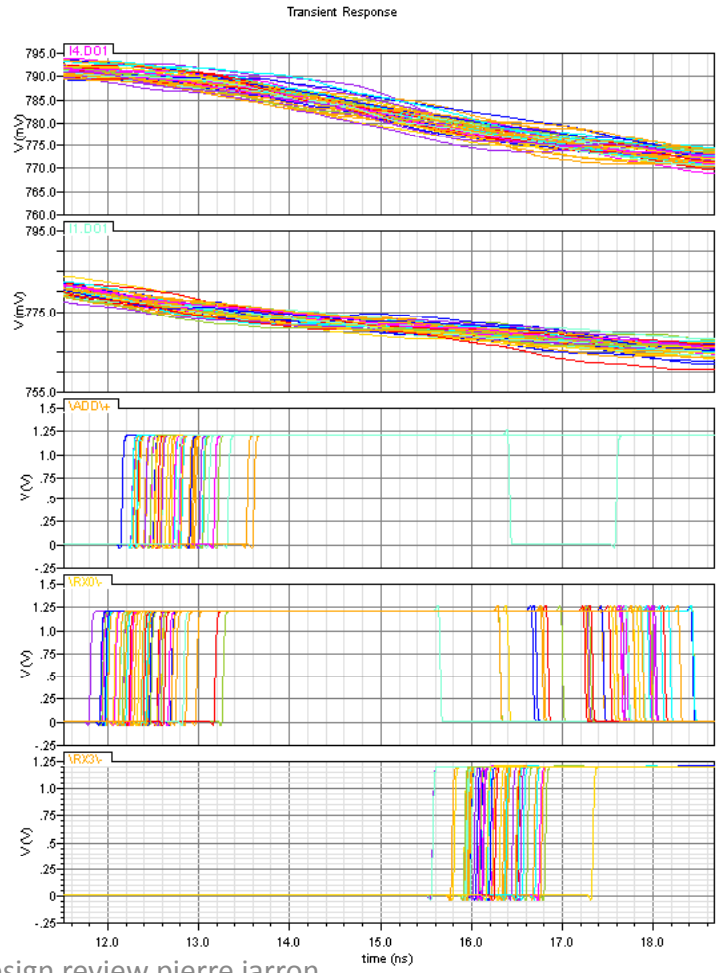
Noise simulation at minimum signal of 0.75fC

Transient noise simulation C_{PP}=60 fF, C_{PG}=80 fF

Qdet=0.75 fC, VT=42 mV

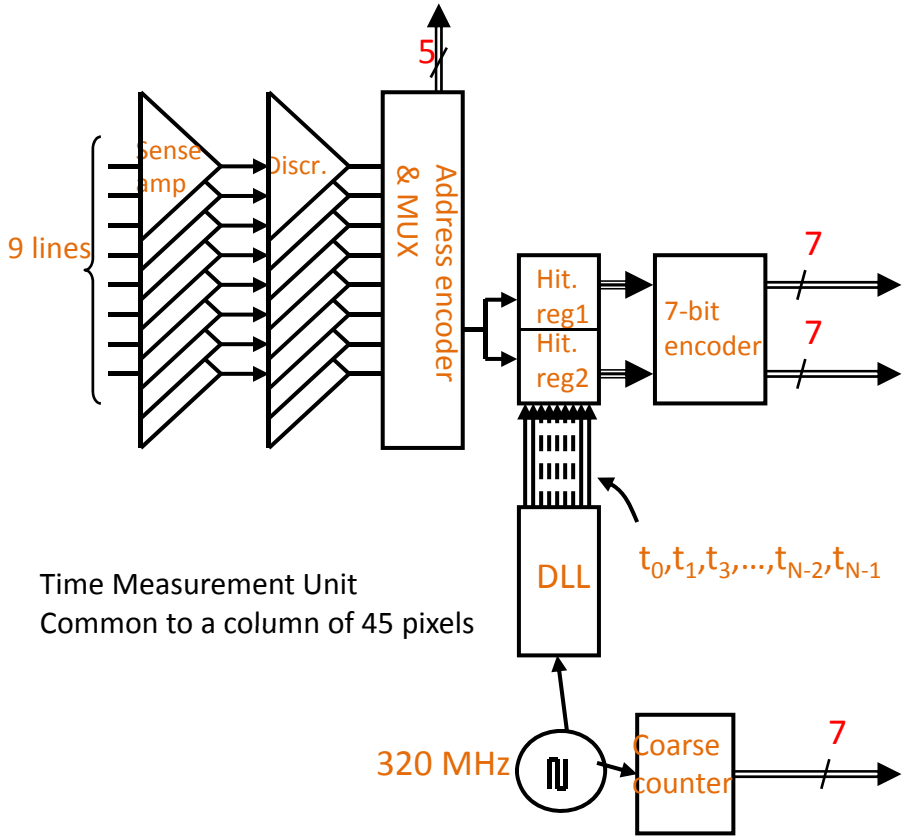


Close-up, Width= 5ns,
Jitter without TOT correction: 150 ps r.m.s



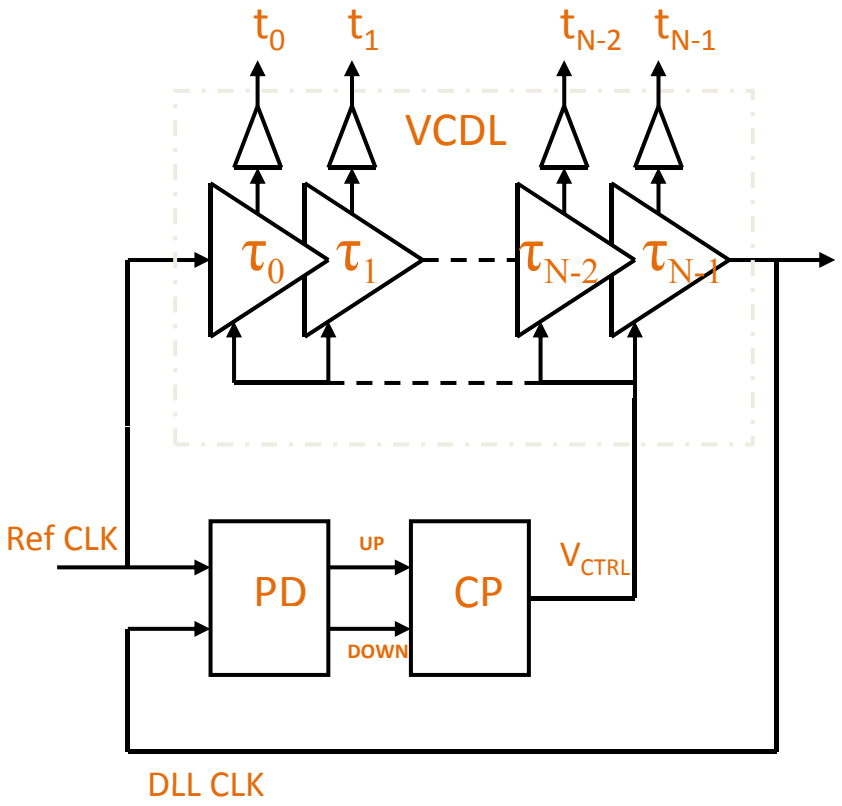
End of column processing

End of column block
Time Measurement Unit and pix address



Time Measurement Unit
Common to a column of 45 pixels

DLL based TDC,
32 delay cells, 100 ps bin



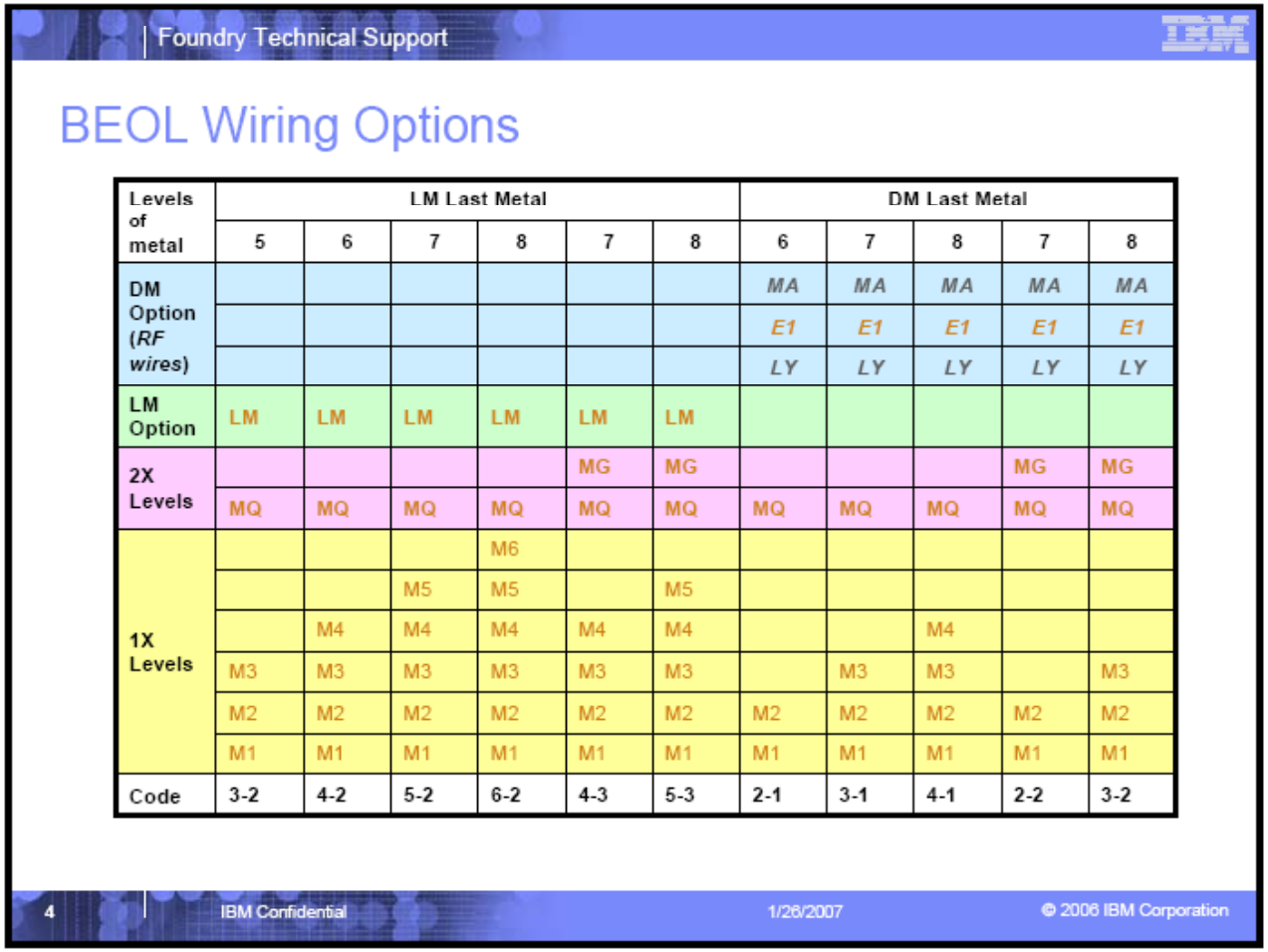
Power budget/pixel cell

component	Current (µA)	Voltage (V)	Power (µW)
preamp	40	1.2	48
amp	40	1.2	48
discriminator	40	1,2	48
Driver data	100 (50)	0.4	40 (20)
Driver Add	40 (20)	0.4	16 (8)
Total	260 (190)		202 (175)

Power budget/EOC column

component	Current (µA)	Voltage (V)	Power (µW)
receiver	100 (50)	0.8	80 (40) x 14= 1.12
DLL		1.2	
TDC		1,2	
Total			

LM DM options



Foundry Technical Support

BEOL Wiring Options

Levels of metal	LM Last Metal						DM Last Metal				
	5	6	7	8	7	8	6	7	8	7	8
DM Option (*RF wires*)							*MA*	*MA*	*MA*	*MA*	*MA*
							E1	*E1*	*E1*	*E1*	*E1*
							LY	*LY*	*LY*	*LY*	*LY*
LM Option	LM	LM	LM	LM	LM	LM					
2X Levels					MG	MG				MG	MG
	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ	MQ
1X Levels				M6							
			M5	M5		M5					
		M4	M4	M4	M4	M4			M4		
	M3	M3	M3	M3	M3	M3		M3	M3		M3
	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2	M2
	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
Code	3-2	4-2	5-2	6-2	4-3	5-3	2-1	3-1	4-1	2-2	3-2

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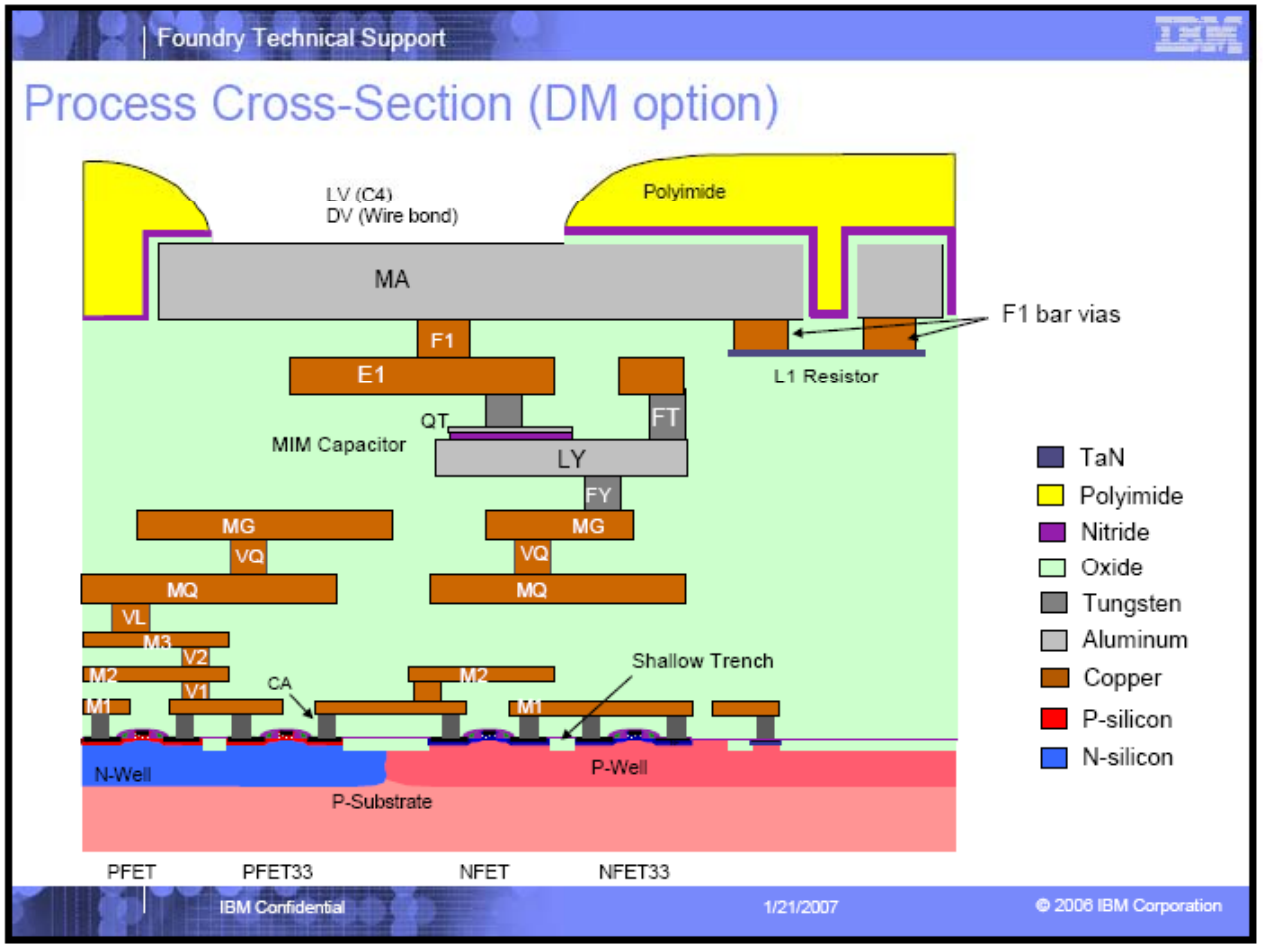
DM option selected



Summary of the EOC overview

- Pixel cell
  - Preamplifier works fine with ENC<200 rms e-
  - Discriminator width is linear with amplitude
    - Walk easily corrected down to less than 100 ps
- Concept of transmission line based bus system
  - Looks working well with pre-emphasis
  - Encoding 9x5 bus
    - has an efficiency dependent of the max pulse width
  - Receiver circuit inspired from NINO looks good
    - Power optimization not yet done
    - Offset compensation to be done
- End of column TDC
  - Looks O.K though very dense
  - Problem of top simulation
- Simulation with Spectre with complex (top) analog circuit
  - Problems after problems with the DM design kit, much less with LM?
- Submission in November
  - Looks difficult, I prefer to postpone in January