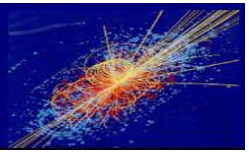
# TDC per pixel option: architecture description

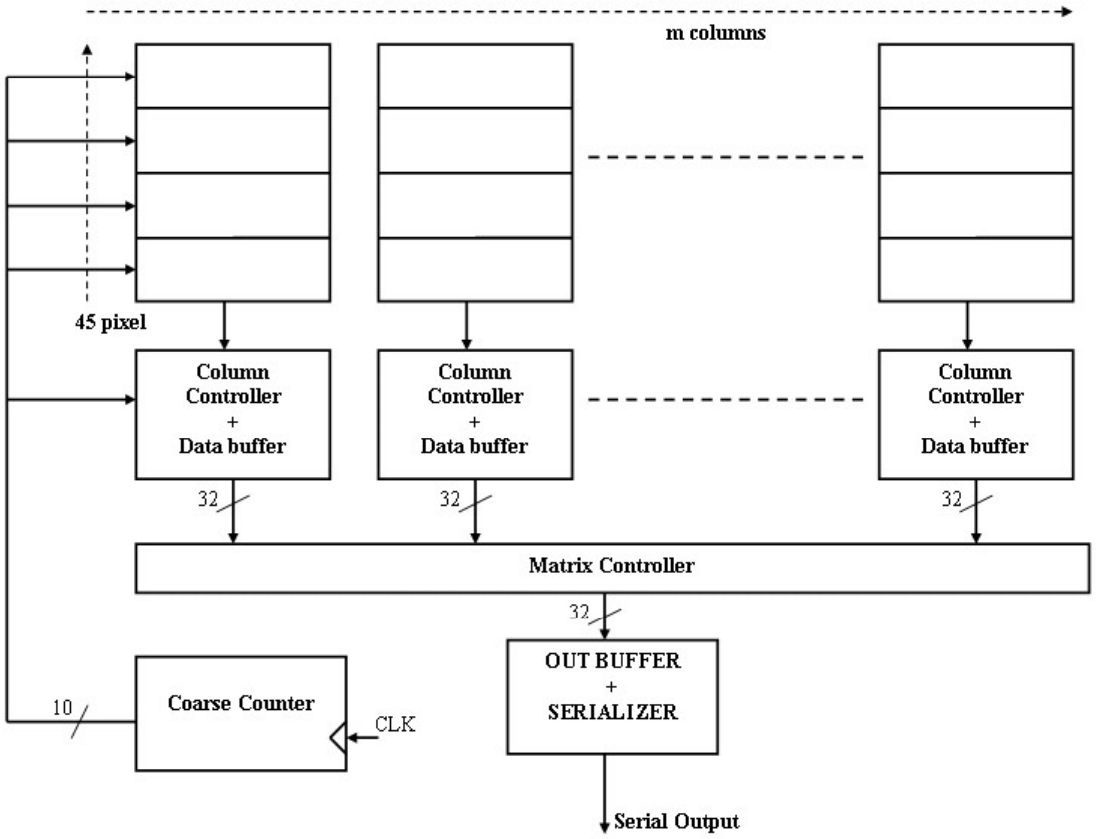
**A. Rivetti**

# Basic features



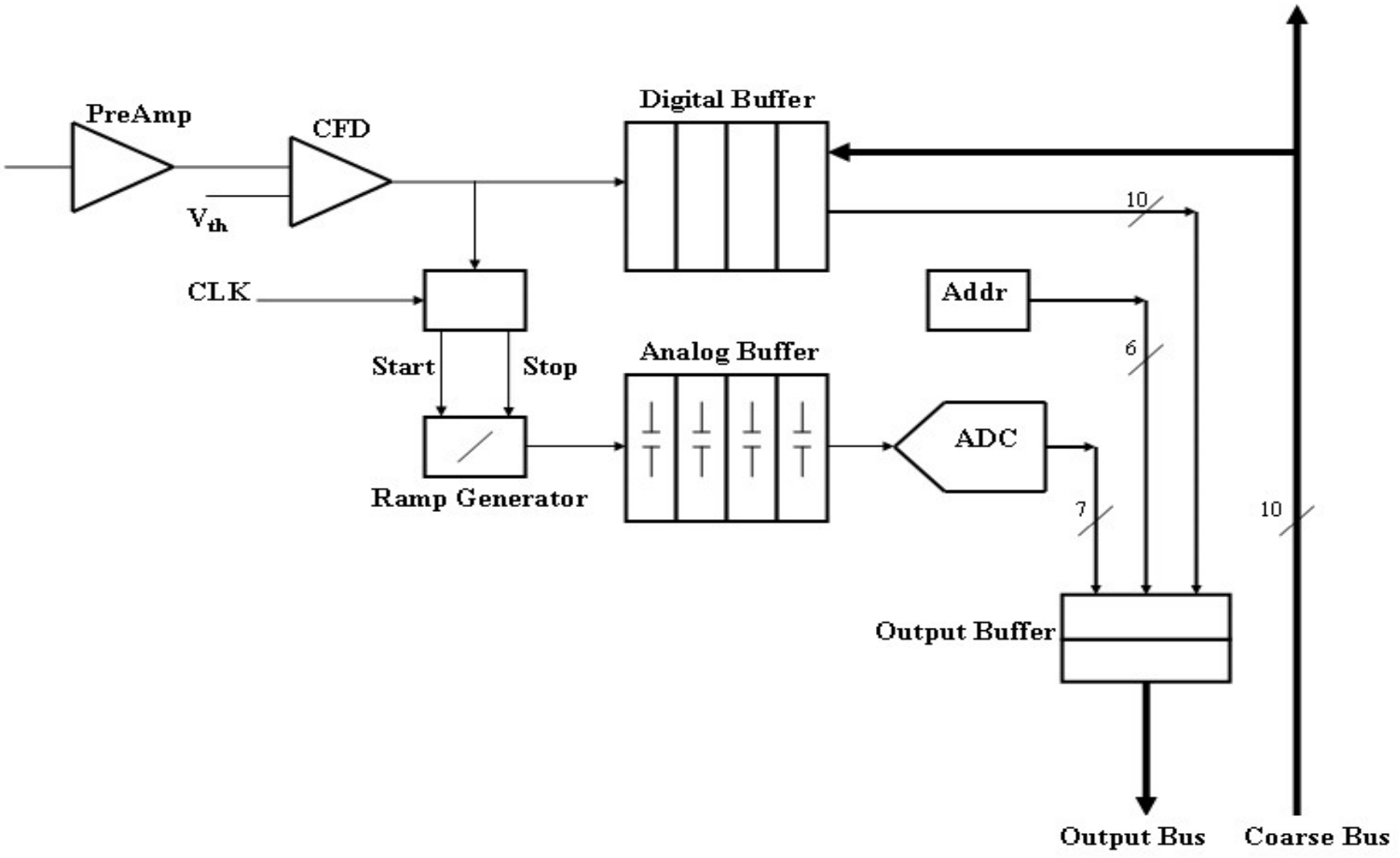
- The time walk correction:
  - Done inside the pixel with a Constant Fraction Discriminator (CFD).
- Time digitization:
  - Coarse time: Gray counter distributed to the pixels.
  - Fine measurement: Time to Amplitude (TAC) converter in each pixel
- Data derandomization and transmission:
  - Four-level buffer inside the pixel and high-speed serial links for off-chip transmission

# Architecture overview

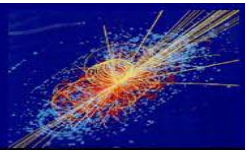



- System Clock: 160 MHz
- Global coarse counter (10 bits)
- Each column of 45 pixels is read-out by its own controller (End-of-Column controller)
- Only digital buses between pixels and EoC controller
- The Matrix controller will merge data coming from m columns (where m depend on the link speed)
- Derandomization done inside the pixel. Token-based read-out scheme.

# Pixel building blocks

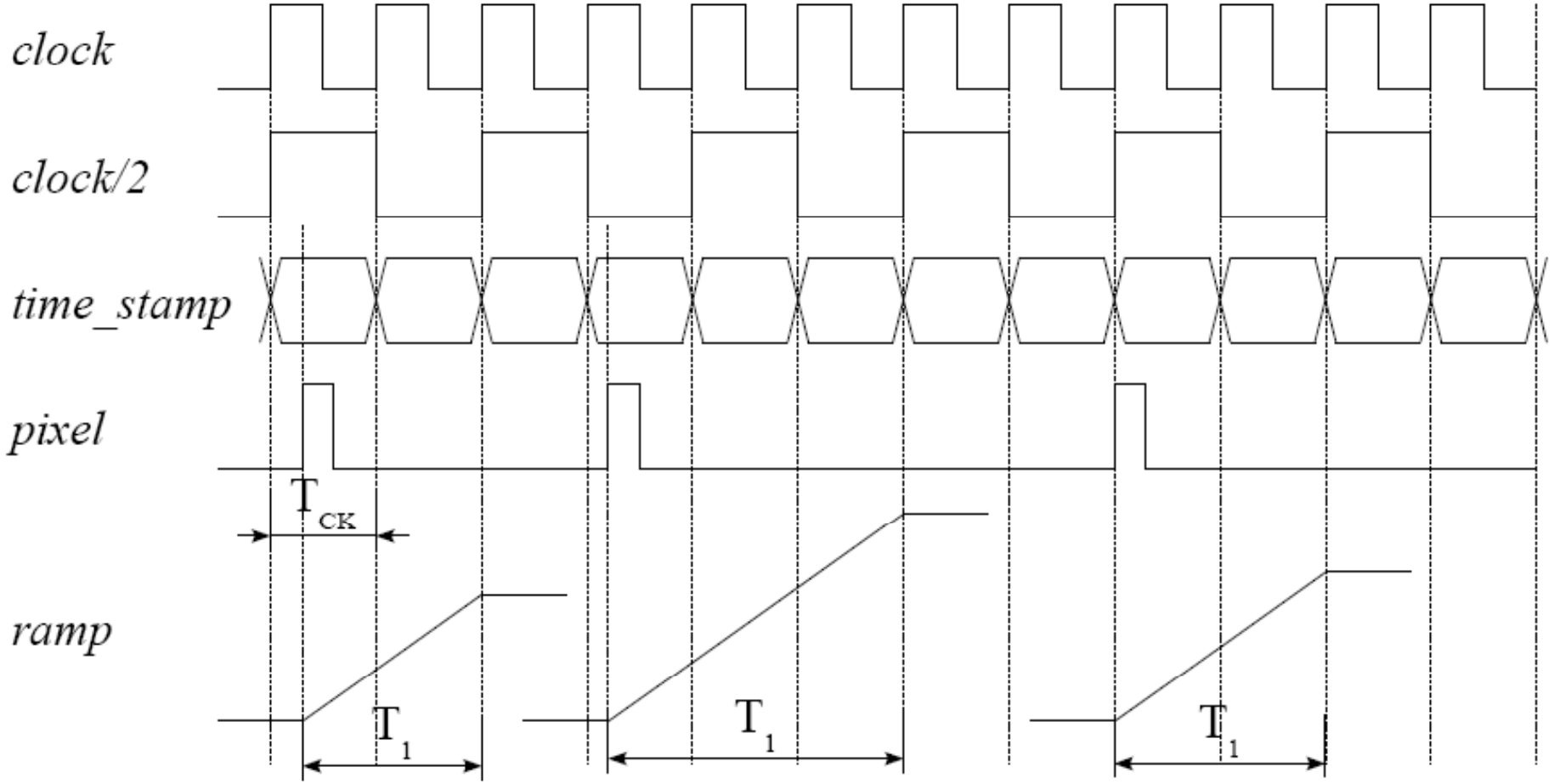


# Pixel operation



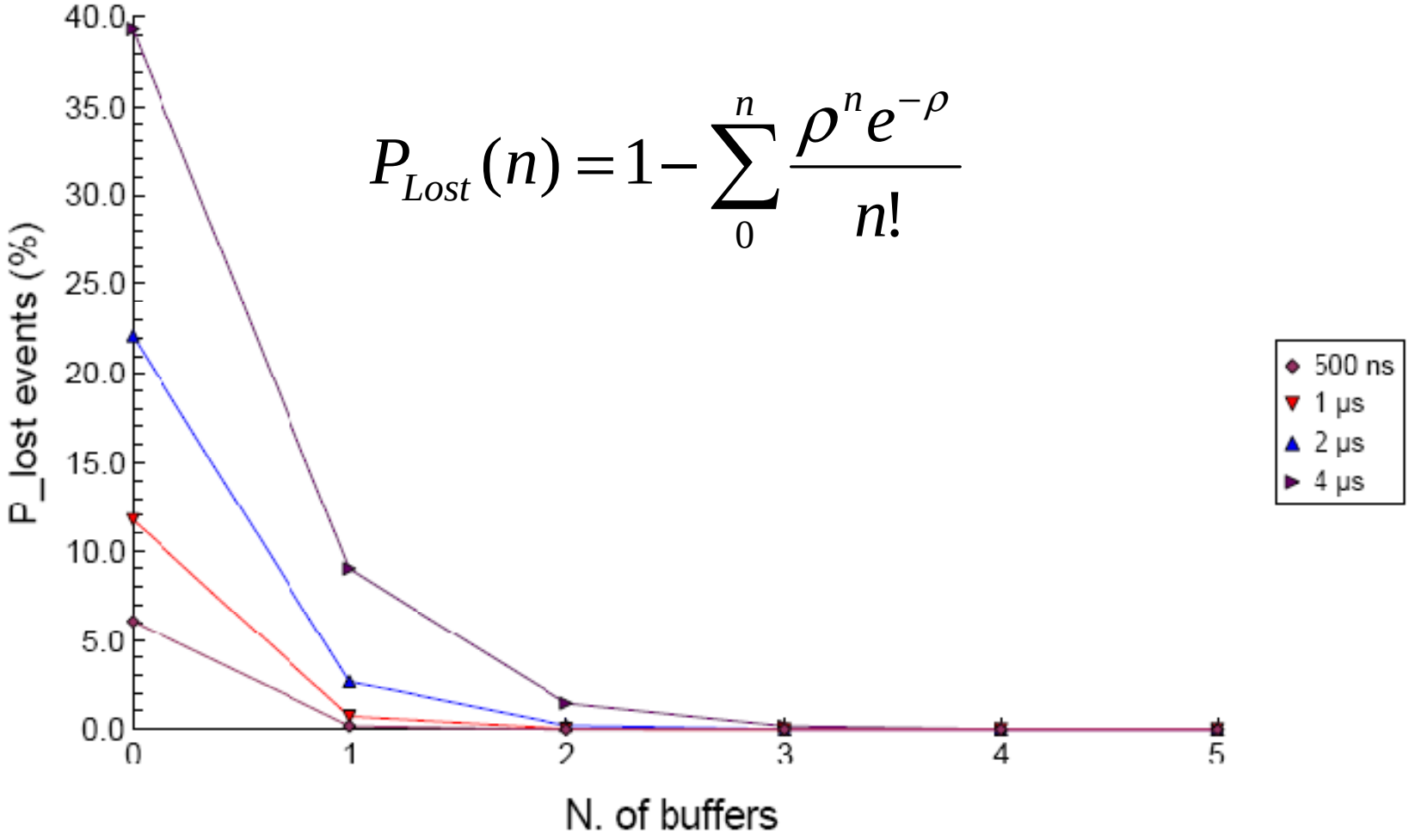
- A coarse counter counts the 160 MHz clock. The word is Gray-encoded and distributed to the pixels.
- The value of the coarse counter is latched into local pixel registers when the CFD fires.
- At the same time a constant current source starts charging-up a capacitor.
- The charging process is stopped at the first leading edge following a trailing edge of the master clock.
- The analogue value stored in the capacitor is digitized with a Wilkinson ADC to provide the fine-time measurement.
- The range of the TDC spans three master clock cycles to guarantee adequate analogue measurement and accommodate time mismatch between the coarse and fine counter
- TDC time bin: 97.6 ps

# Timing waveforms

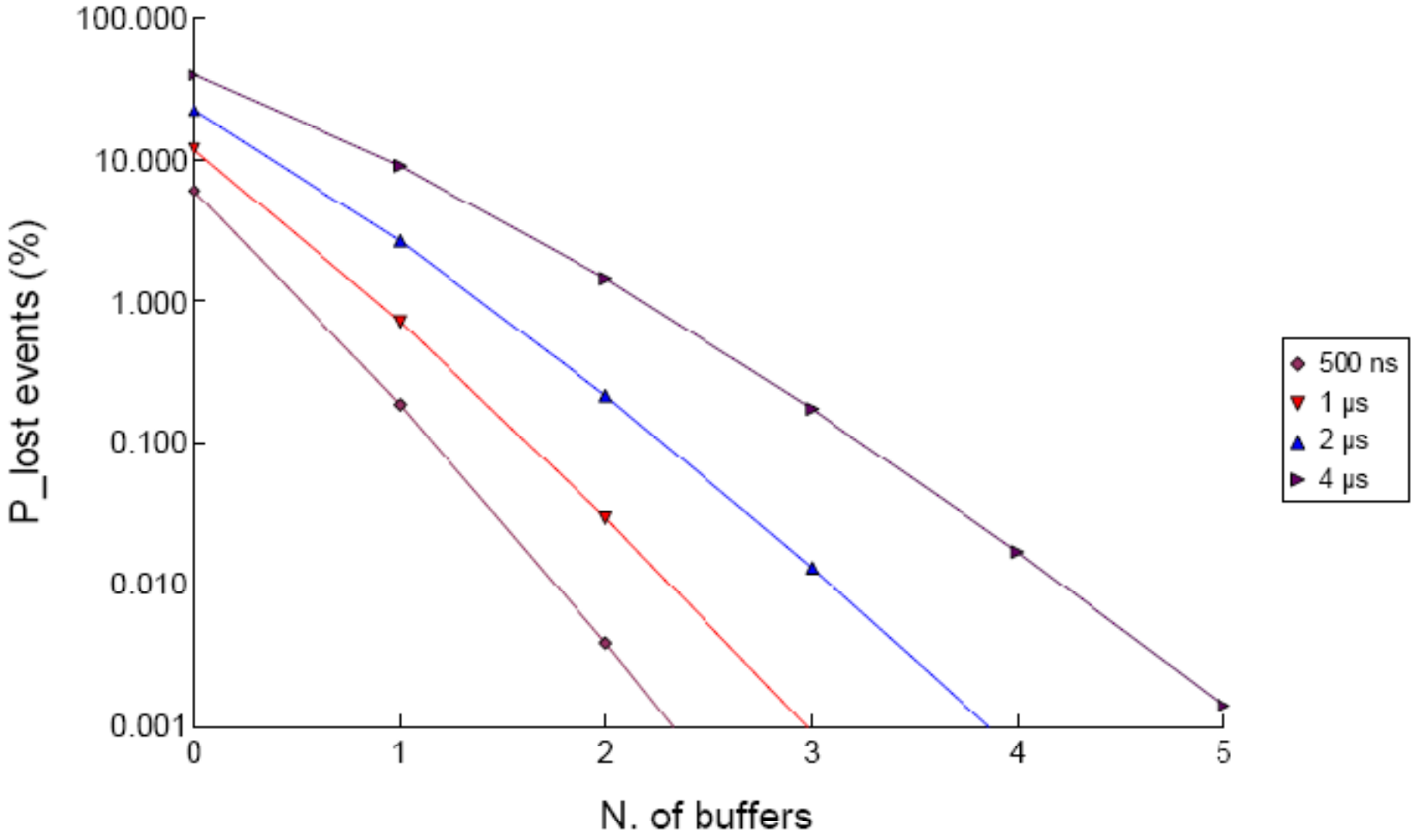


# How many buffers?

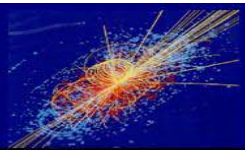
$$P_{Lost}(n) = 1 - \sum_{0}^{n} \frac{\rho^n e^{-\rho}}{n!}$$



# How many buffers?



# Advantages and drawback

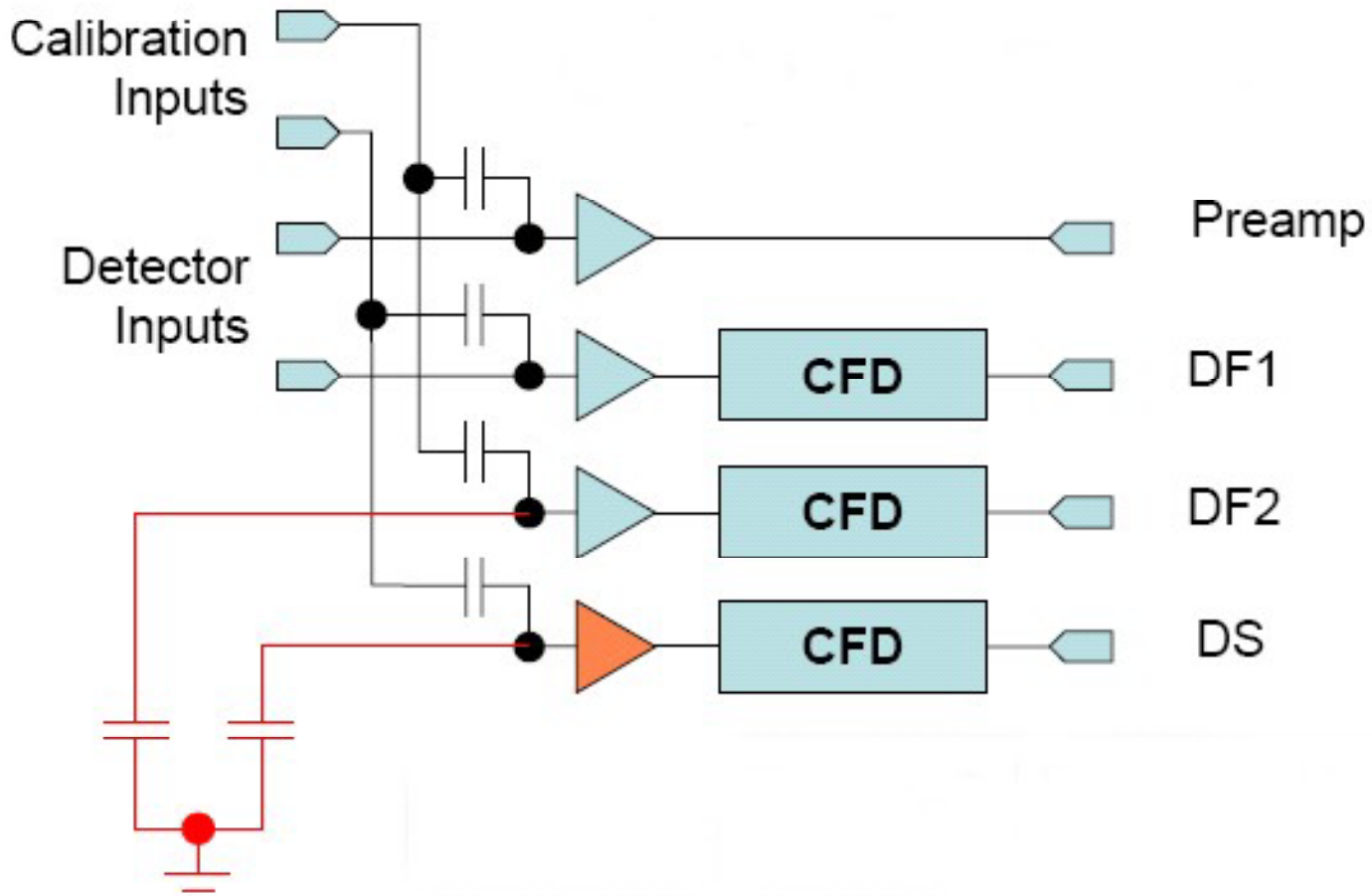


- Optimal usage of pixel area (300 μm x 300 μm).
- Simplified read-out scheme.
- No analogue signal propagation outside the pixel…
- Lower system clock (160 MHz vs 320 MHz.)

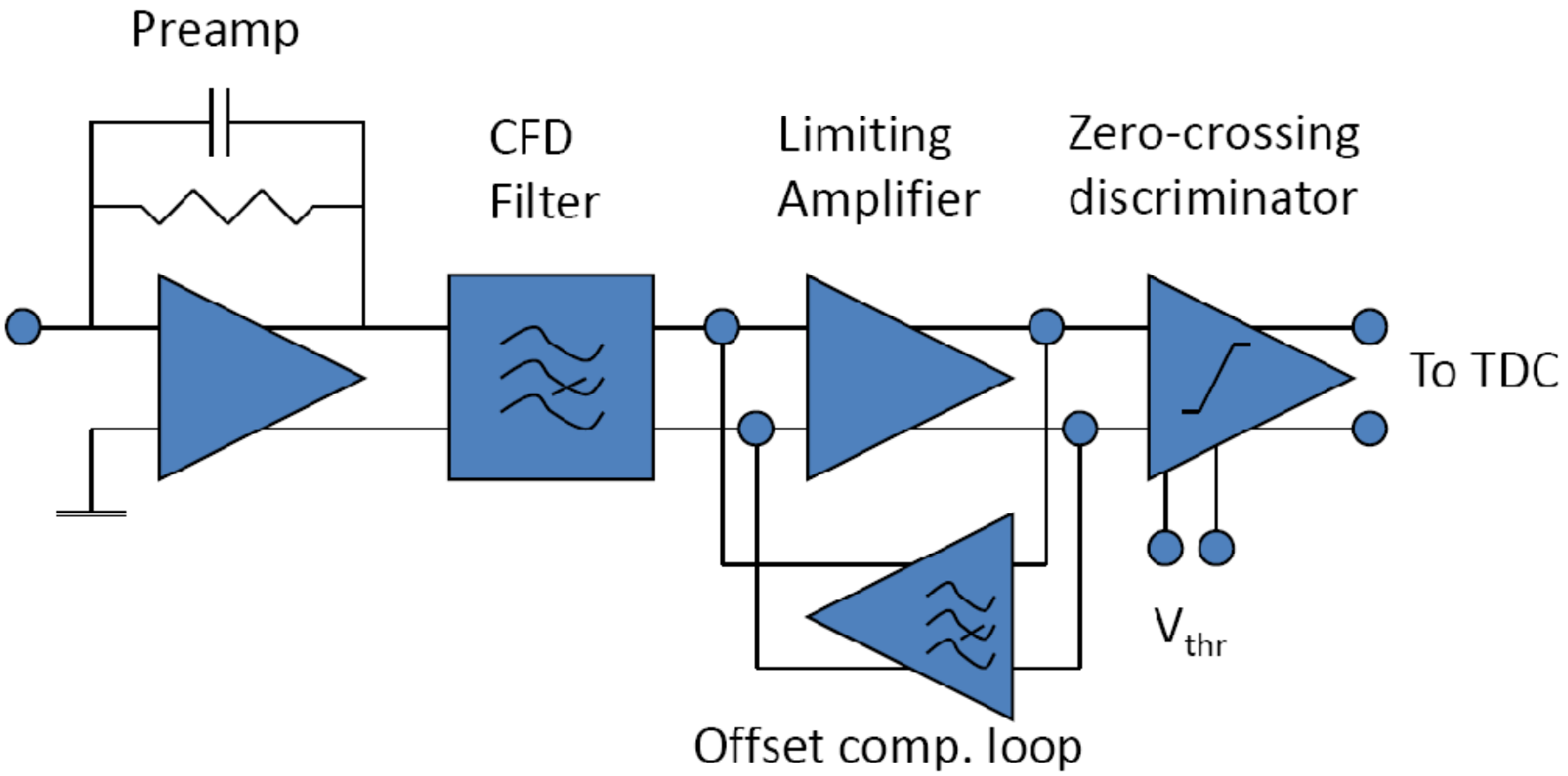
But…

- More digital activity close to the front-end.
- More digital logic in critical area => SEU tolerance required.
- Needs careful clock distribution over the whole matrix.

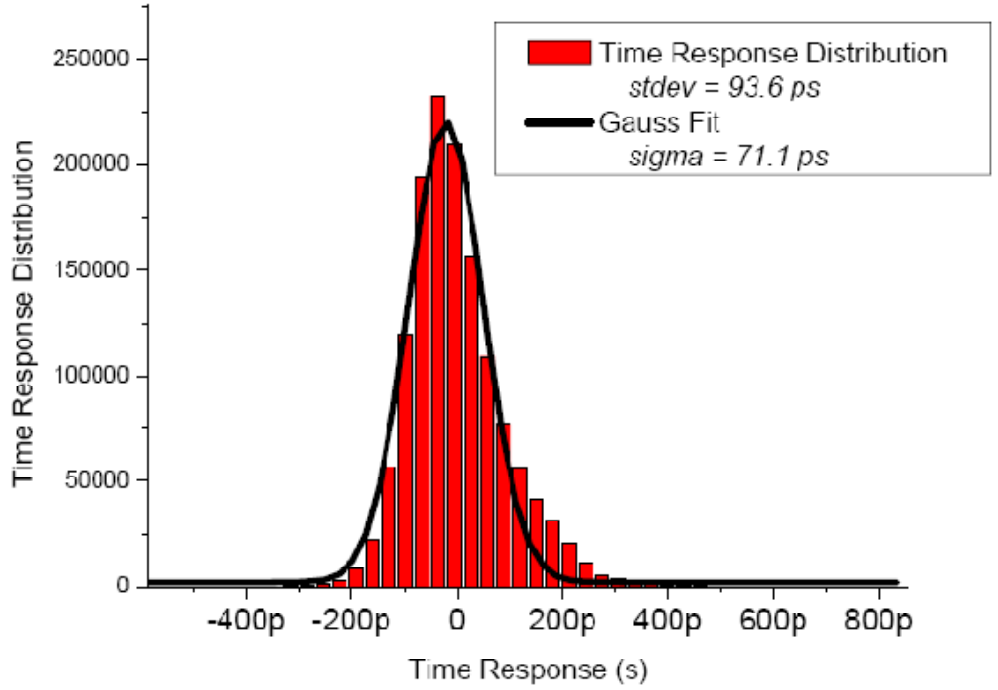
# First prototypes



# Prototype building blocks

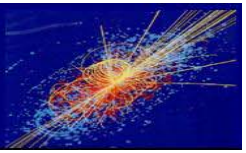


# Expected time resolution




- Total resolution calculated through Monte-Carlo based on the jitter and residual walk measuremets of the first prototype.

# demonstrator chip: key points



- Full pixel design.
- Two full columns with 45 pixels each.
- One spare column with 15 pixels.
- Final End of Column logic
- Not final data transmission scheme

# TDC on pixel demo chip