NA62 front end for end of column demonstrator

Jan Kaplon/Pierre Jarron

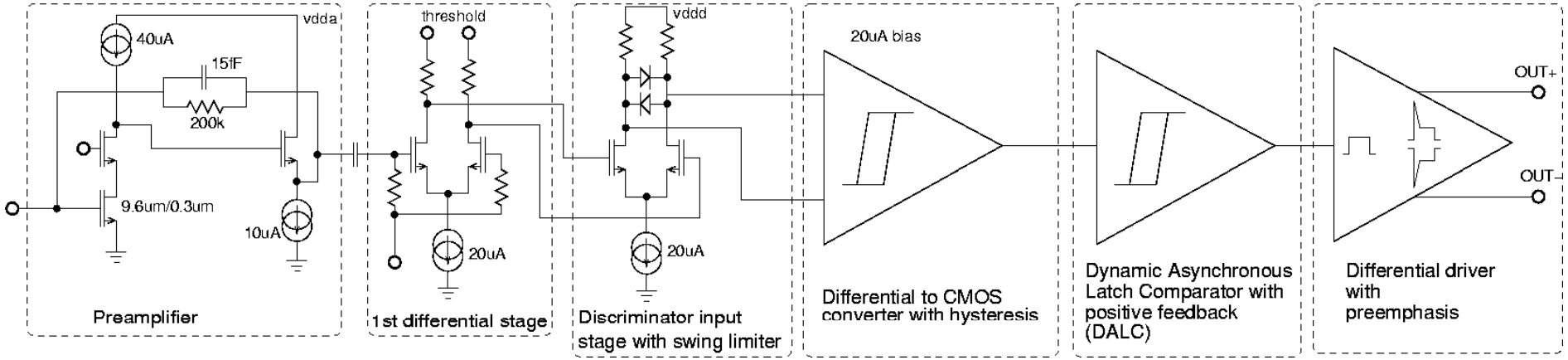
Architecture

Preamp; buffered cascode (NMOS input transistor), resistive feedback (200k)

Gain;70mV/fC (27mV/fC at preamp output)

Preamplifier AC coupled to shaper and discriminator stages

Consumption (without transmission line driver) ; 120uA/pixel



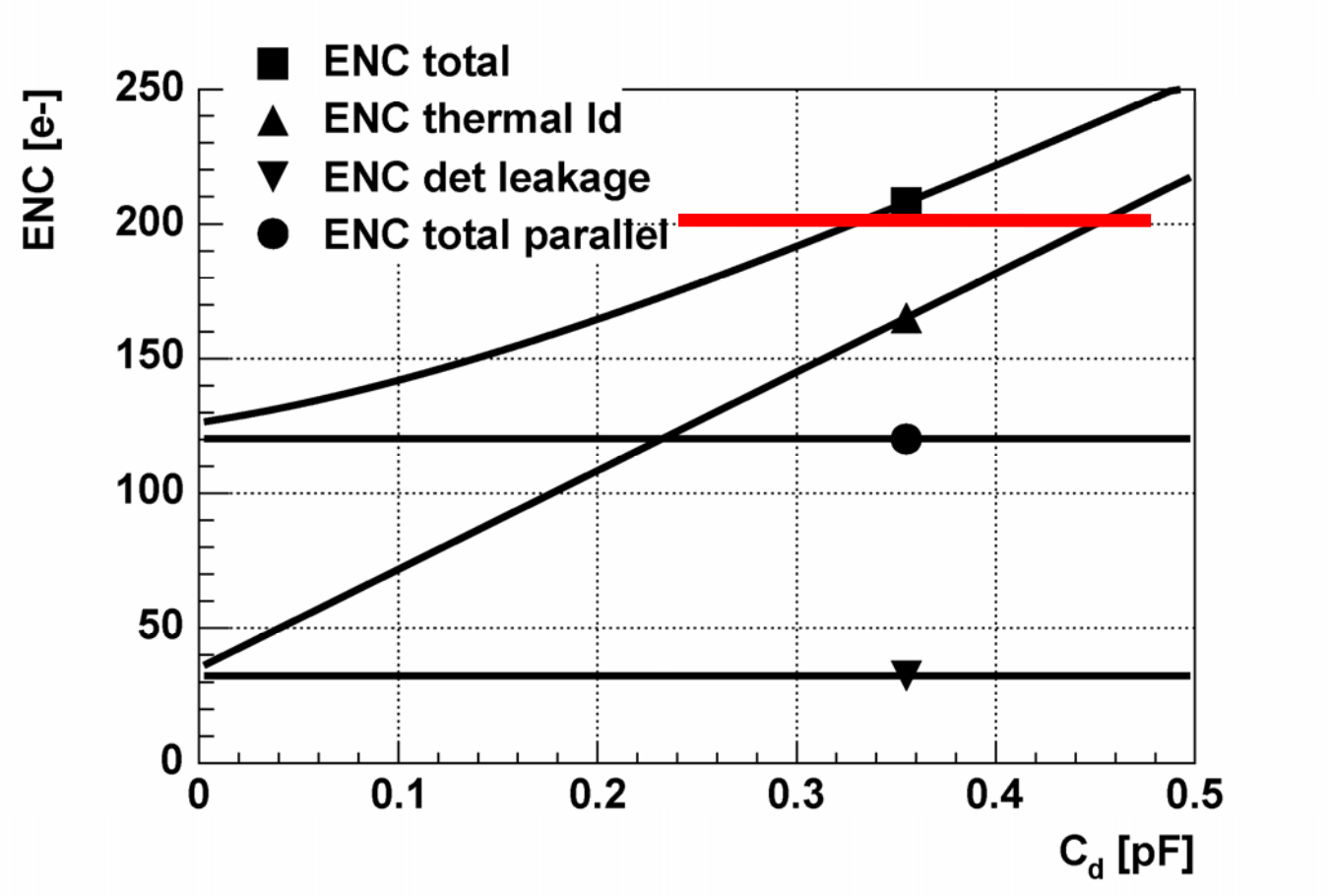
Feedback ;

Cf=14 fF

Rf= 200k

Input transistor; NMOS 9.6/0.3um, 40uA bias

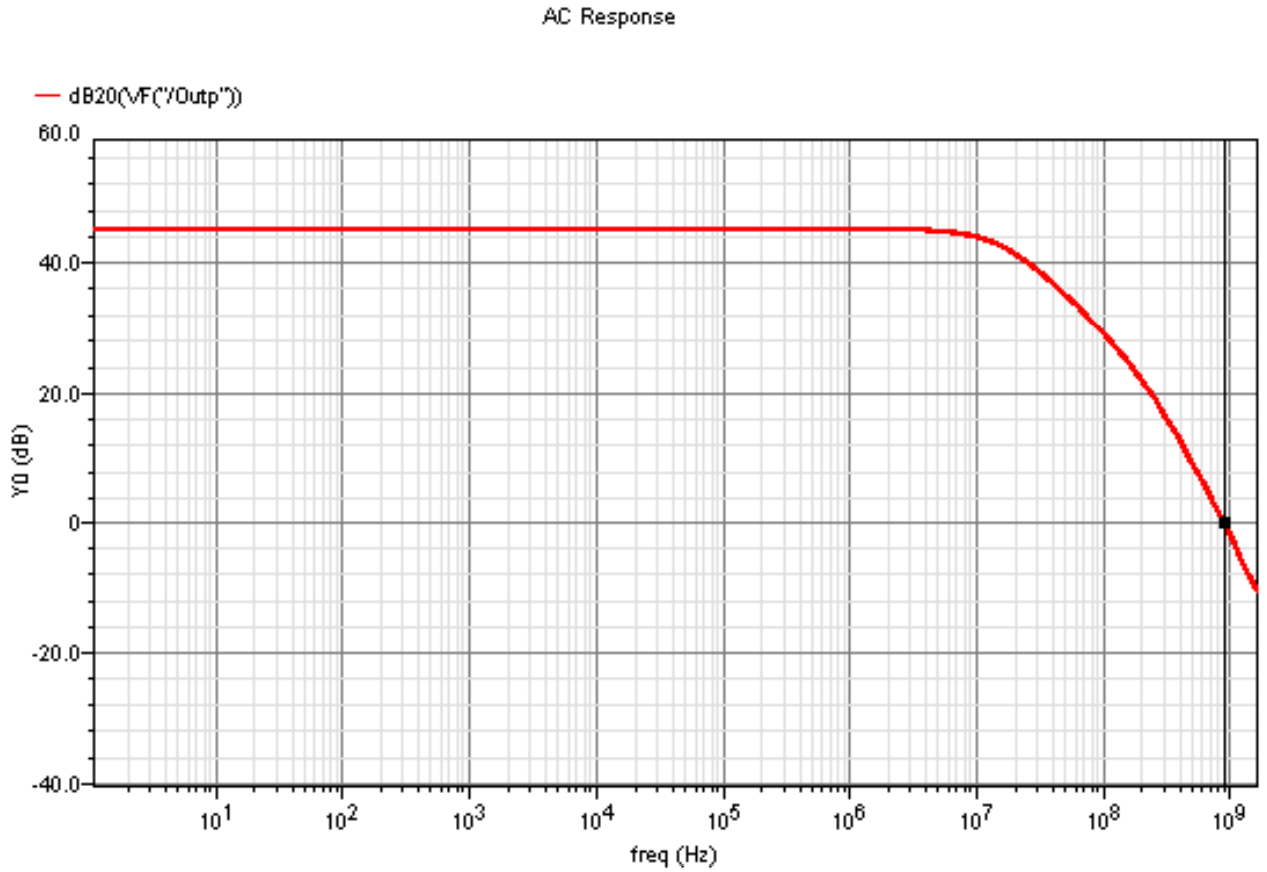
Noise



5ns peaking time CR-RC^2
Input transistor bias; 40uA, Feedback resistor 200kΩ
Detector leakage; 20nA

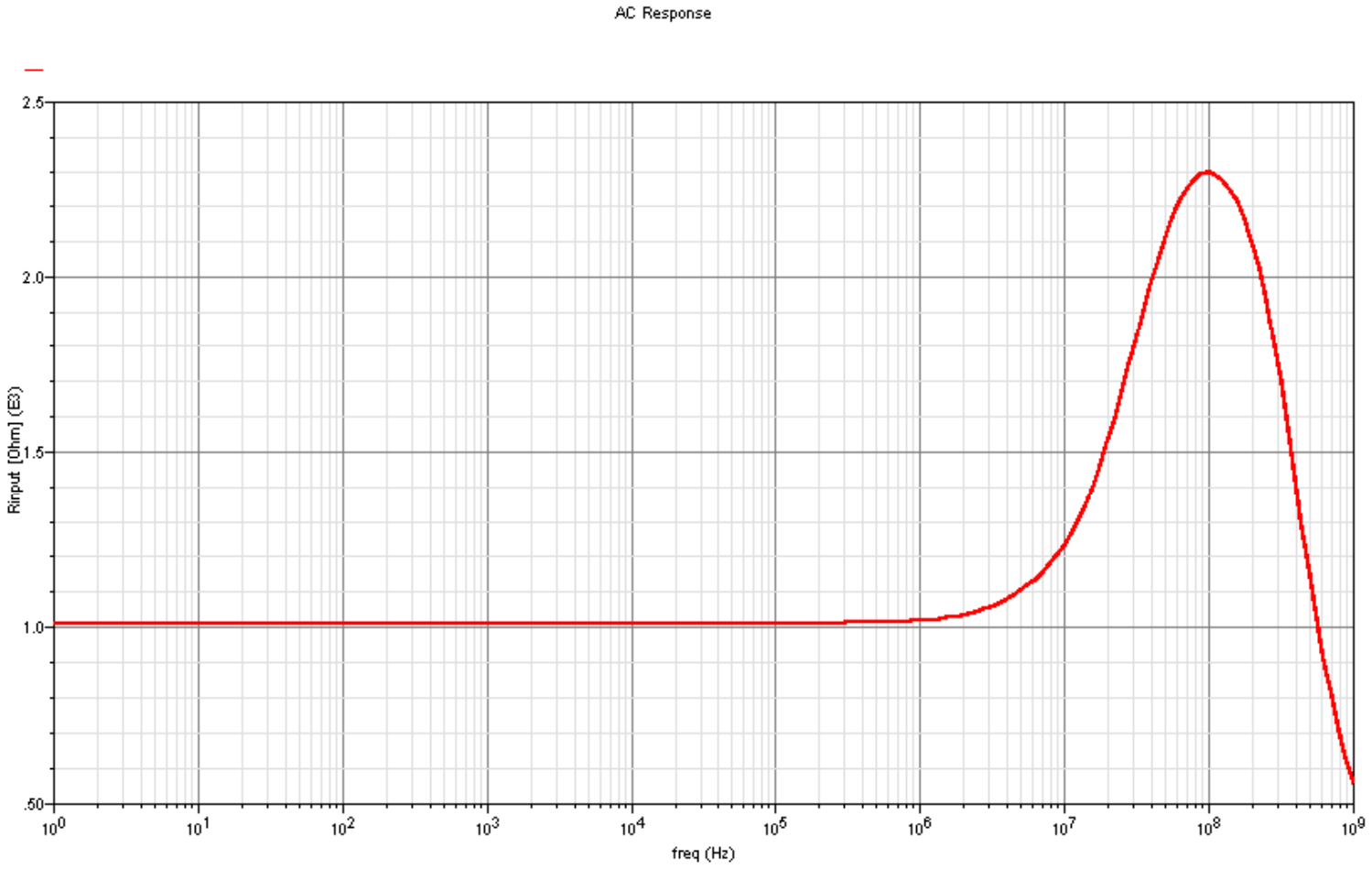
Open loop gain simulation

Gain Bandwidth Product 900MHz (simulation for compensated cascode)



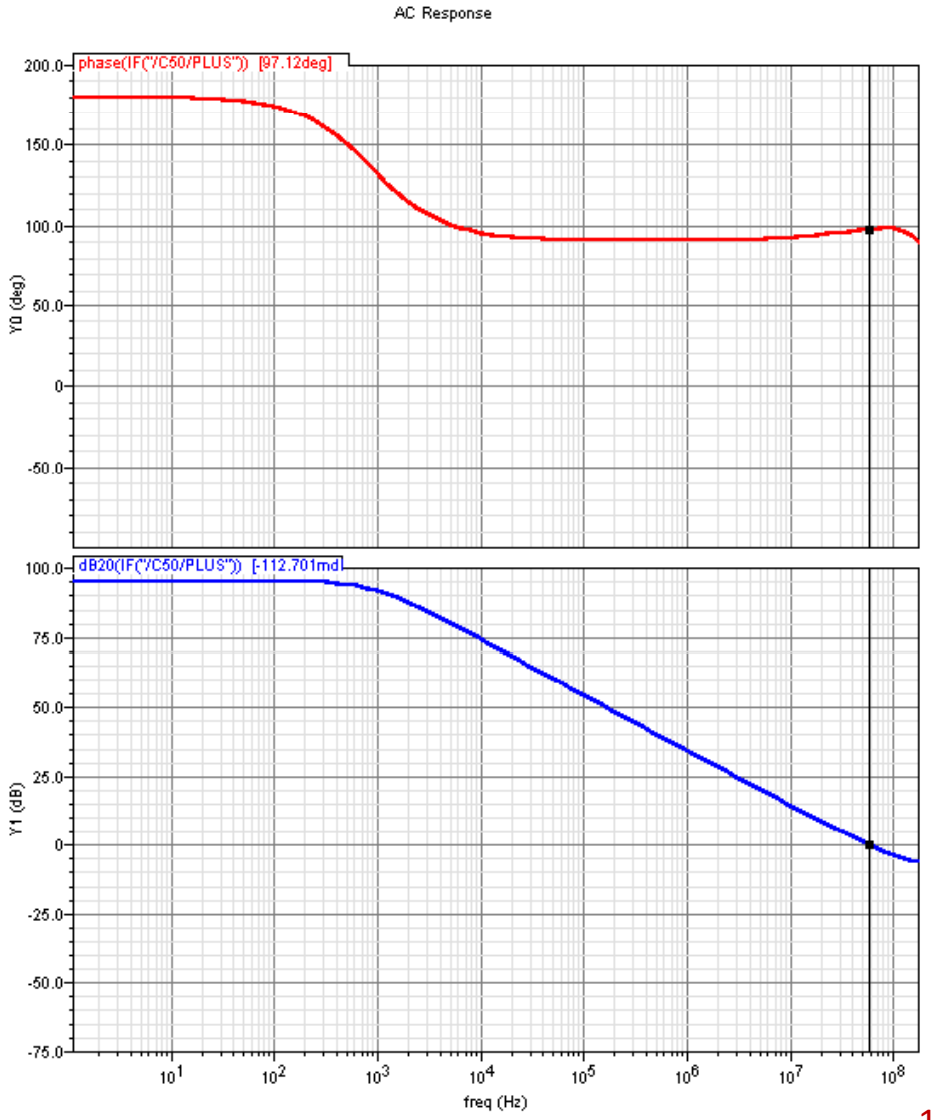
Input impedance simulation

Input impedance 1 – 2kΩ



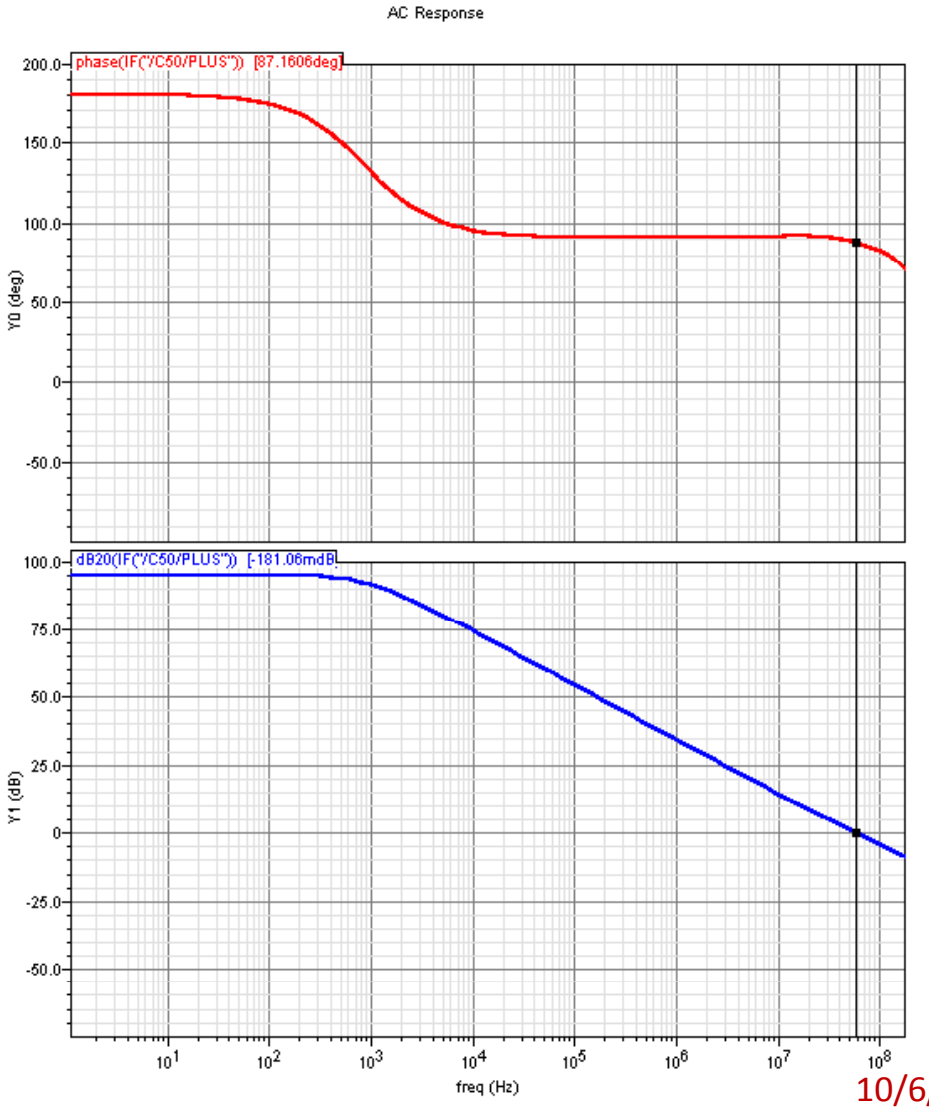
Phase margin simulation

Phase margin for Cinput 250fF ; 90^{o}

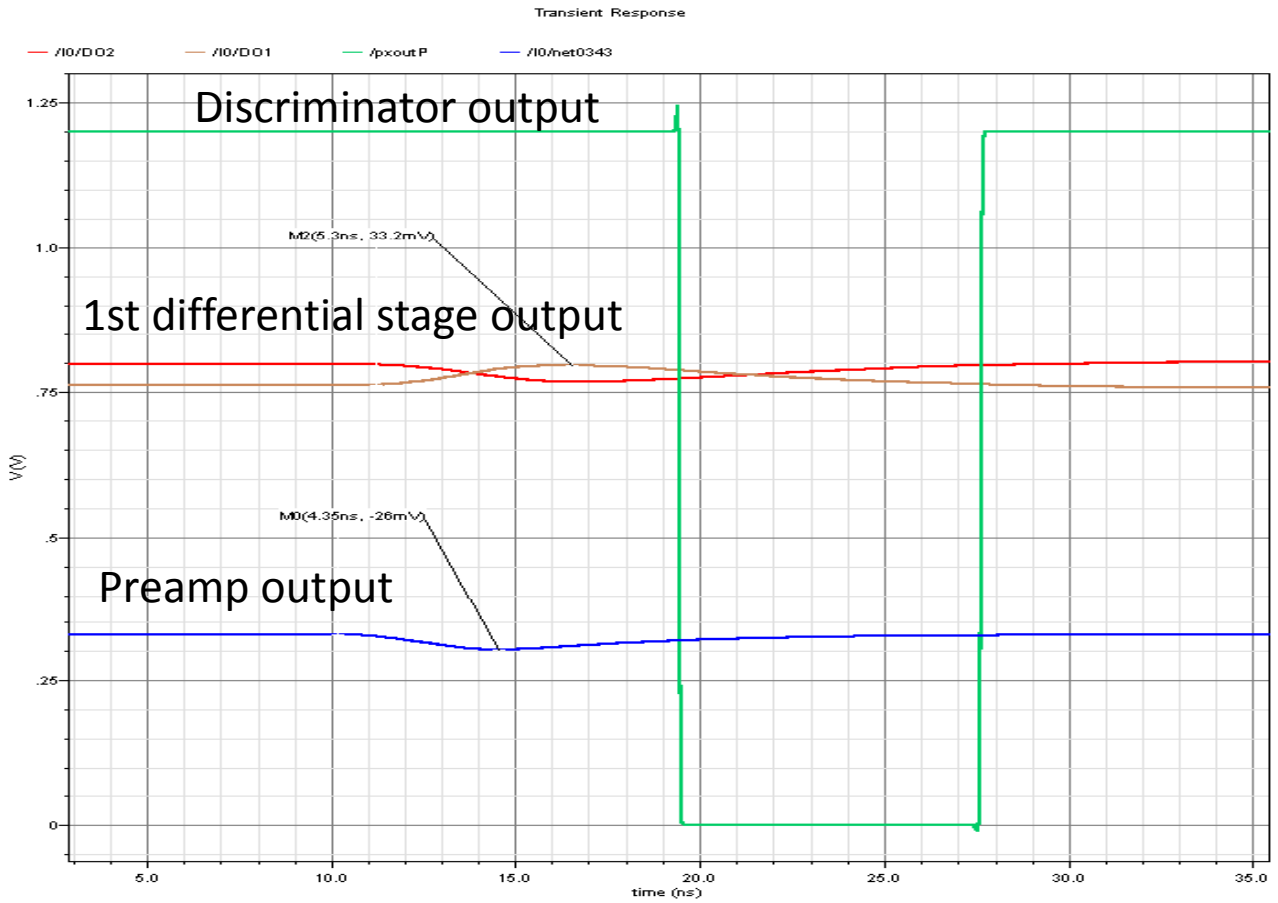


Phase margin simulation

Phase margin for Cinput 500fF ; 87º



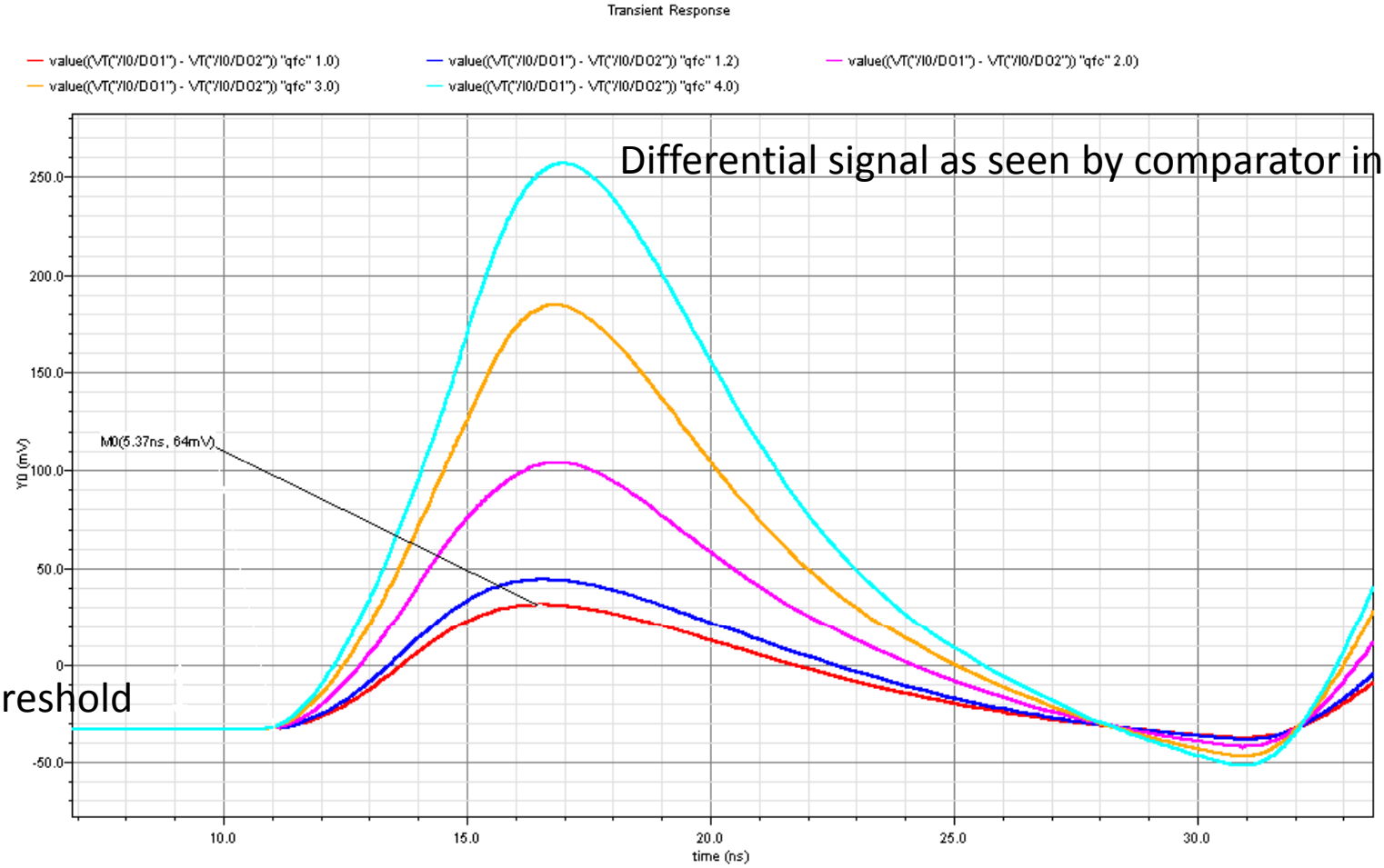
Transient simulation



Peaking time; 4.5ns at preamp, 5.5ns at discriminator input

Transient simulation

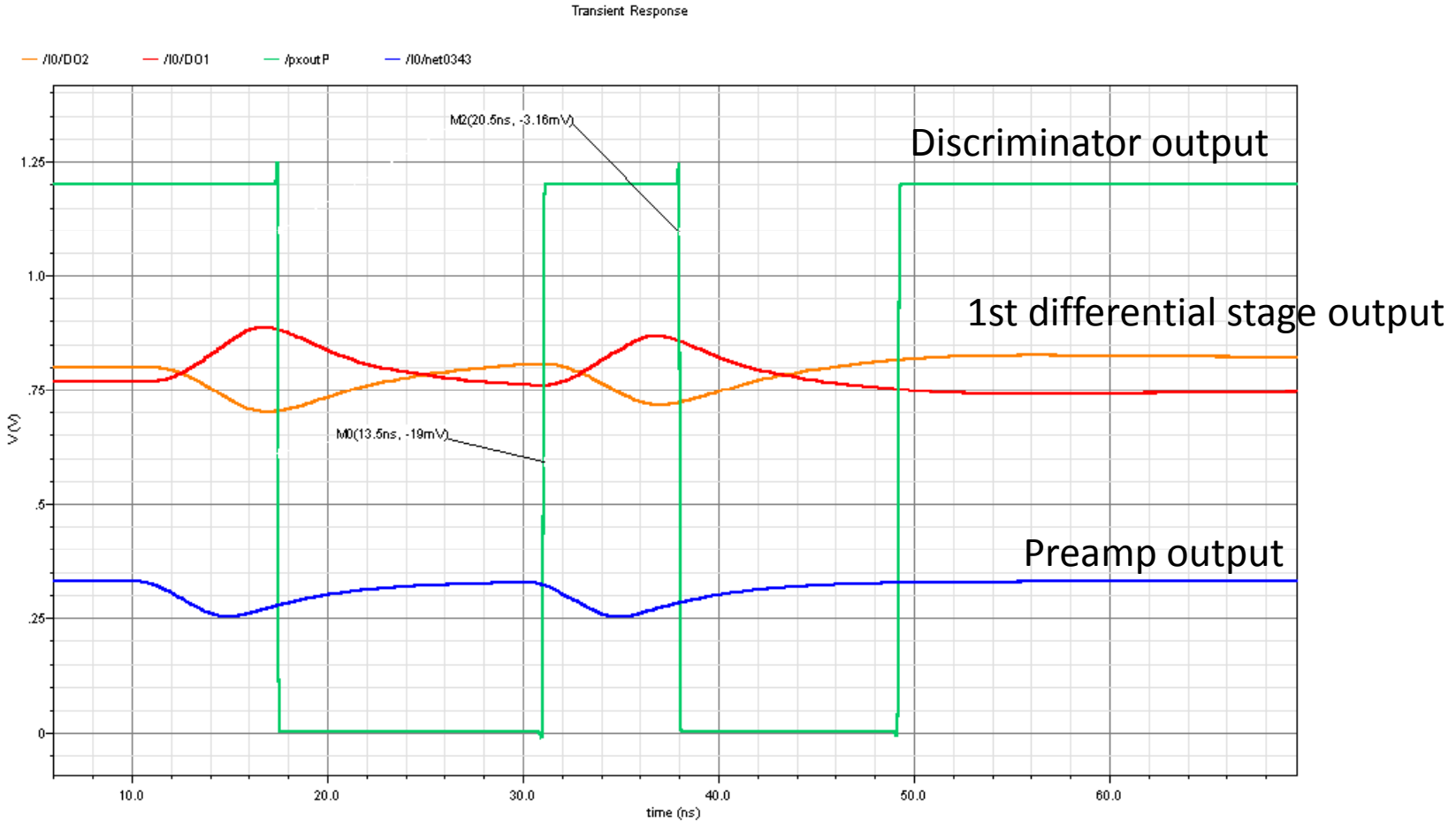
Good linearity and no degradation of peaking time up to 4fC (1,1.2, 3, & 4fC signals)



Differential signal as seen by comparator input

threshold

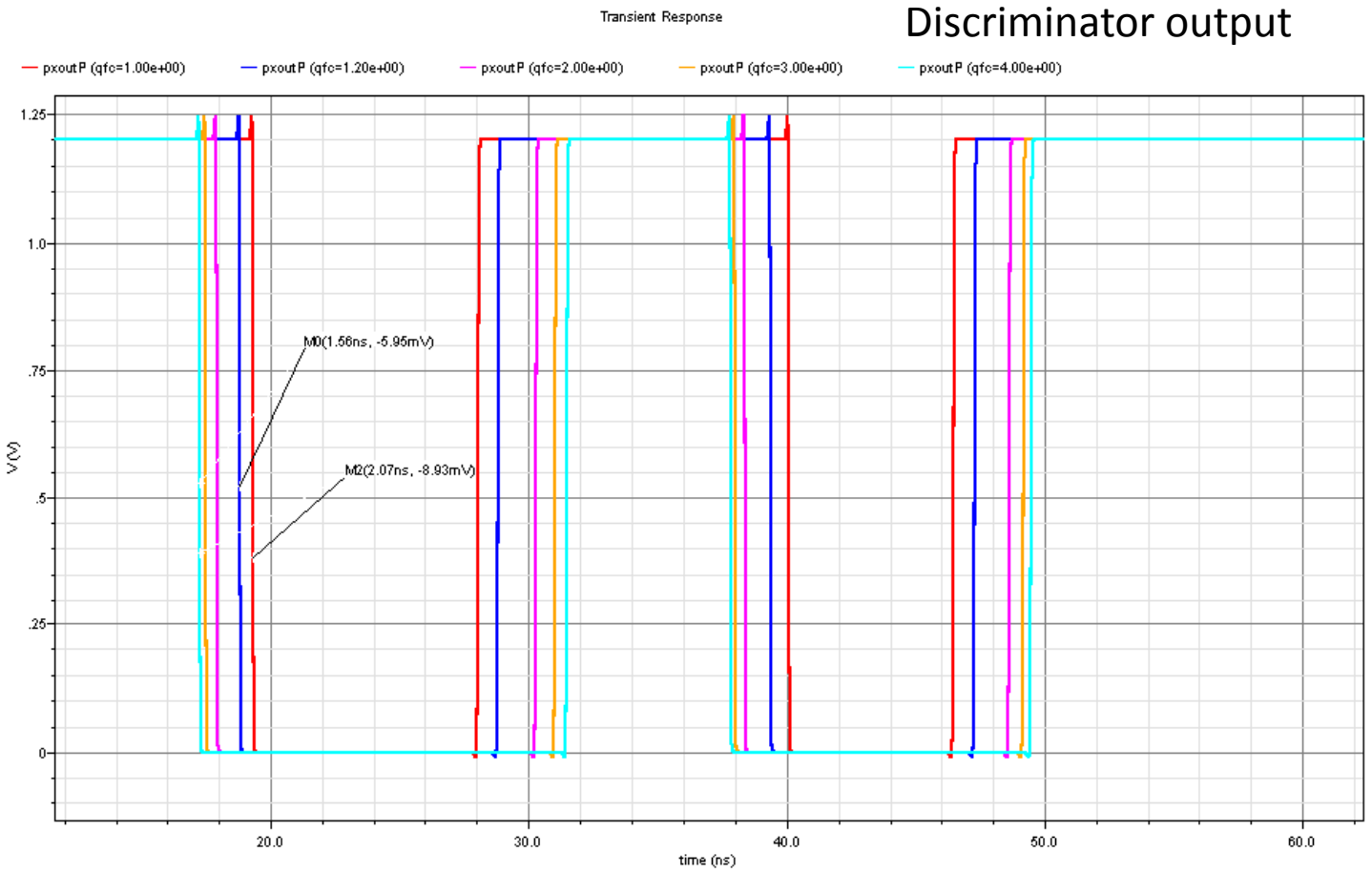
Transient simulation



Double pulse resolution; 2 signals 3fC in 20ns distance at 0.7fC threshold

Transient simulation

Discriminator output

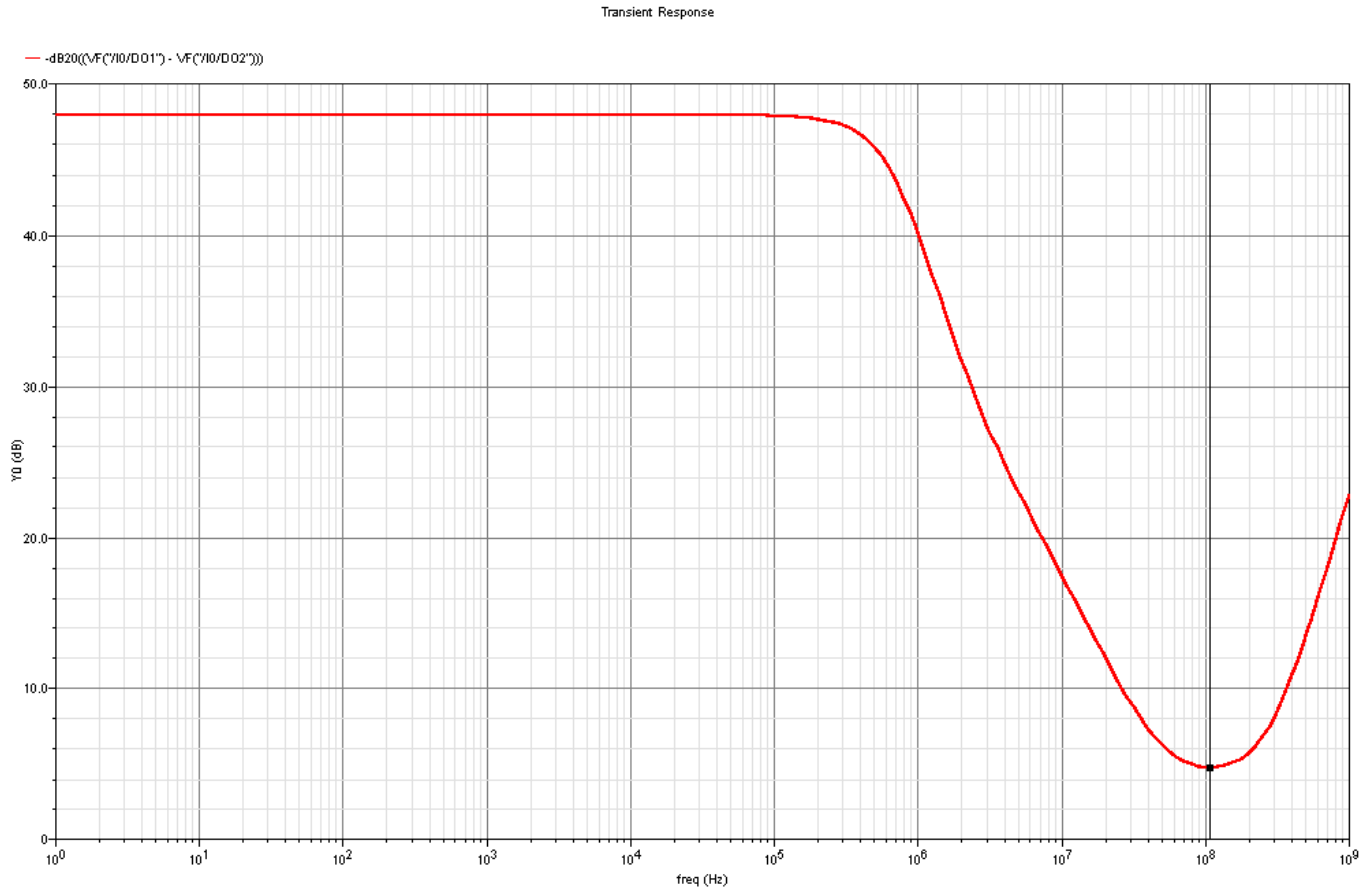


Walk; 1.5ns for 1.2 and 4fC (0.7fC threshold)

Walk; 2ns for 1 and 4fC (0.7fC threshold)

Pulse width; 8 to 14ns (1 to 4fC)

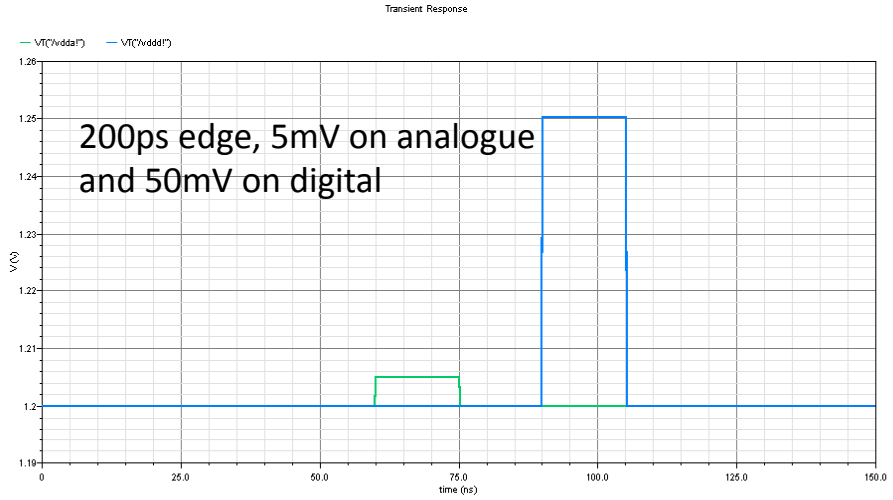
PSRR (discriminator differential input)

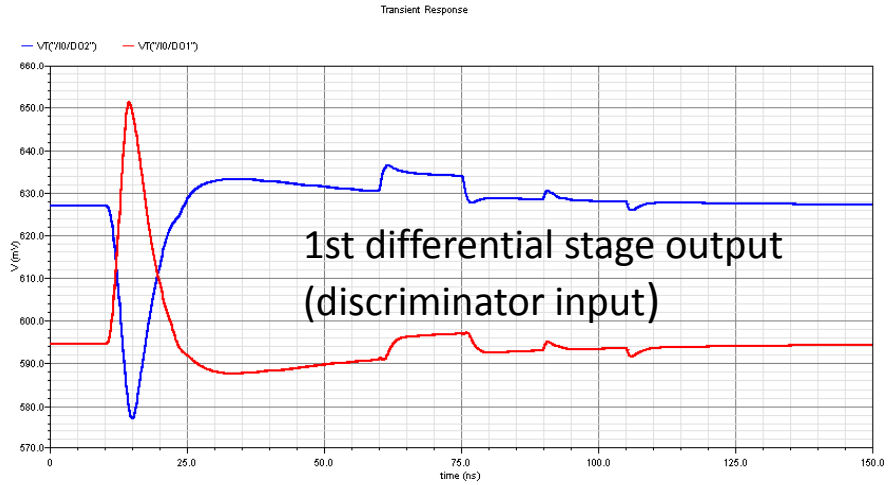


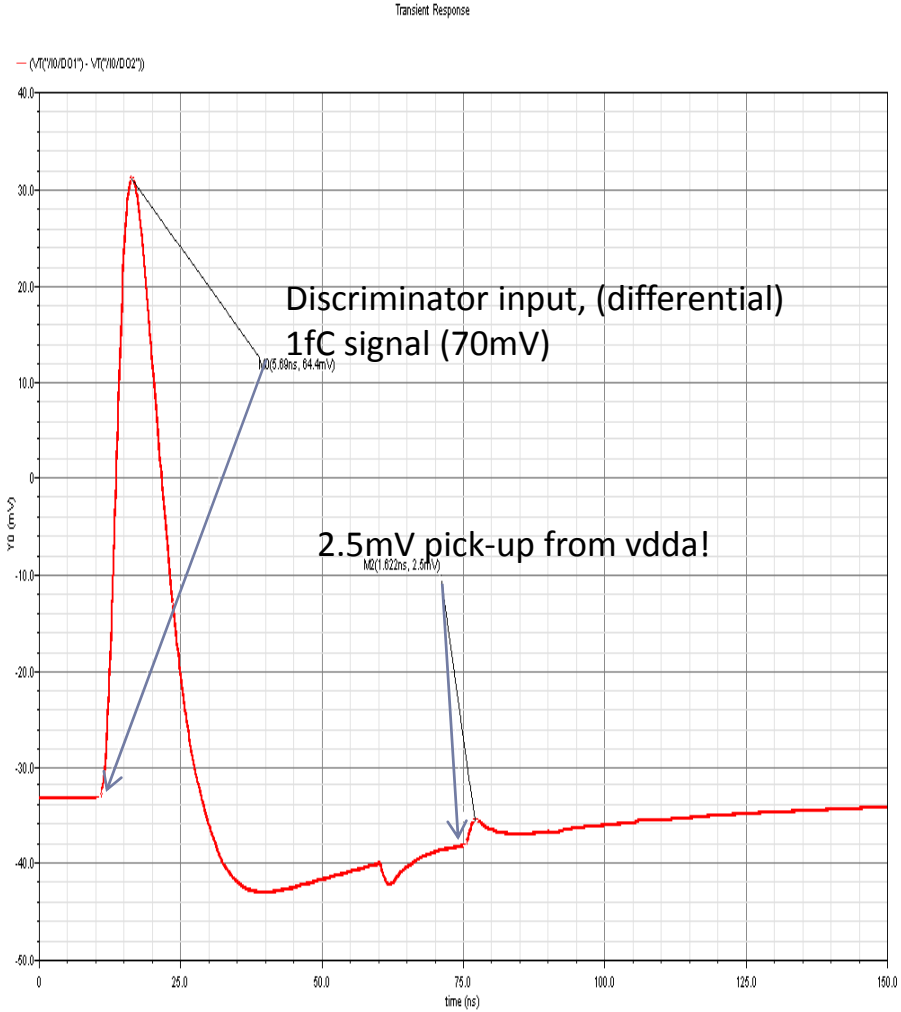
Low and medium frequencies; 48dB, degrading after 1MHz

Worst case; 2dB at 100MHz (5dB for standard layout NMOS)

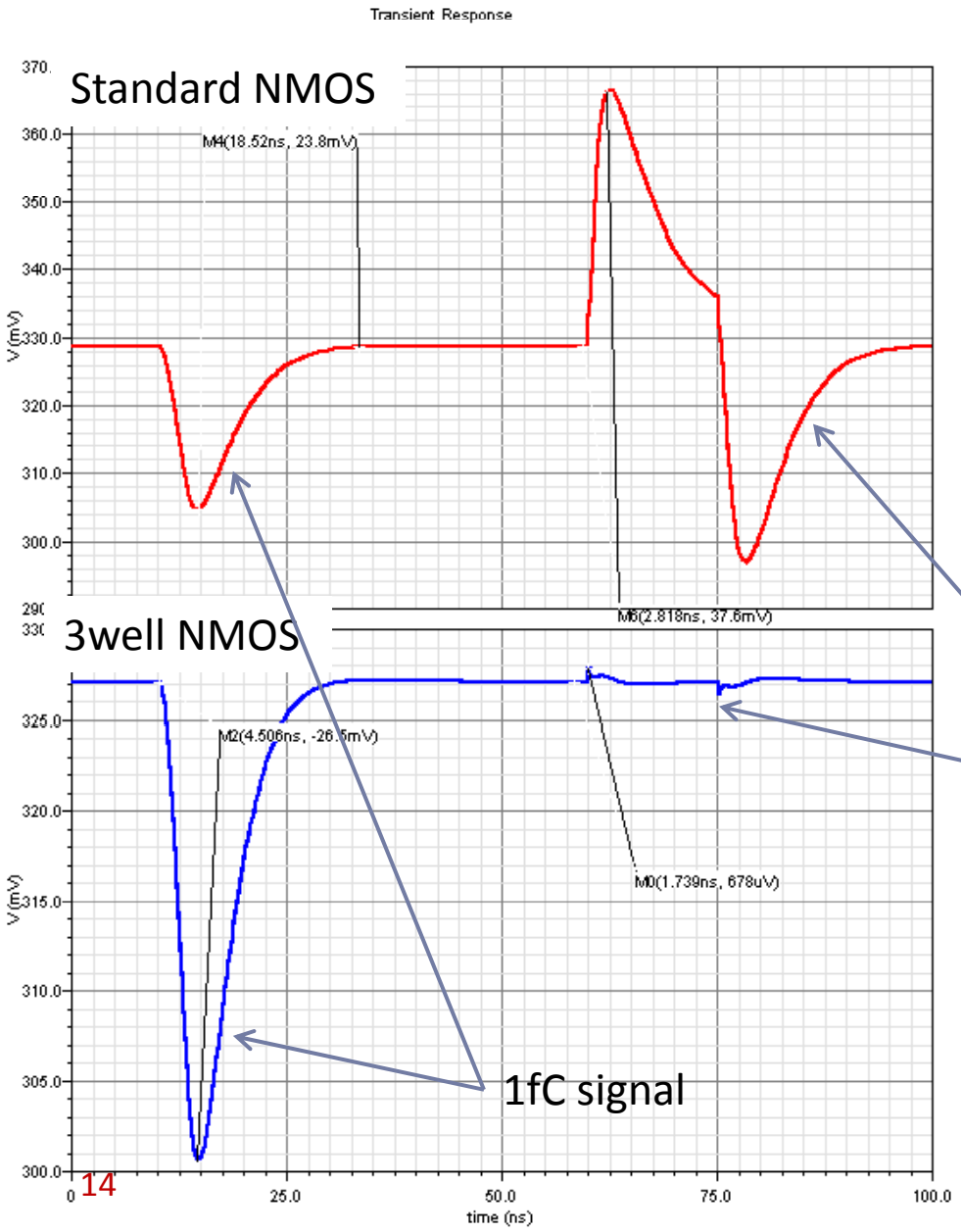
PSRR


Transient Response
VT("/vddal") VT("/vdddl")
200ps edge, 5mV on analogue
and 50mV on digital
V (V)
time (ns)


Transient Response
VT("/I10/DO2") VT("/I10/DO1")
1st differential stage output
(discriminator input)
V (mV)
time (ns)


Transient Response
(VT("/I10/DO1") - VT("/I10/DO2"))
Discriminator input, (differential)
1fC signal (70mV)
M0(5.89ns, 64.4mV)
2.5mV pick-up from vdda!
M2(1.822ns, 2.5mV)
Y0 (mV)
time (ns)

Input stage, standard versus 3well NMOS



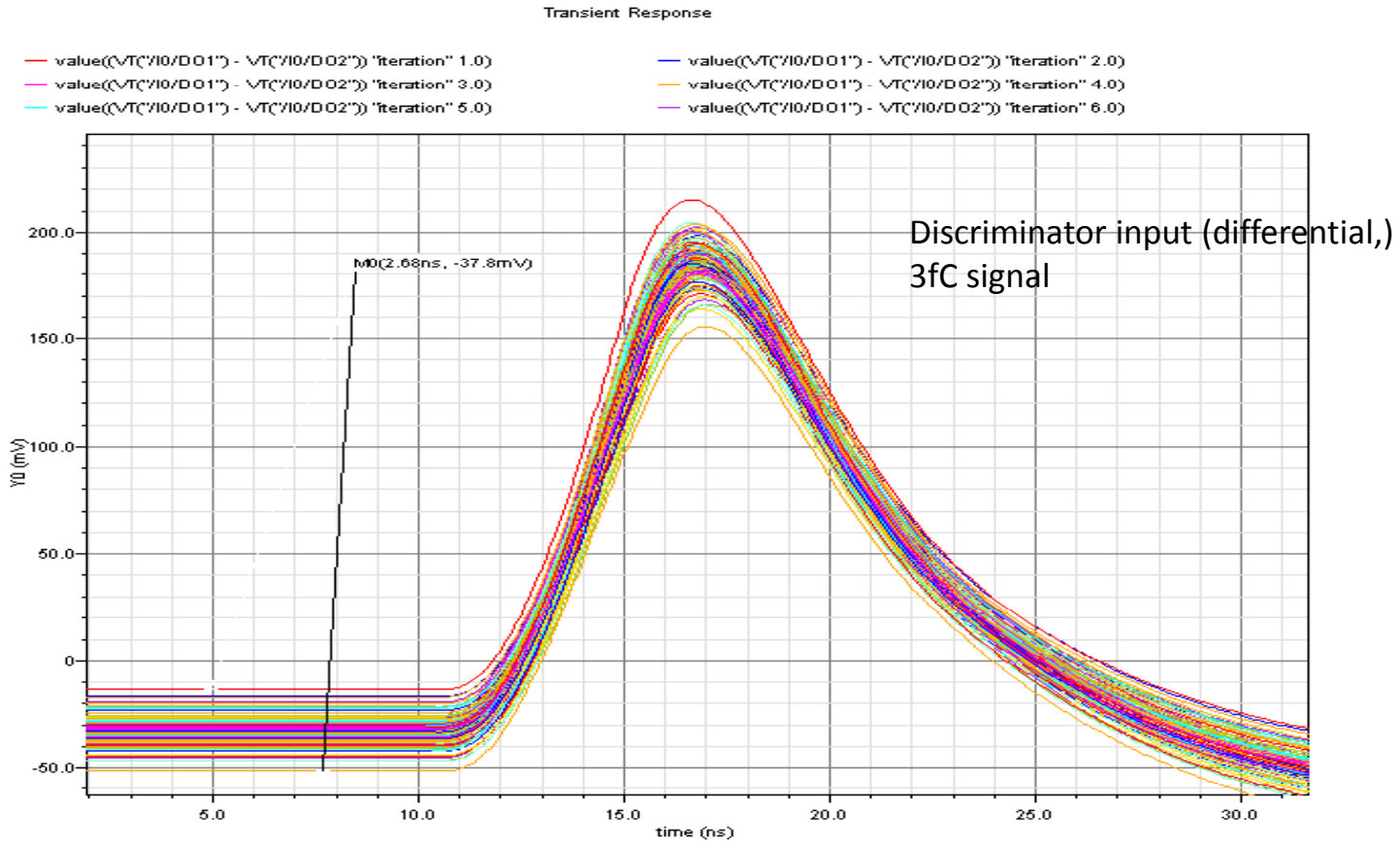
Comparison between standard and 3well NMOS susceptibility to substrate pick-up

5mV injection to substrate

Mismatch (no TRIM DACs)

3fC signal, mismatch 6mV RMS (0.1fC RMS) → minimum threshold without trimming 0.7fC

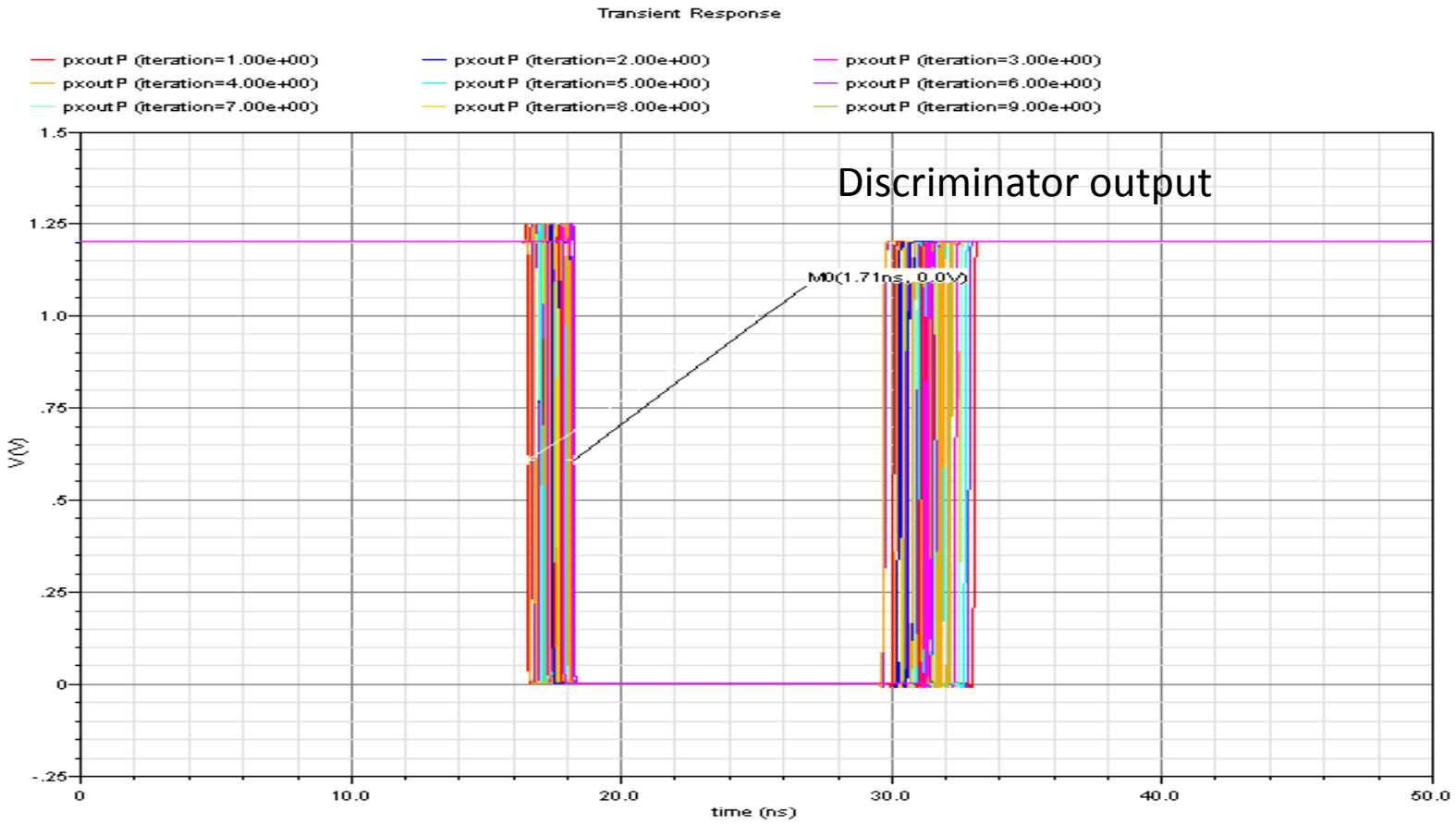
Assuming 5-bit TRIM DAC with 50mV range the mismatch can be minimized down to 1.5mV pk-pk (0.25mV RMS)



Discriminator input (differential,)
3fC signal

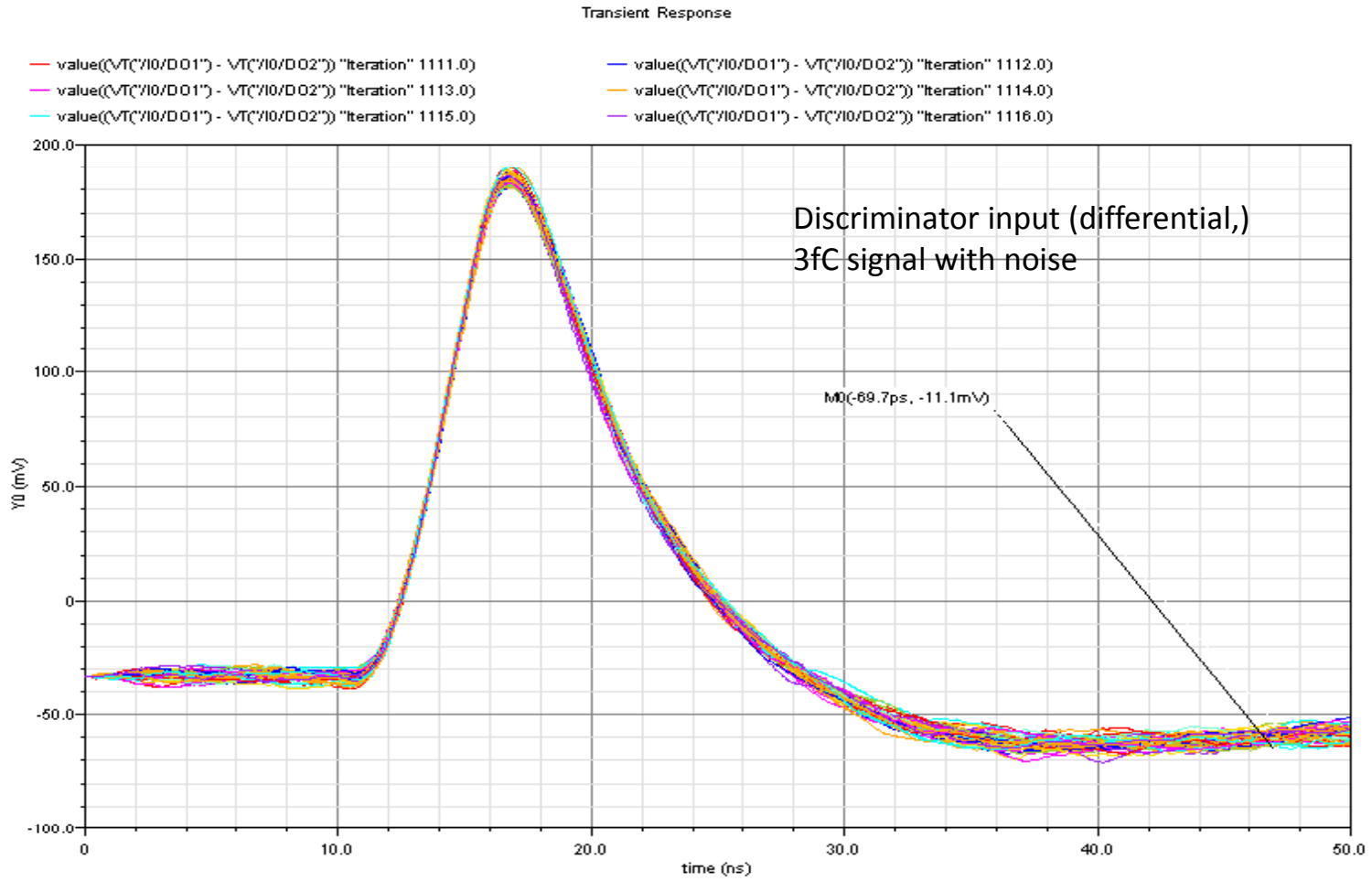
Mismatch (no TRIM DACs)

3fC signal, mismatch 6mV RMS, 300ps RMS (1.7ns pk-pk)



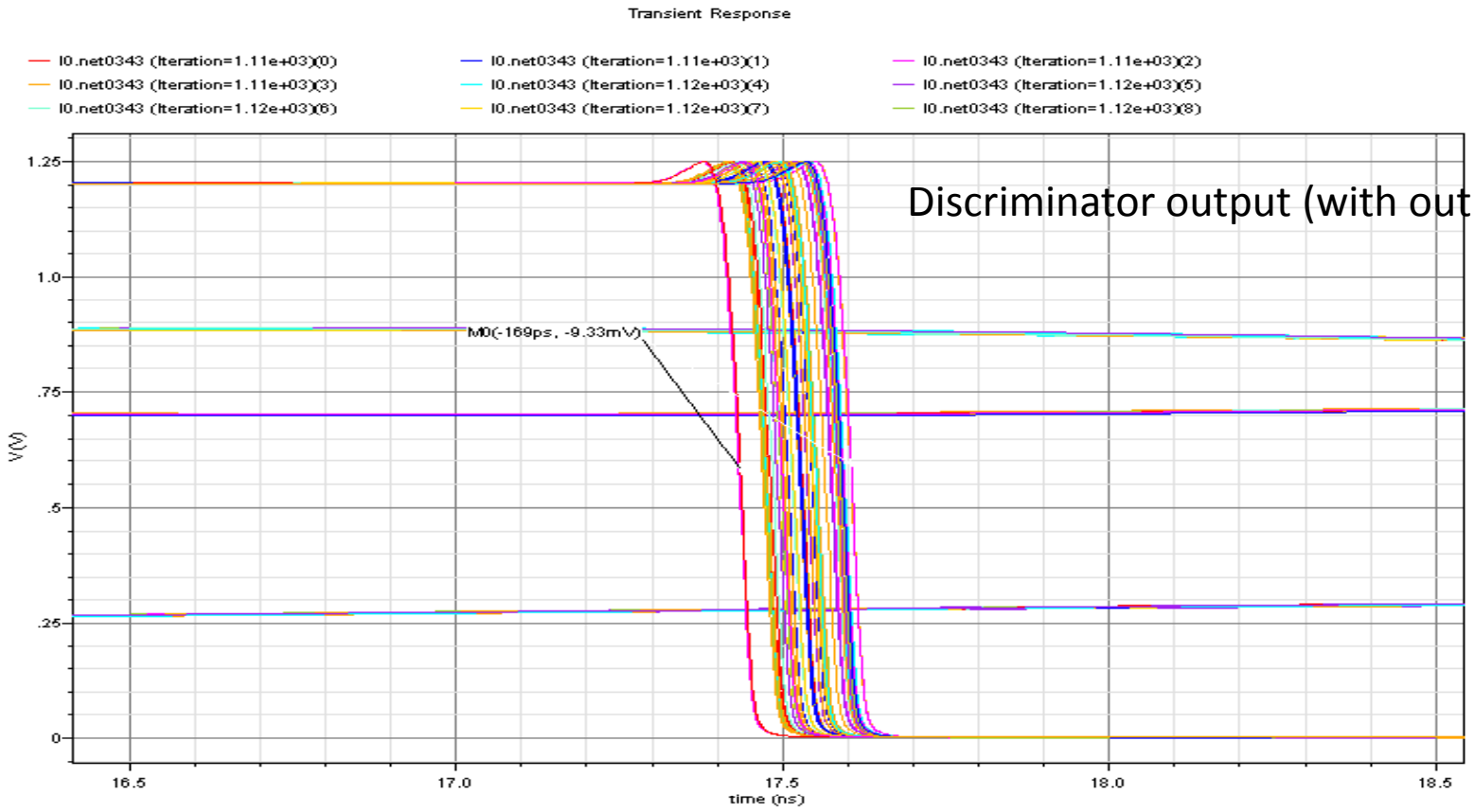
Noise & Jitter (transient noise simulation)

3fC signal, noise ~2mV RMS, → ~180e- RMS



Noise & Jitter (transient noise simulation)

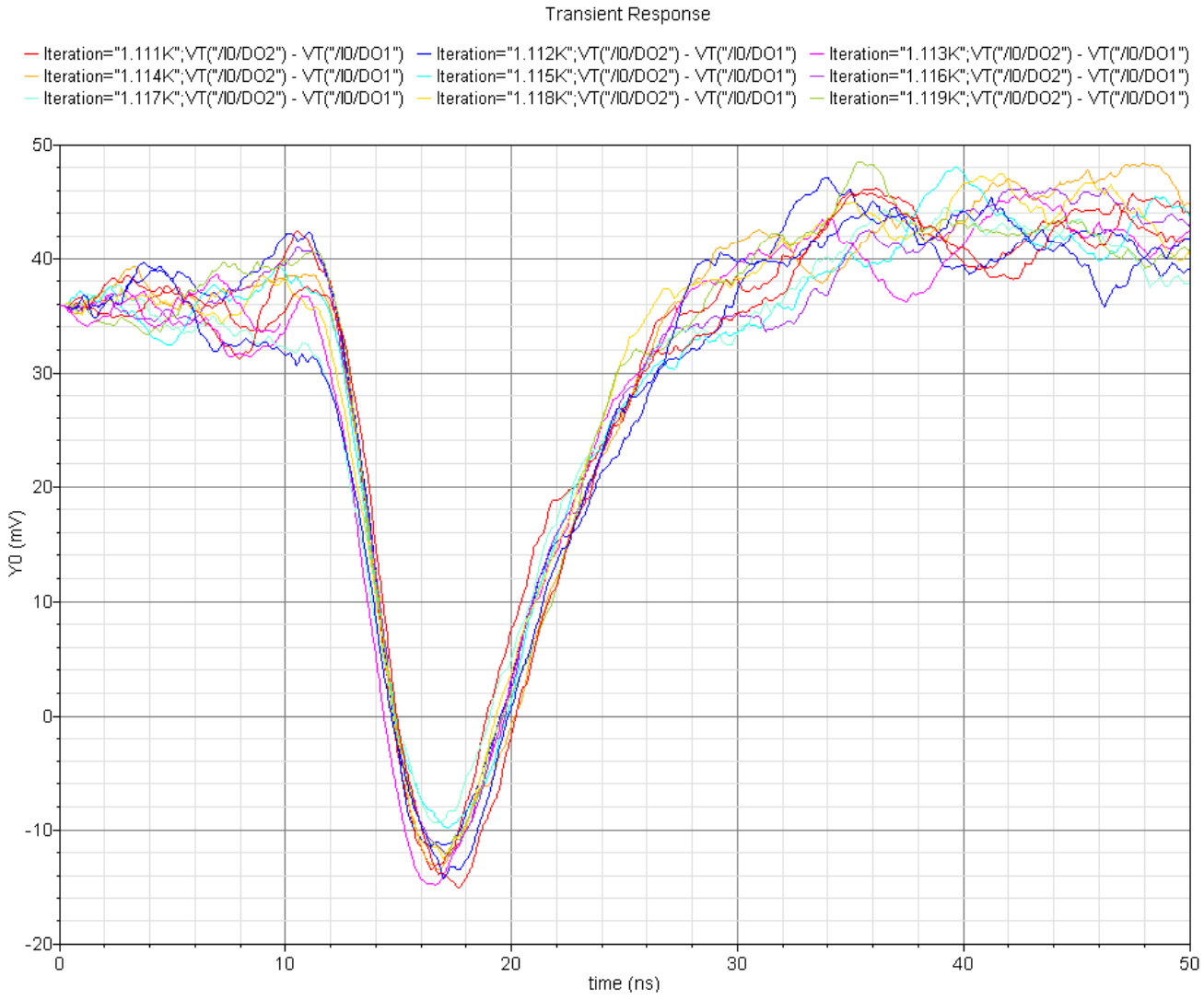
3fC signal, noise ~180e- RMS → jitter 30ps RMS (160ps pk-pk)



Discriminator output (with output jitter)

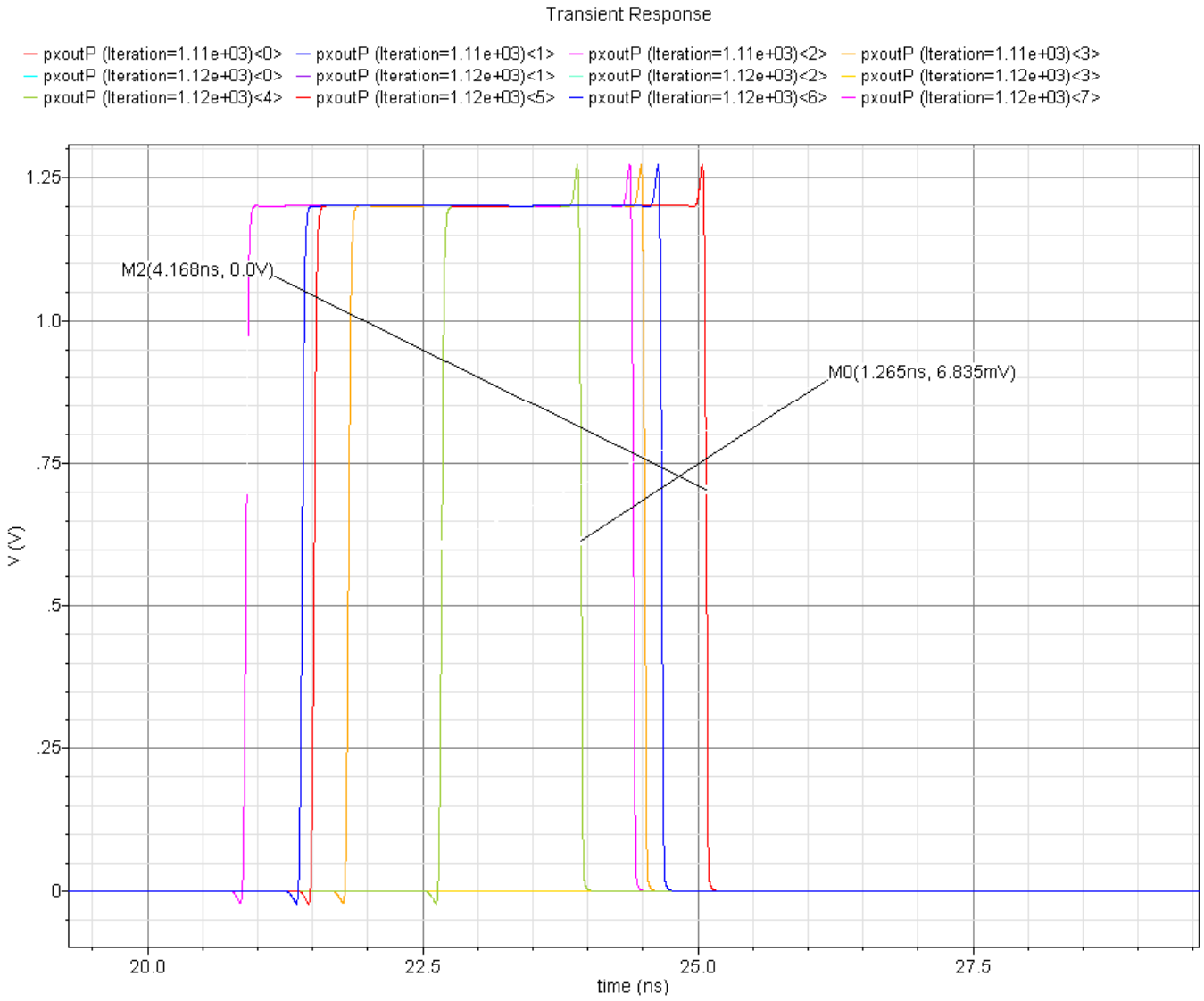
Crossing the threshold

0.7fC signal at 0.7fC threshold; noise triggering (~180e- ENC)



Crossing the threshold

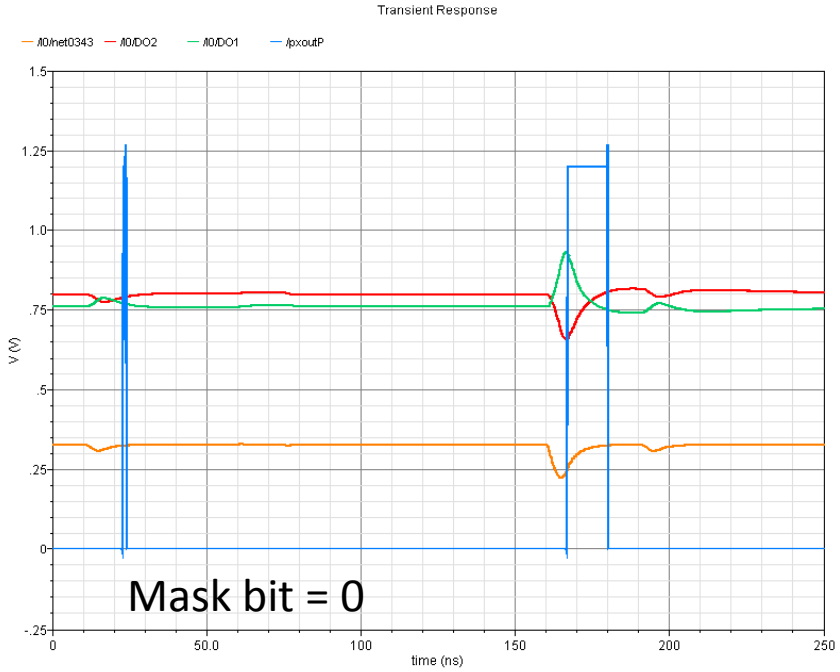
0.7fC signal at 0.7fC threshold; noise triggering (5 triggers out of 10, 1.2 to 4ns width)

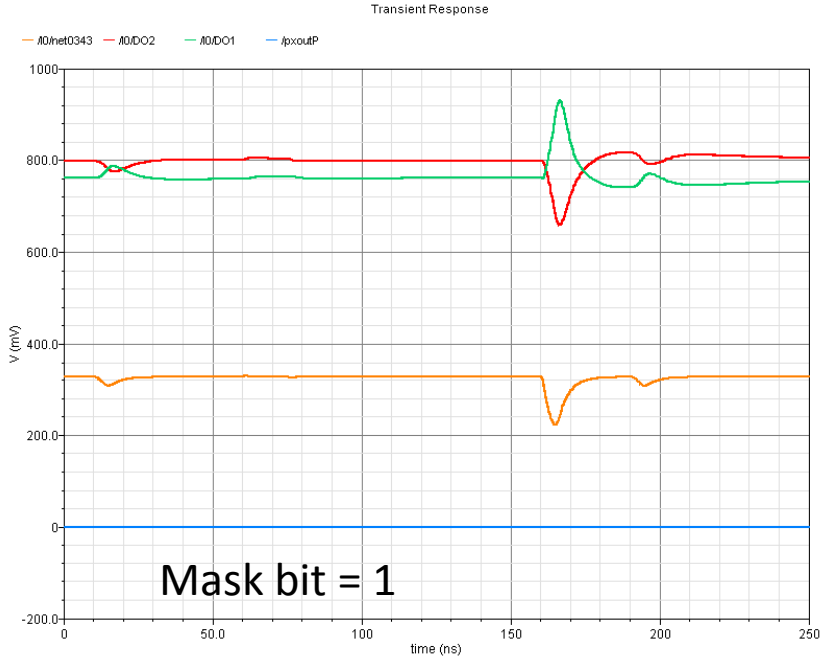


Calibration and mask register

Two D flip-flops per pixel (on top level all D flip-flops connected in one serial register)

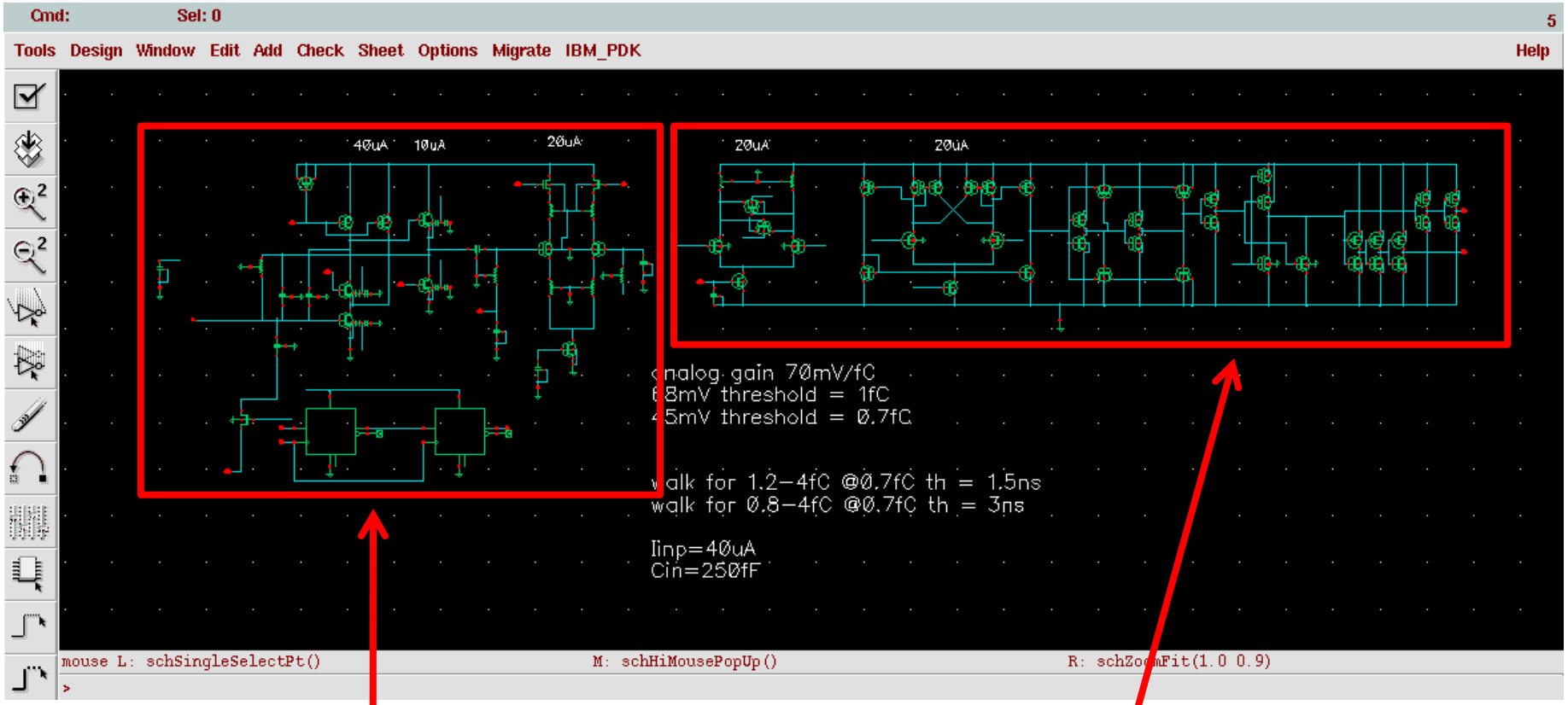
- 1st bit connect Calibration input (20fF capacitor) to common calibration line (1 = CAL LINE connected)
- 2nd bit for masking the output (OR logic – 1 block, / 0 – pass)





Separation of analogue and digital part

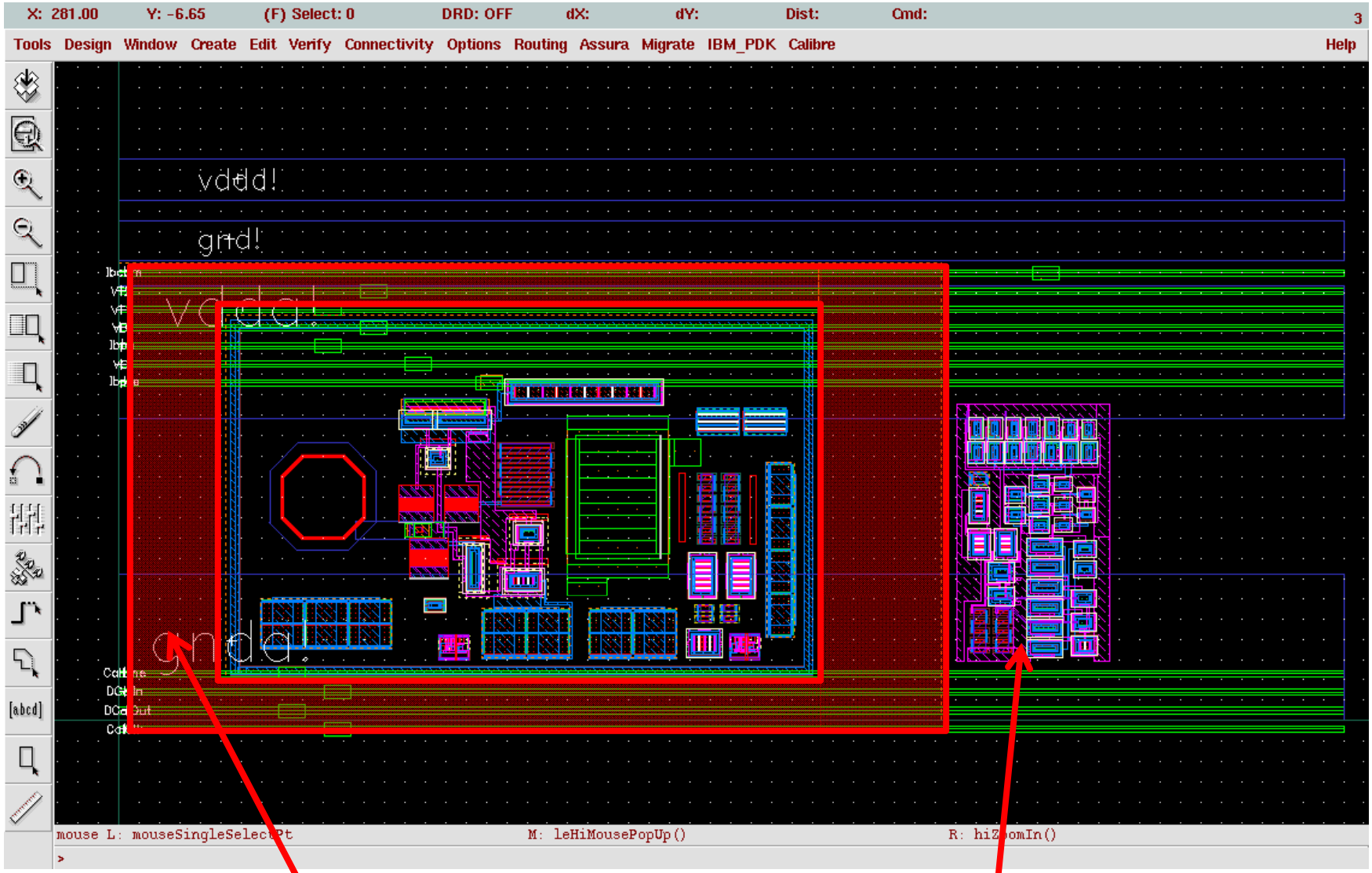
2 domains of power supply and gnd on pixel



Analog vdda and gnda, all NMOS in preamplifier with 3well layout

Digital vdd and gnd

Separation of analog and digital domain

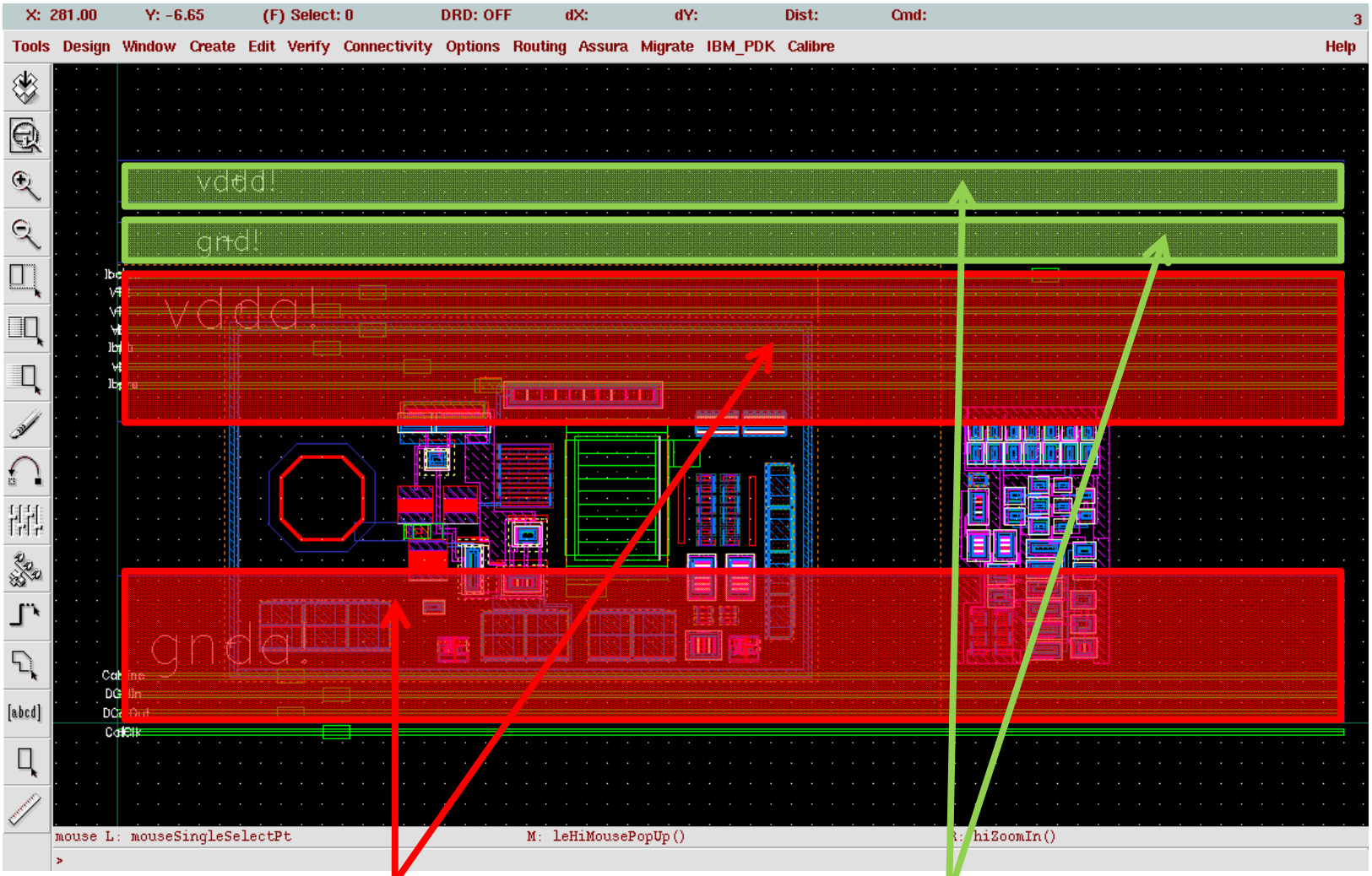


MOAT separation of analogue and digital substrate (~500 Ω)

Digital part

Separation of analogue and digital power supply

Power distributed with last metal MA (7mΩ/sq)



35um width for analog (70uA/pixel)

10 um width for digital (~120uA for comparator + TL driver)