Bus operation, receiver, DALC design review

bus operation

Receiver

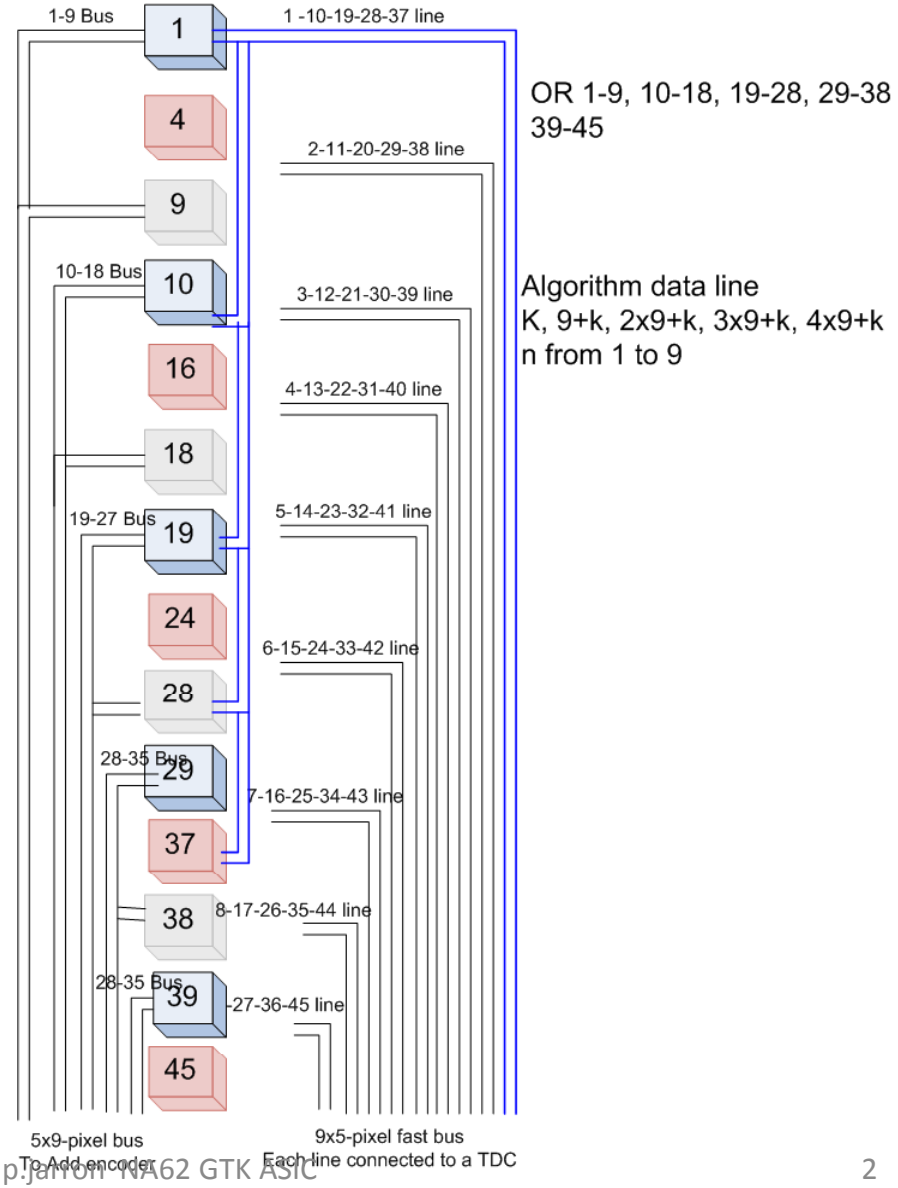
DALC

Bus system architecture

Address bus lines **Hit data bus lines**

Encoding pixel address

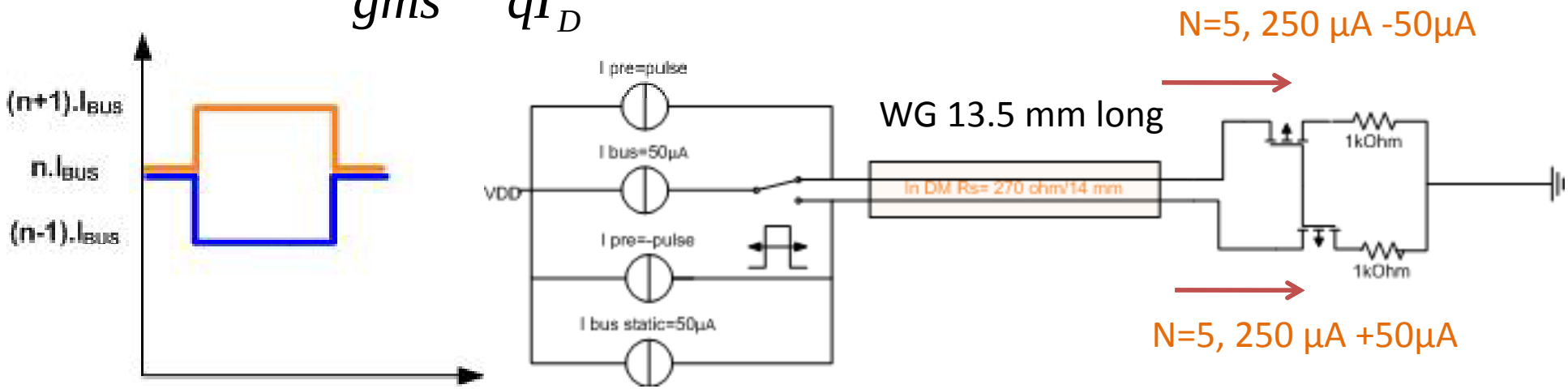
1. Pixel address is encoded by a 5x9 networked bus
2. Decreases the number of TDC from 45 to 9, factor 5 smaller
3. 1800 double-TDC bank to 360 double TDC
4. The only issue is the pile up on data line
5. No problem of pile up for address line



RF bus system principle

1. Circuit concept inspired from NINO configuration
   - NMOS input inverted to PMOS
   - Current source replaced by a switching current
   - Transmission line inserted between bias and input PMOS sources
   - Bus static current is balanced and provide receiver biasing
   - Transmission line terminated on one half of the series resistance, x4 odd impedance
   - Far end WG voltage constant, receiver output voltage ± 50 mV

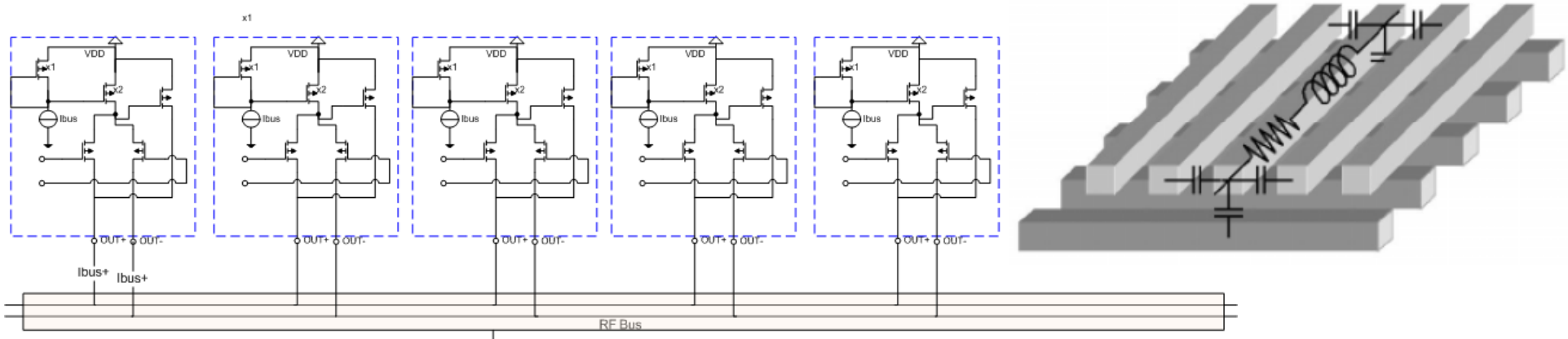
$$R_{IN}\ \min = \frac{1}{gms} \approx \frac{kT}{qI_D} \approx 160\Omega \quad for\ I_D = 250\mu A$$



Logic level | n(5 /9) switched current | cross coupled lines | current receiver

Bus architecture

- Adapted to 45 pixel column
  - Several drivers connected to the same line, 5 for data, 9 for address lines
  - Drivers consist of switching a current source when a hit occurs
  - Differential signal transported in the cross-coupled transmission line at near speed of light
  - Transmission line model defined by IBM
  - It is a non ideal transmission line, lossy, need pre-emphasis to correctly work
  - Receiver biasing is provided by the summing of driver current



Bus System timing

Bus signals are digital

Differential logic levels are:

"0" 0µA

"1" 100µA

However, in case of pile up, hits in the same data or address bus lines within 10-20 ns, caused a double bus current signal during pile up.

Address lines can pile up

State is used to decode pixel address 9 x 5 -> (1-45)

Hit data lines cannot pile up

Leading and trailing edges are the time stamp for the TDCs

In case of pile up hits are lost

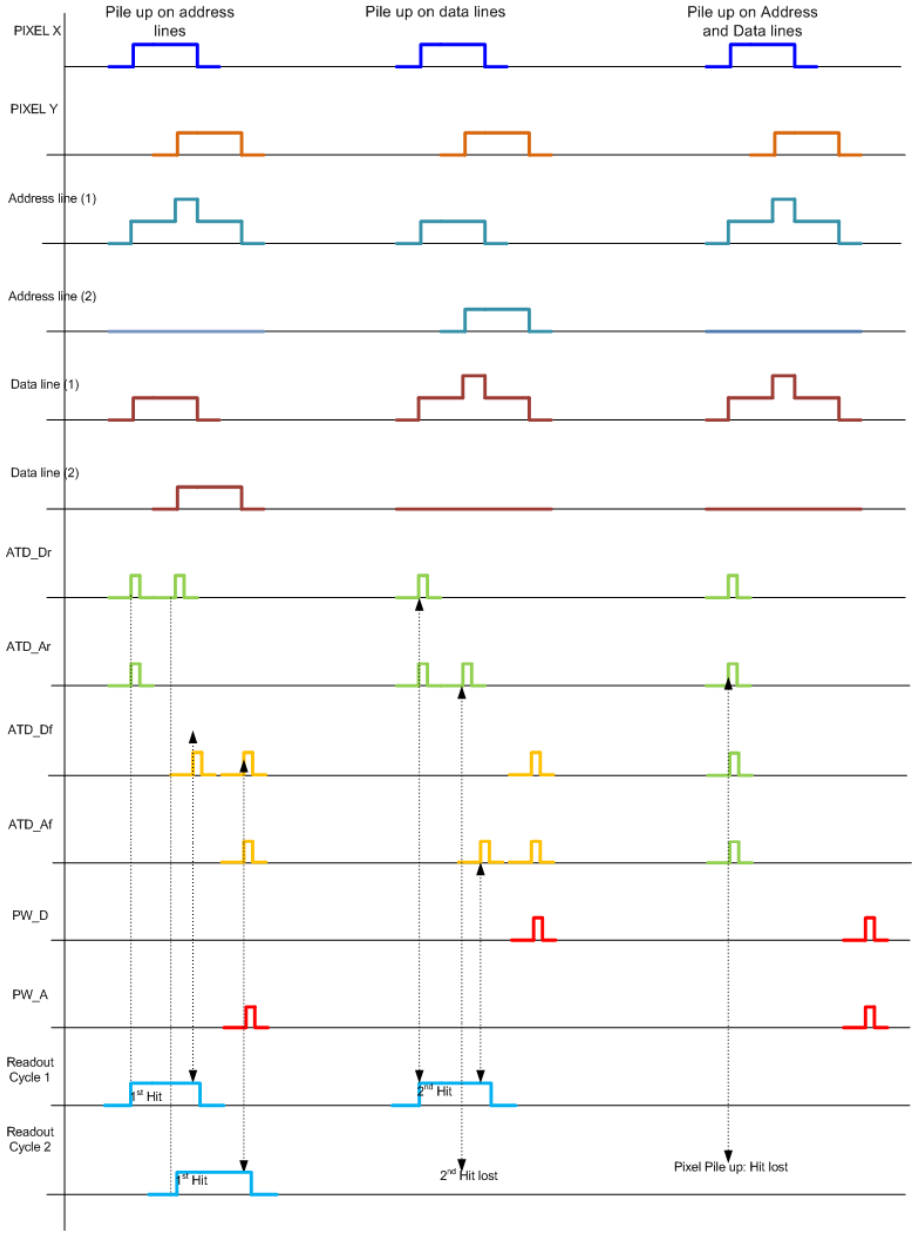
Occurrence<1%

There is an idea to detect pile up and correct, so far not yet implemented

ATD leading and Trailing are address transition detected signals are self trigger on edges that control TDC loading

A readout cycle starts from the leading edge and ends to the trailing edge

A data bus pile up corrupts the cycle and event is lost



Bus simulated with Spectre

Complete simulation of the column bus

with LM process

9 hits are generated in 80 ns simulation,

no pile up on data lines

Pile up on address lines

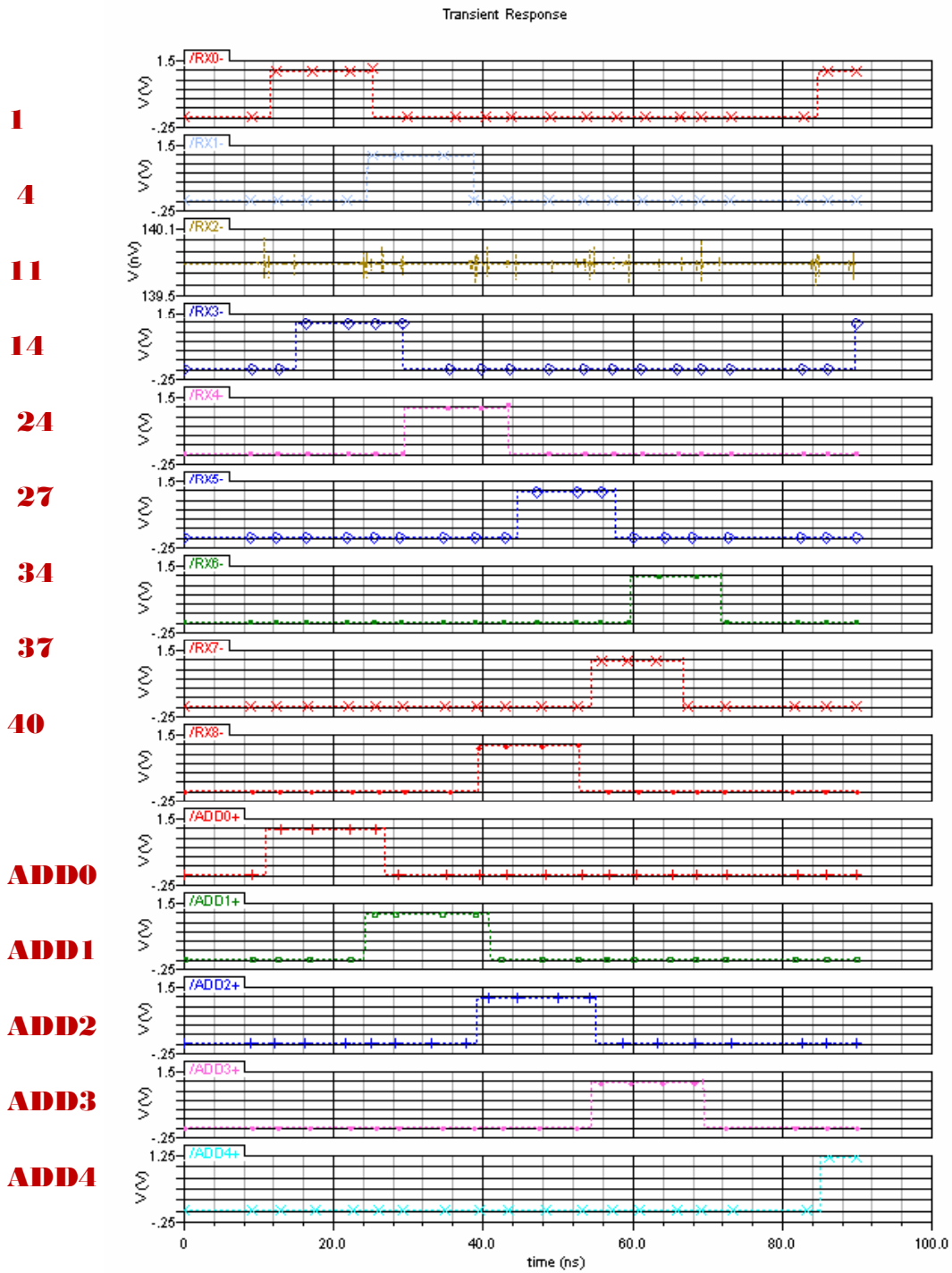
Signal are readout at receiver outputs

Results is conform to expectation

some timing adjustment should be done

Check again simulation on DM process

Simulation with data lines pile up should be tested



• DALC response

DALC circuit

At the driver and TDC inputs, signal transition should be very fast <50 ps

A dynamic asynchronous latch circuit has been developed to get this fast transition without static power.

The circuit uses positive feedback during transition to fasten edges

Positive NMOS and PMOS feedback

Steady state

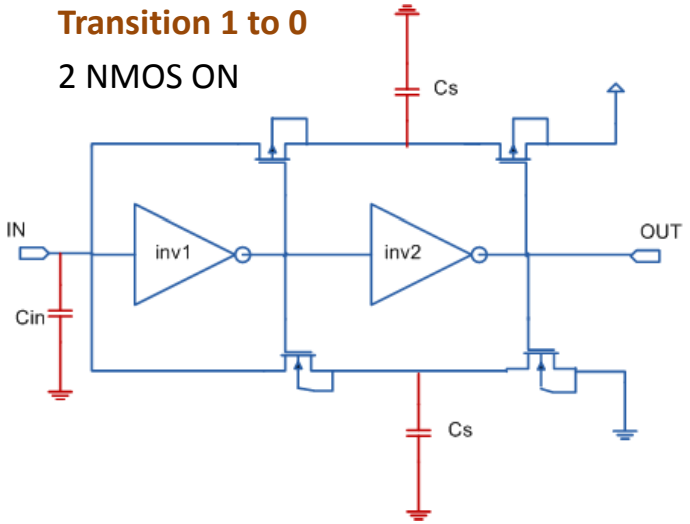
branch 1 MOS ”OFF”, 1 MOS “ON”

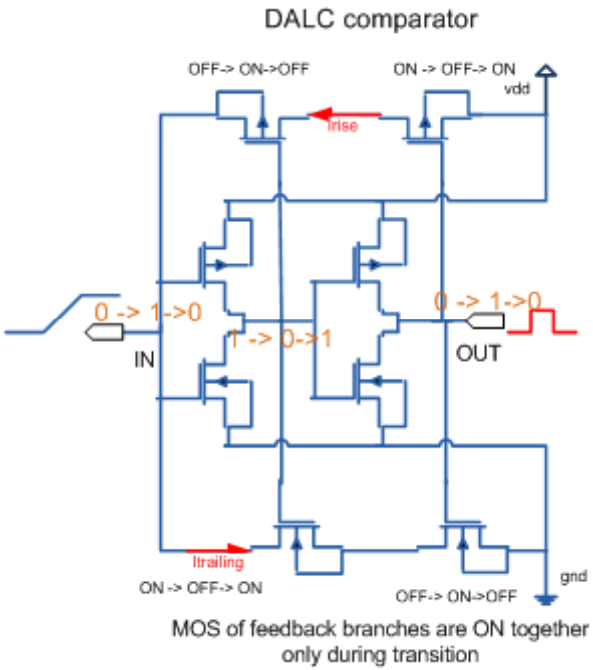
Transition 0 to 1

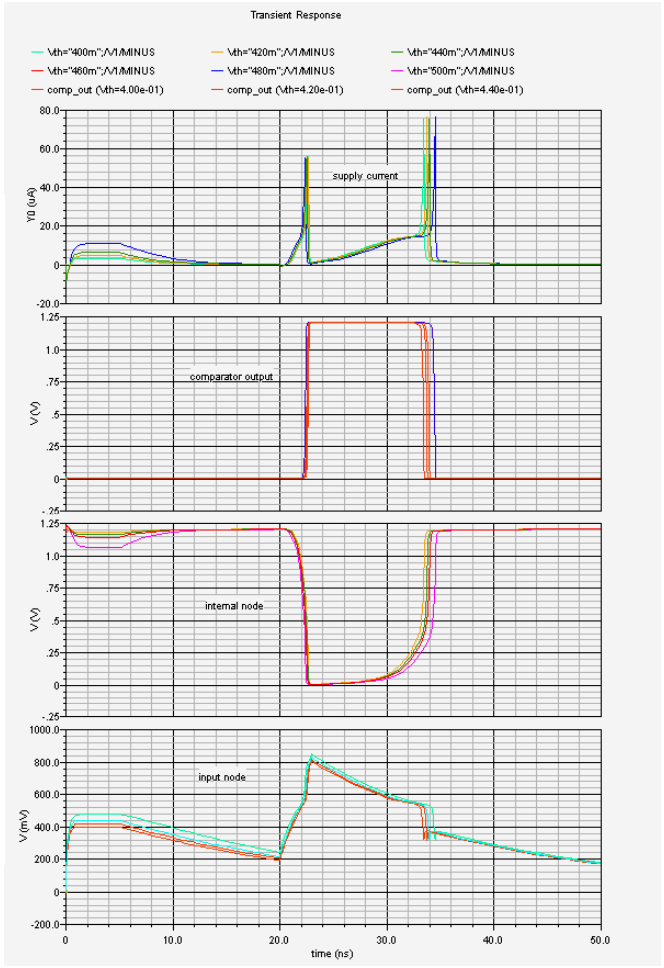
2 PMOS “ON”

Transition 1 to 0

2 NMOS ON







Receiver stage

Input tranconductance defines line termination:

250 µA about 200-250 Ω

The value is 5 times higher than odd line impedance

No reflection due to dispersive propagation

First stage output is slower than waveguide

250 ps rise time on broadband inputs.

Signal polarity controls by external signal, 0, VDD

Latency about 400 ps, mainly from the broadband stage