Simulation, design, and manufacturing tests of single-type column 3D silicon detectors

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Outline

- Introduction
- Concept of a Single-Type Column 3D detector
- TCAD simulations of a 3DSTC detector
- Fabrication tests of 3D detectors at ITC-irst
- Layout of the first batch
- Conclusion

Introduction

Technological development of 3D silicon sensors has recently been started at ITC-irst (Trento-Italy).

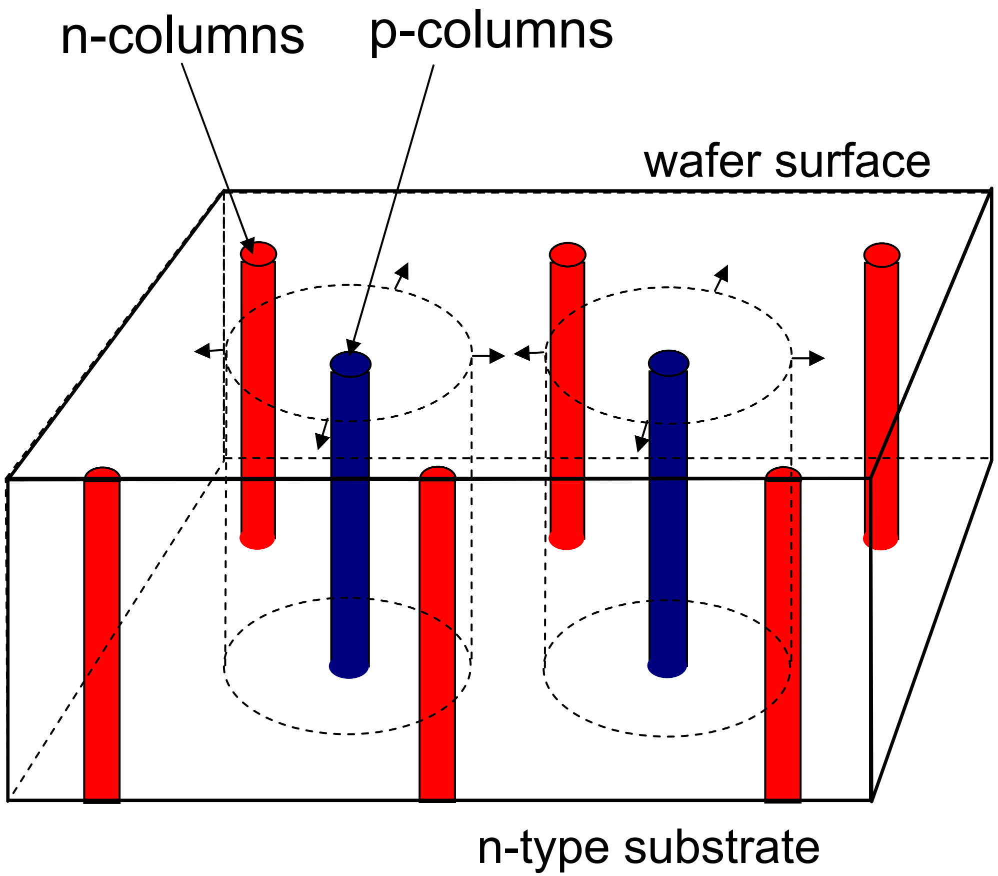
Funding support from an agreement between INFN and the Autonomous Province of Trento.

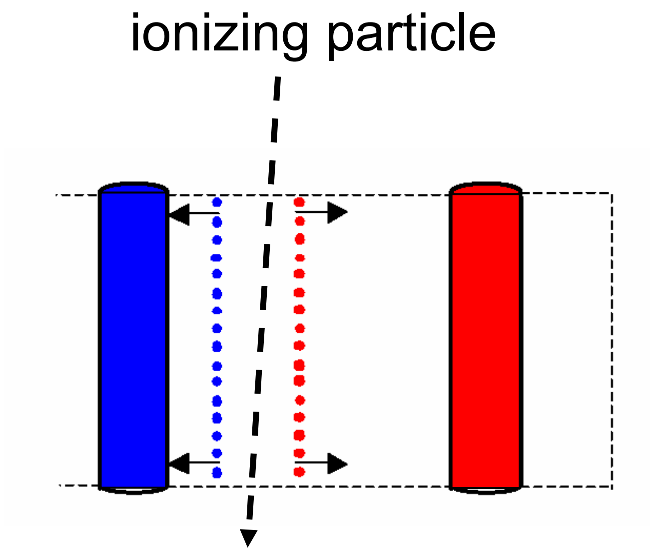
ITC-irst is also inside RD50 collaboration.

This talk describes the work carried out so far.

"Standard" 3D detectors - concept

Proposed by Parker et al. NIMA395 (1997)





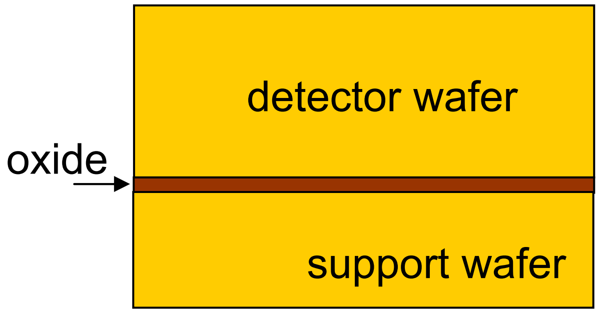
Short distance between electrodes:

- low full depletion voltage
- short collection distance

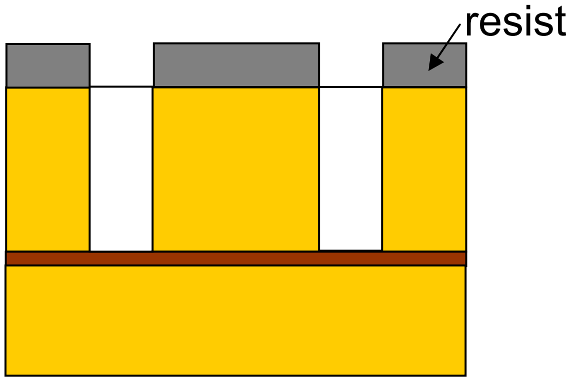
→ more radiation tolerant than planar detectors!!

“Standard” 3D detectors - fabrication

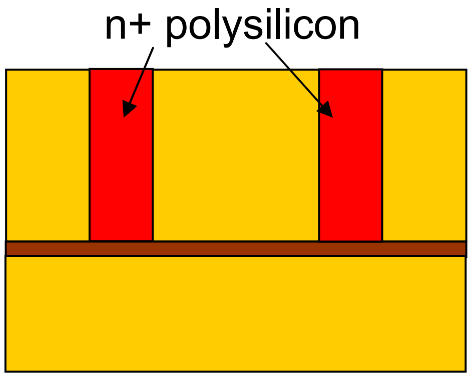
Kenney et al. IEEE TNS, vol. 46, n. 4 (1999)



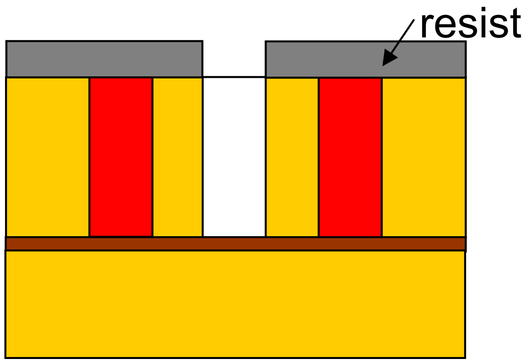
1) wafer bonding



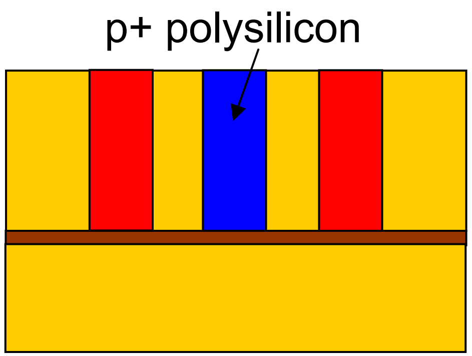
2) n+ hole definition and etching



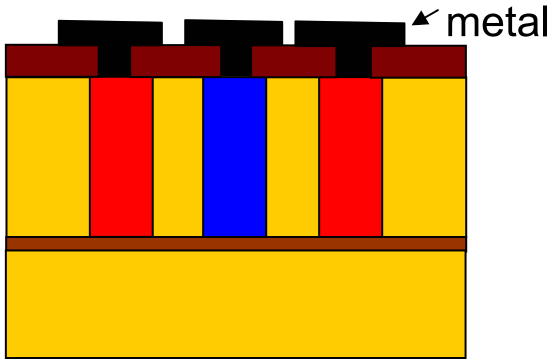
3) hole doping and filling



4) p+ hole definition and etching



5) hole doping and filling

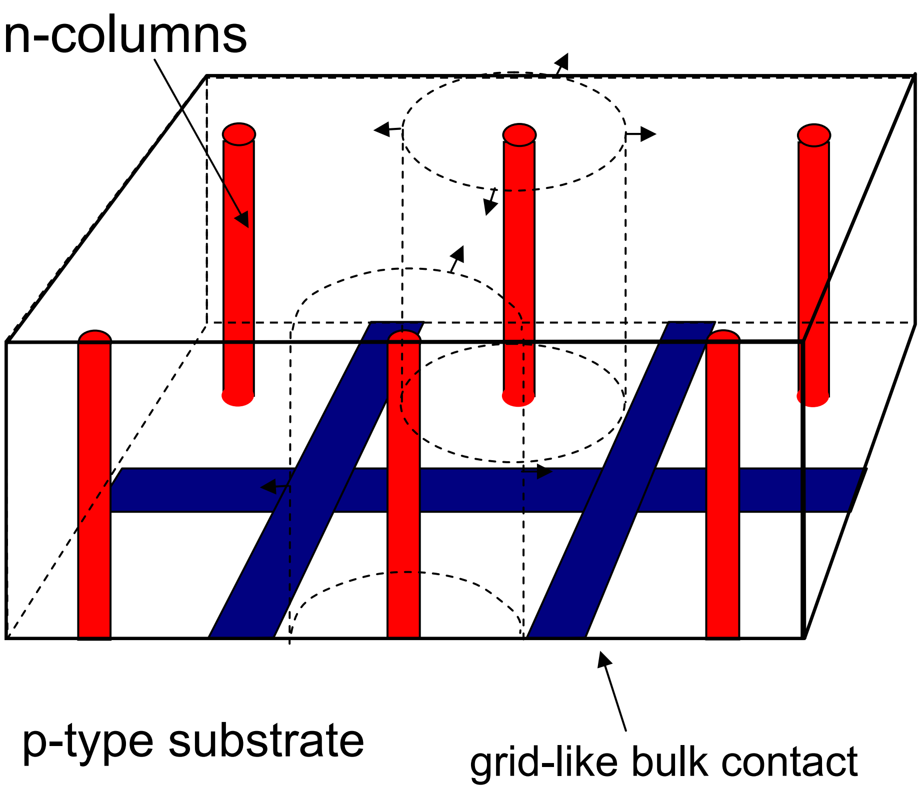


6) Metal deposition and definition

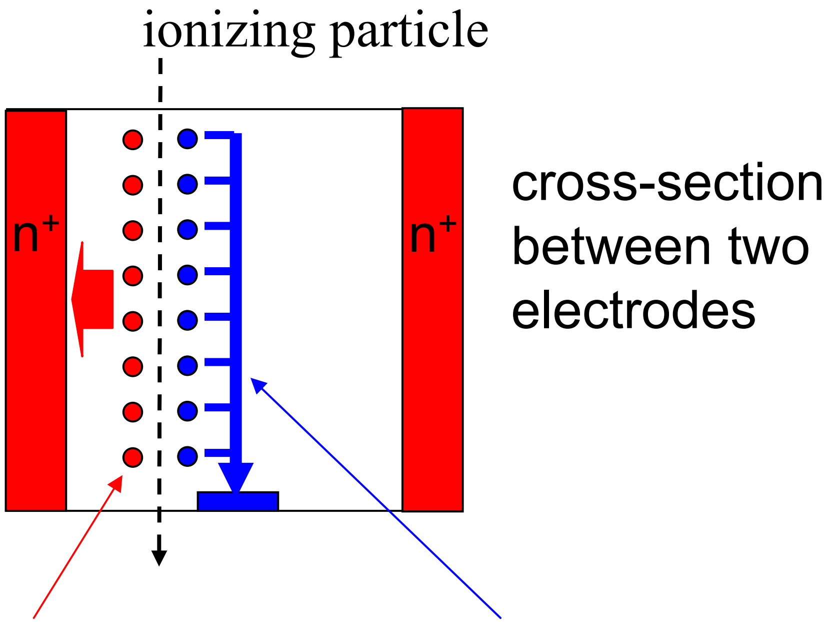
Rather challenging process for mass production!

Single-Type-Column 3D detectors - concept

Sketch of the detector:



Functioning:



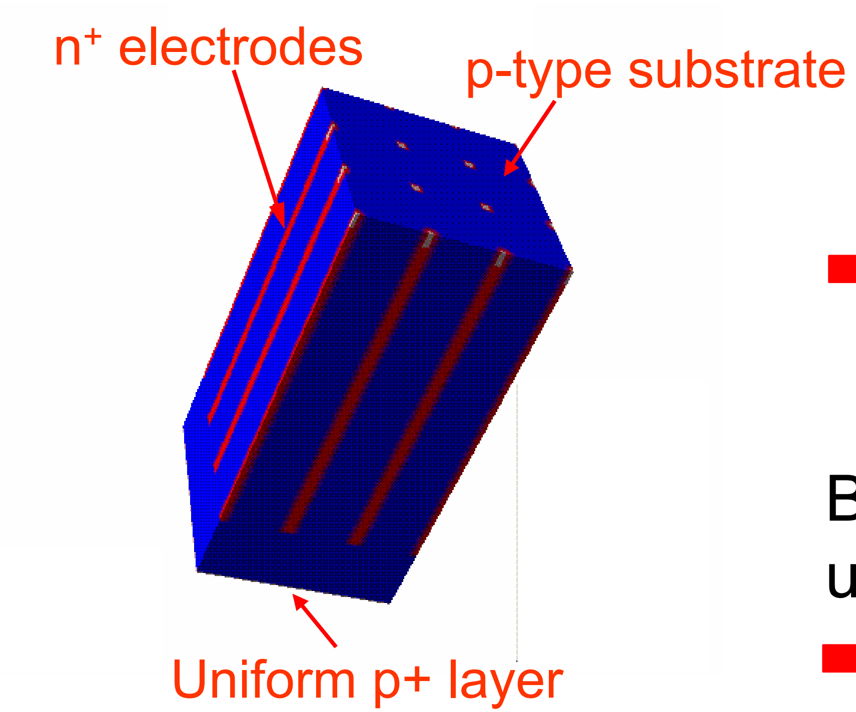
electrons are swept away by the transversal field

holes drift in the central region and diffuse towards p+ contact

Etching and column doping performed only once

3DSTC detectors - concept (2)

Further simplification: holes not etched all through the wafer



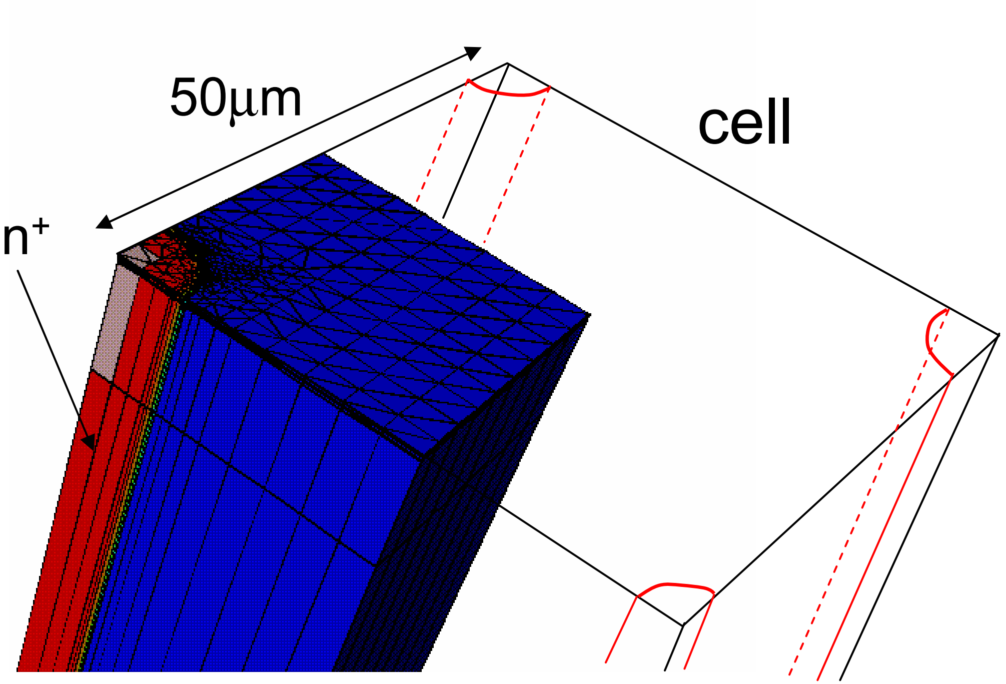
➡ No need of support wafer.

Bulk contact is provided by a backside uniform p+ implant

➡ single side process.

TCAD Simulations - static (1)

3D simulations are necessary ➡ DEVICE3D tool by Silvaco

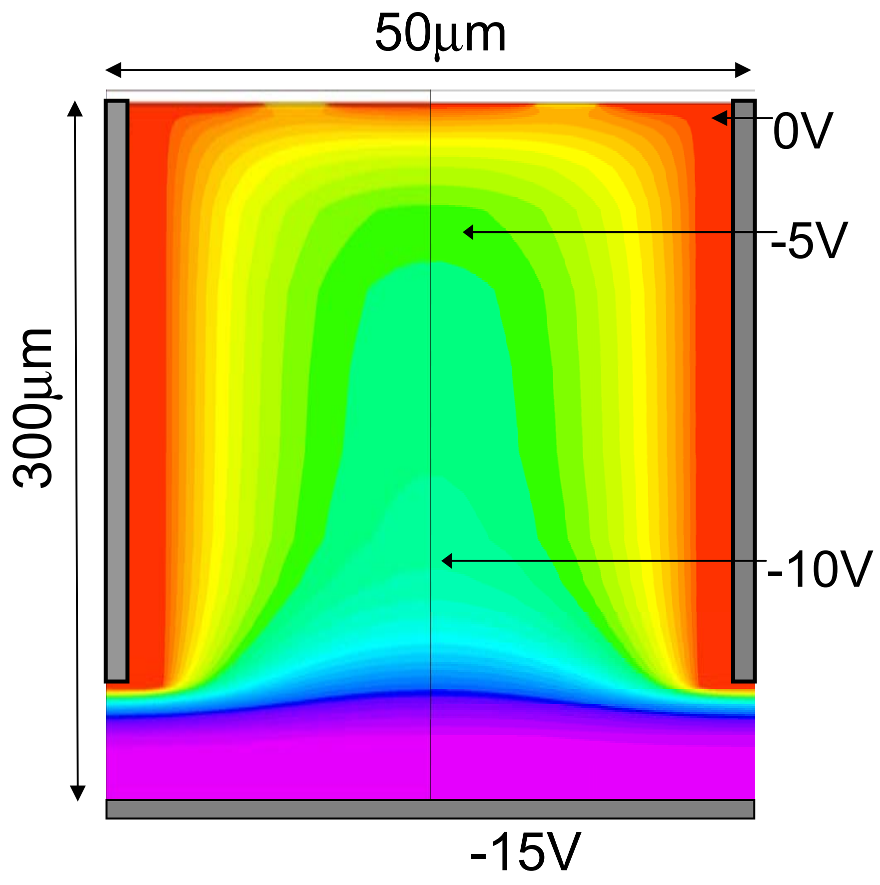


- p-type substrate
- Wafer thickness:300μm
- Holes: 5μm-radius
  250μm-deep

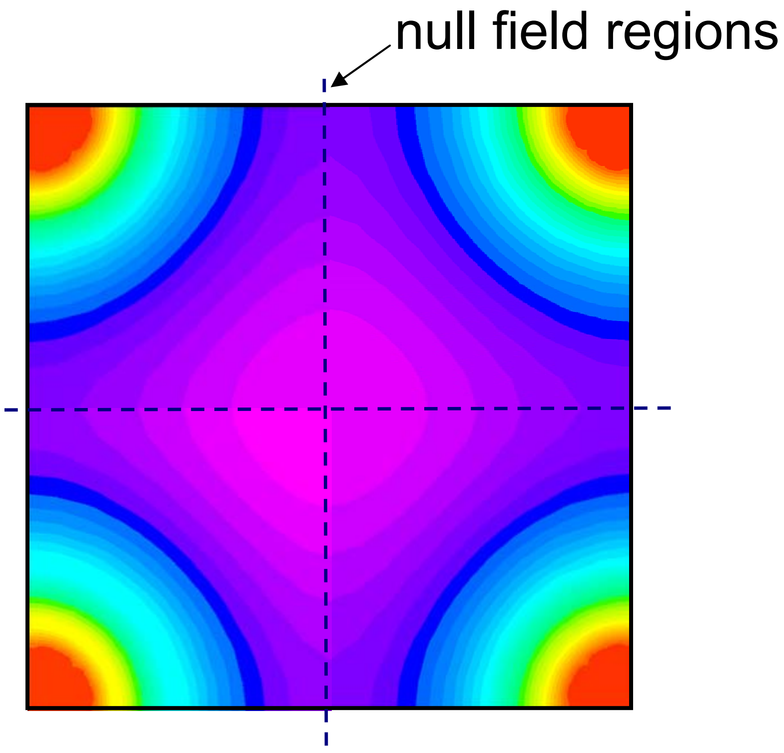
Important to exploit the structure symmetries to minimize the region to be simulated

TCAD Simulations - static (2)

Potential distribution
(vertical cross-section)

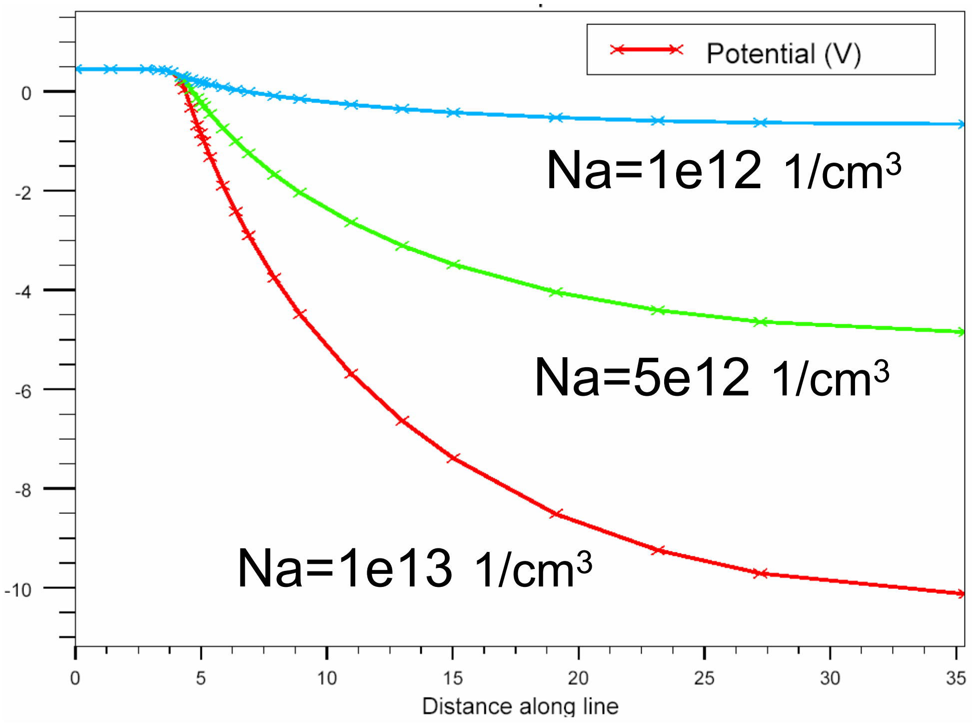


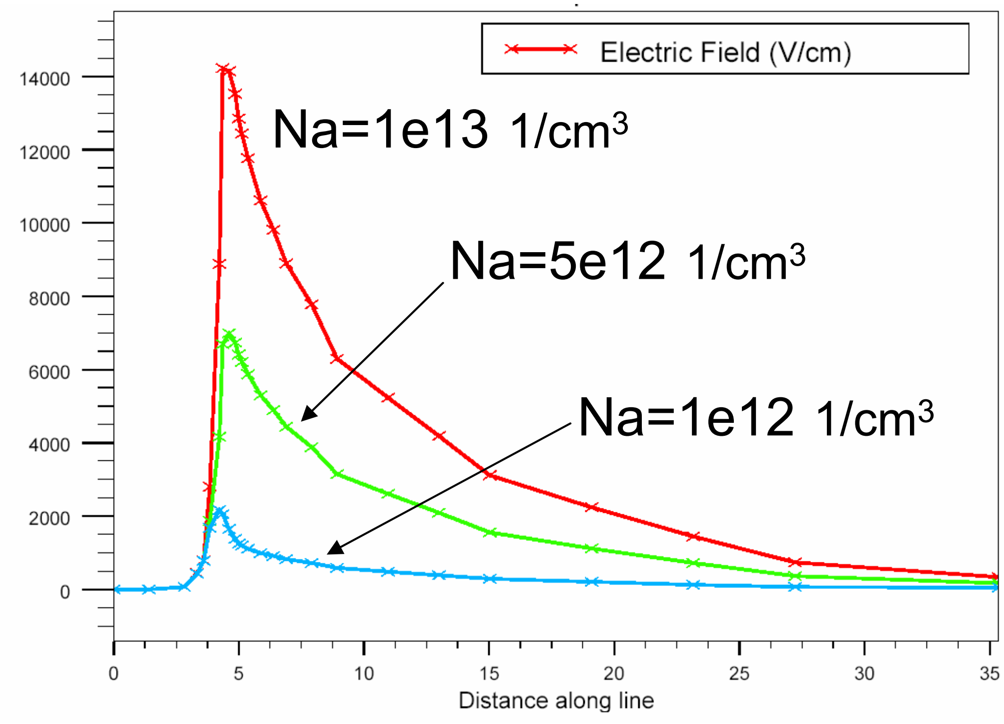
Potential distribution
(horizontal cross-section)



TCAD Simulations - static (3)

Potential and Electric field along a cut-line
from the electrode to the center of the cell



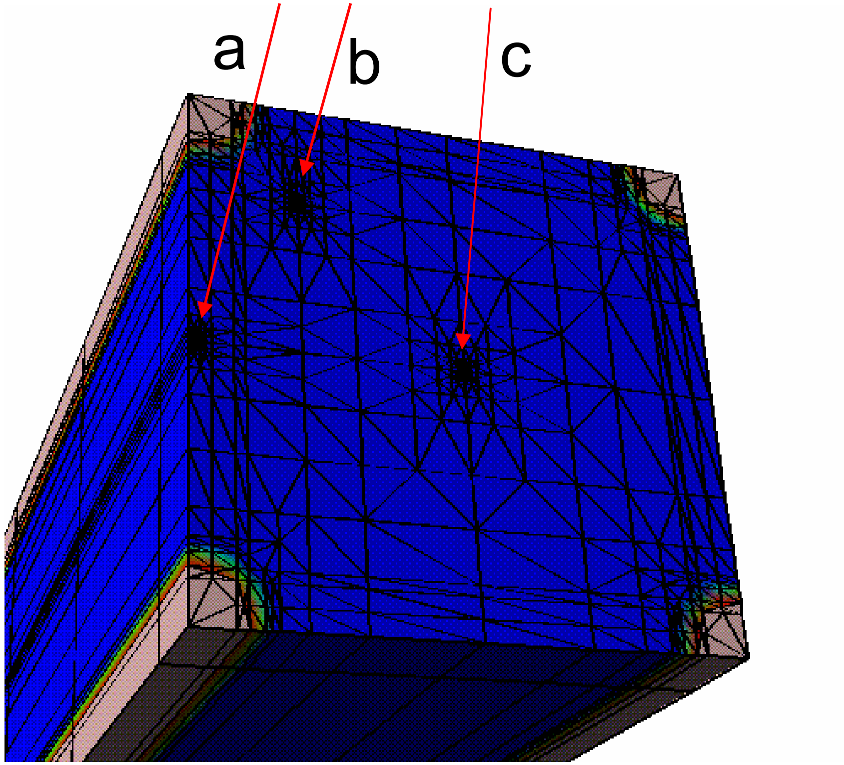


To increase the electric field strength one can act on the substrate doping concentration

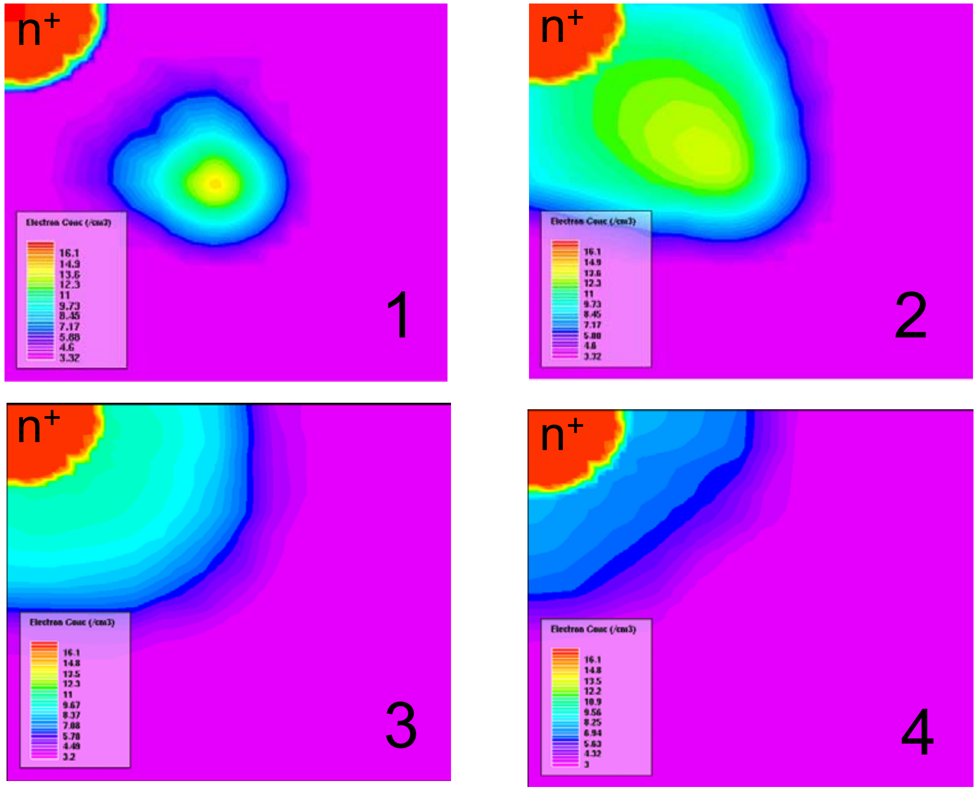
TCAD Simulations - dynamic (1)

Current signal in response to an ionizing particle.

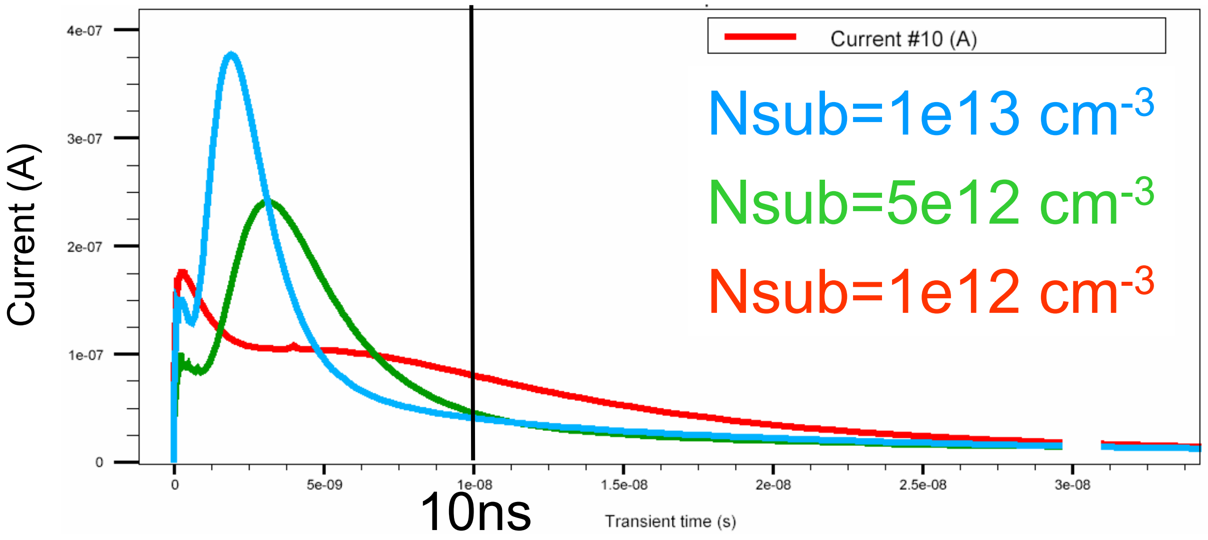
Vertical tracks in 3 different positions



Electron cloud evolution

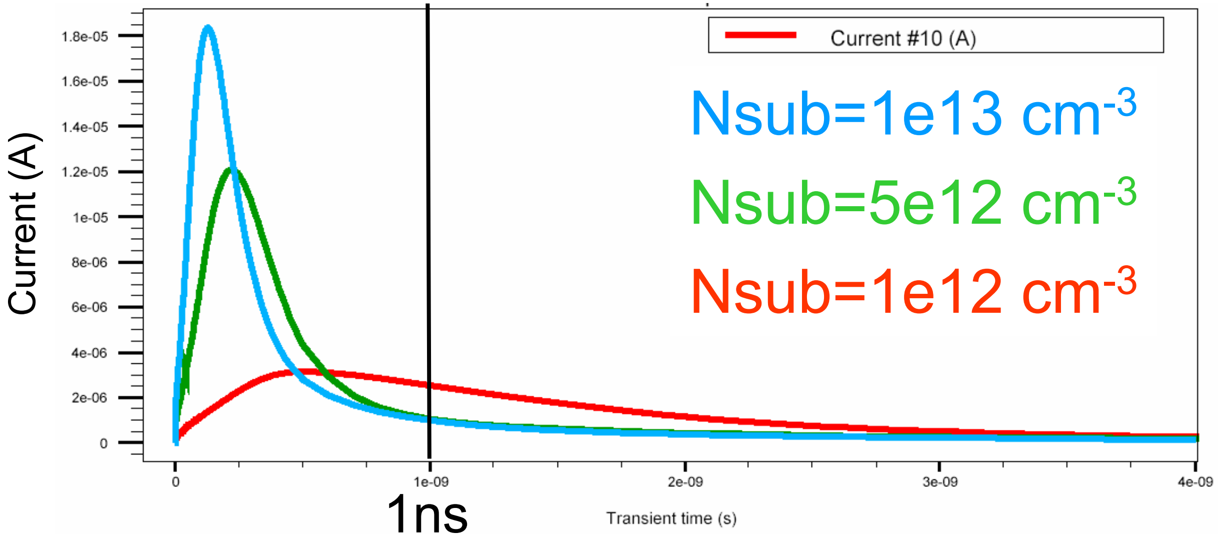


TCAD Simulations - dynamic (2)



Case c.

In the worst case the induced current peak is within 10ns

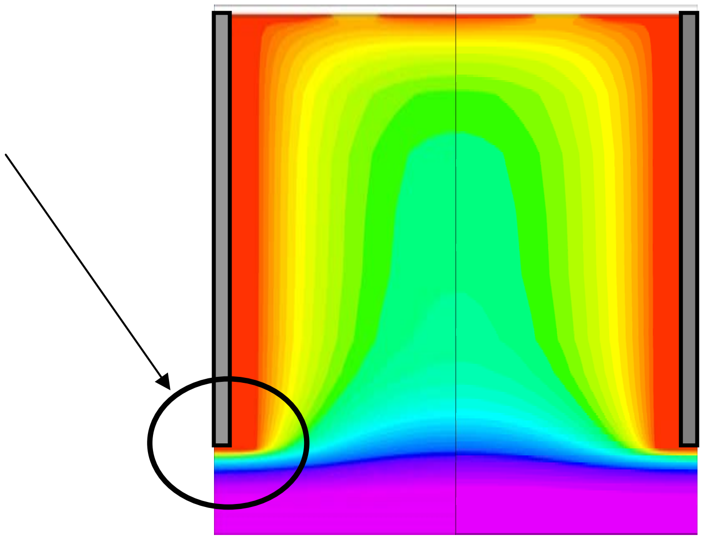


Case b.

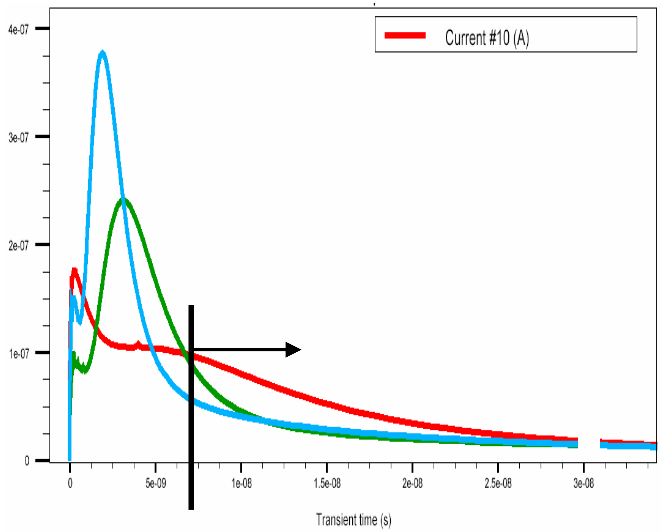
For a hit 5μm from the electrode the peak is within 1ns.

TCAD Simulations – critical points evidenced

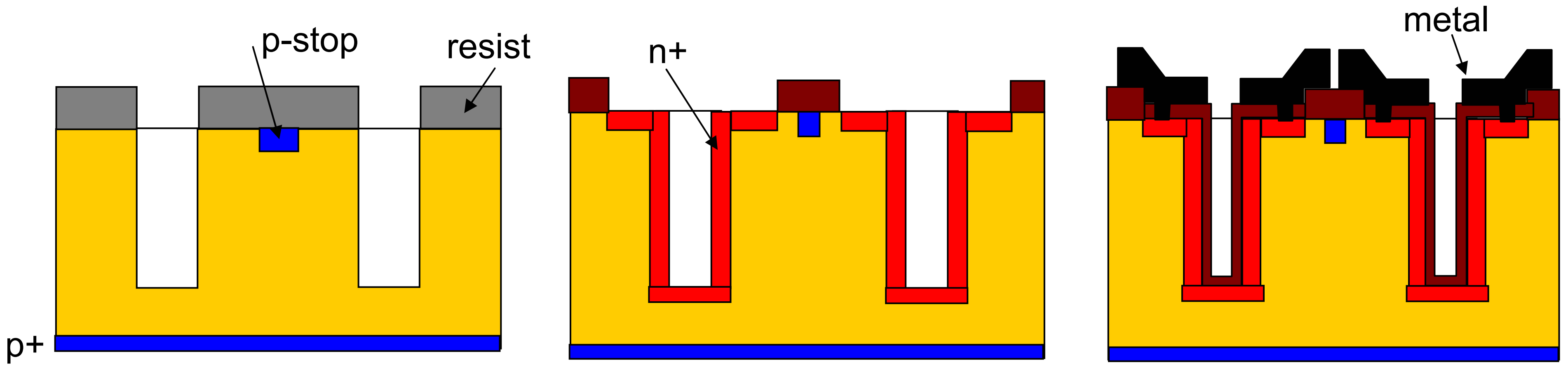
High field at the bottom of the hole. Anyway the critical value should not be reached because of the low bias voltages required.



Long low tail in the current signal due to hole movement. Simulations have shown that this effect can be strongly reduced using electrodes penetrating all through the wafer.



Fabrication process of 3DSTC detectors



1) n+ hole definition and etching

2) hole doping

3) Metal deposition and definition

Holes are etched at **CNM Barcelona**. 250μm depth with a radius of ~5μm

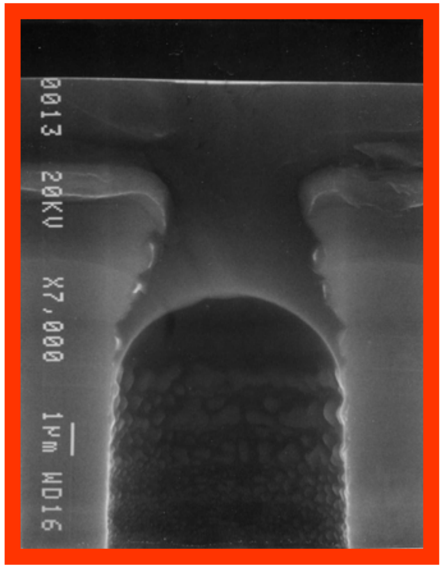
Doping by simple P diffusion or by P-doped poly-Si deposition

Holes are **partially** filled with thermal oxide or TEOS.

Contact only at the top.

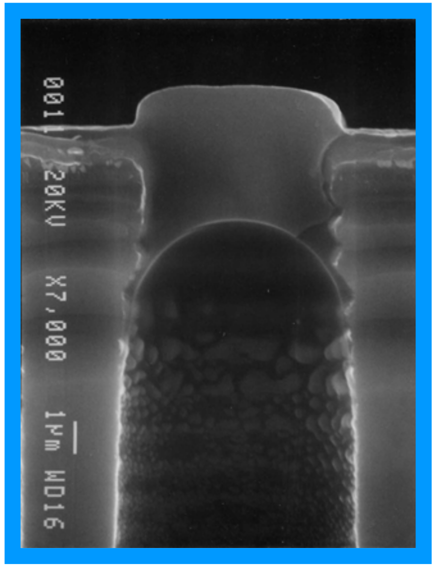
Single process steps have been already performed

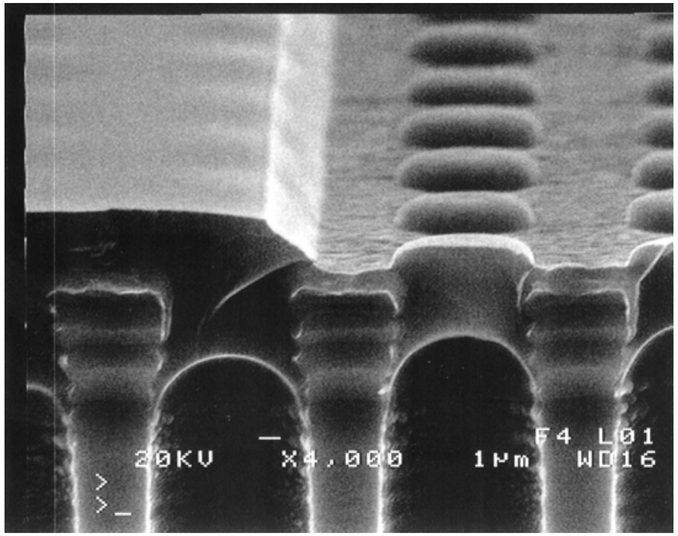
Fabrication process - lithography



as-deposited:
Photoresist tends to penetrate inside the hole forming a thicker layer in these region

after exposure and development: residual photoresist in the hole region





Important that **resist can be defined in the proximity of the hole**.

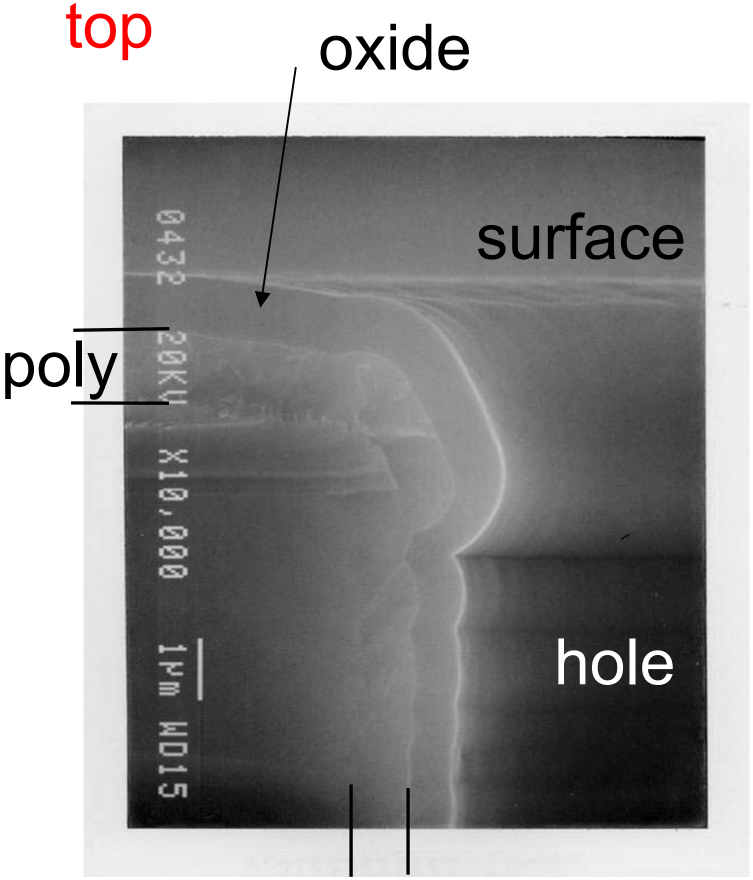
The resist trapped in the hole is removed after the process

Fabrication process - deposition

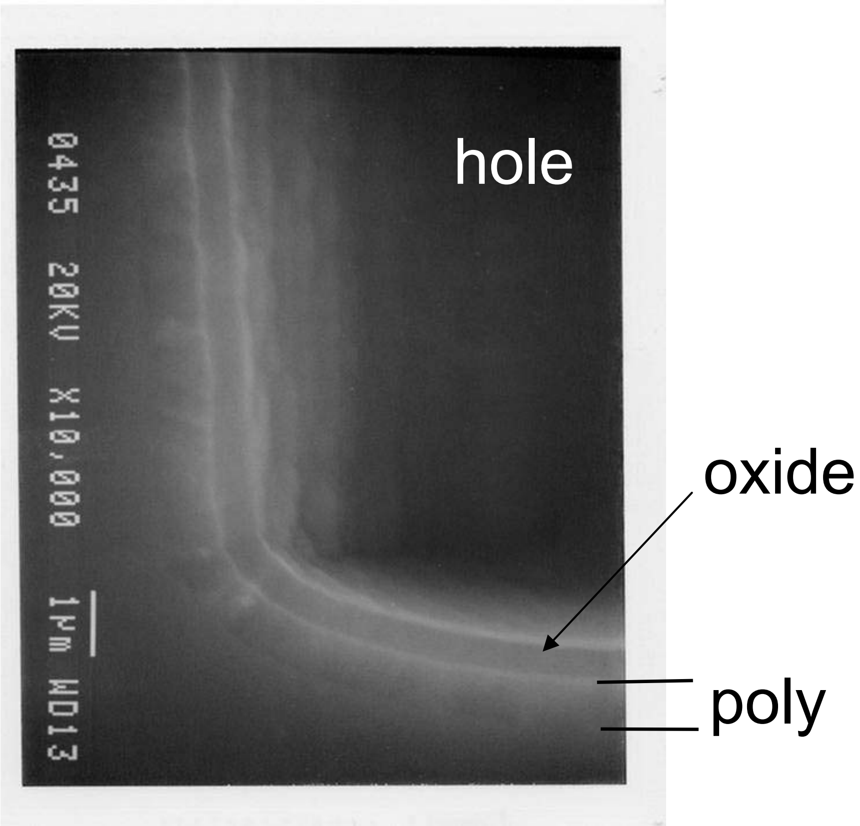
Poly and oxide deposition

	Surface	Top	botton
Poly	1μm	0.8μm	0.7μm
TEOS	1μm	0.7μm	0.6μm

top



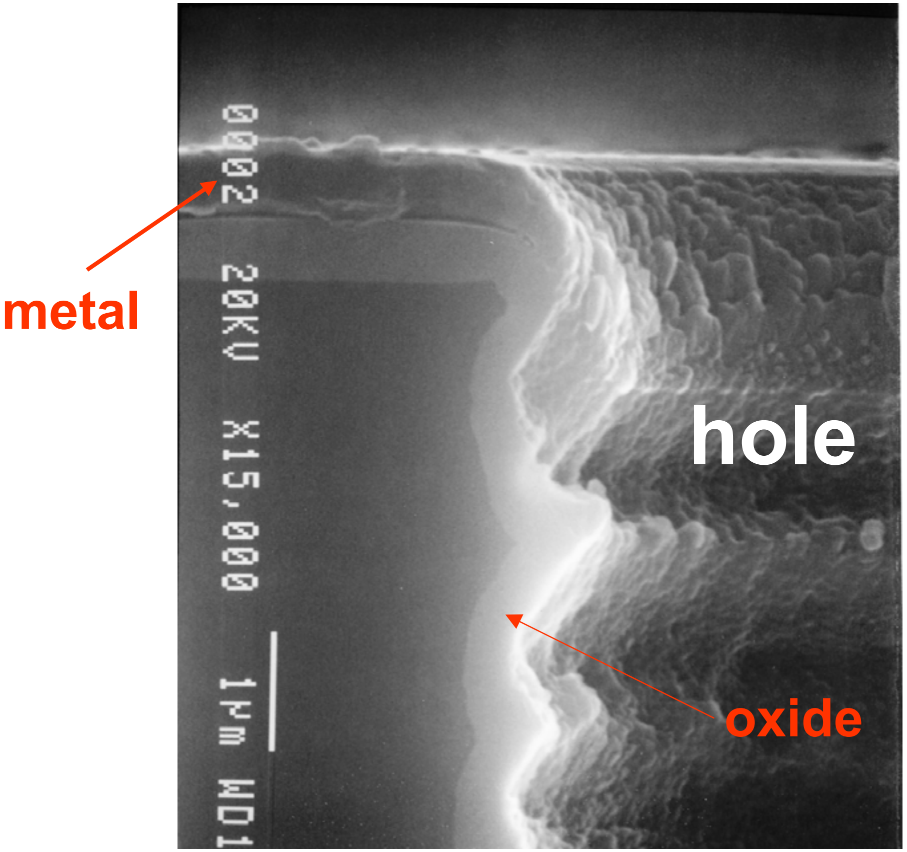
bottom



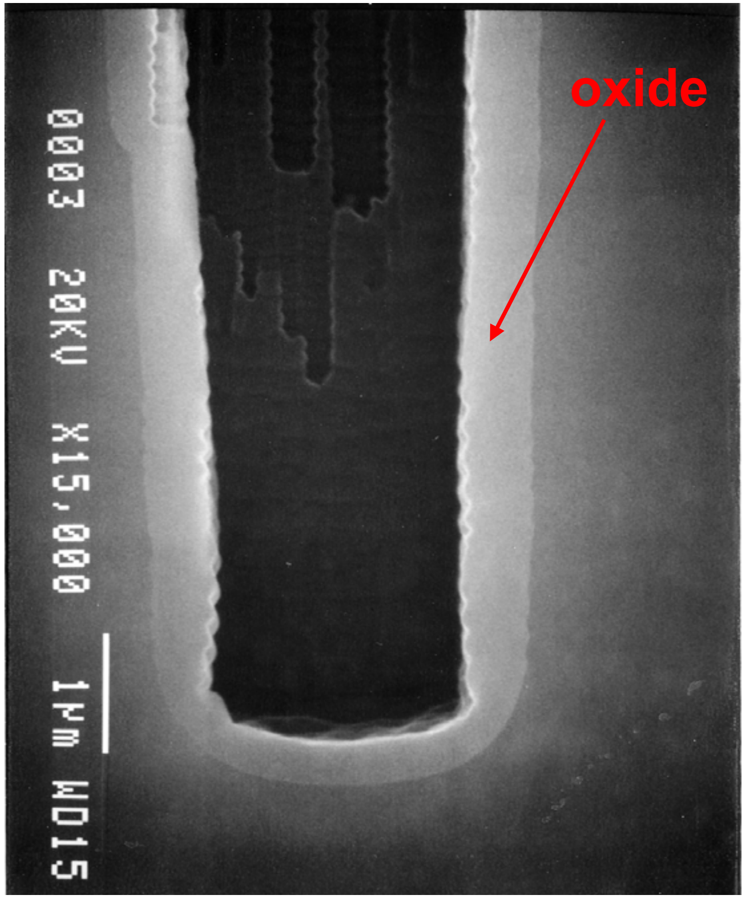
Fabrication process – oxide growth

Oxide Growth (500nm) in a 5μm diameter hole

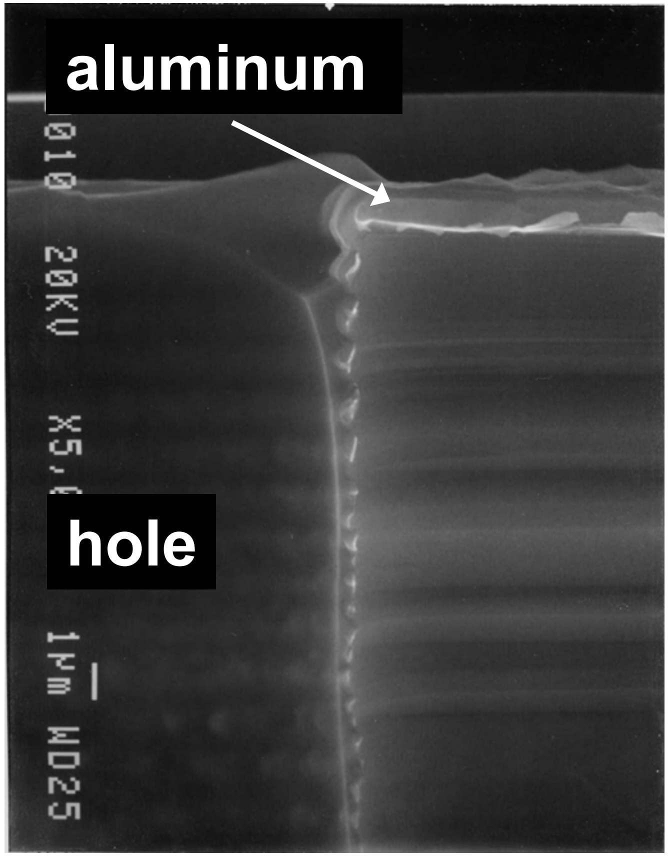
top



bottom

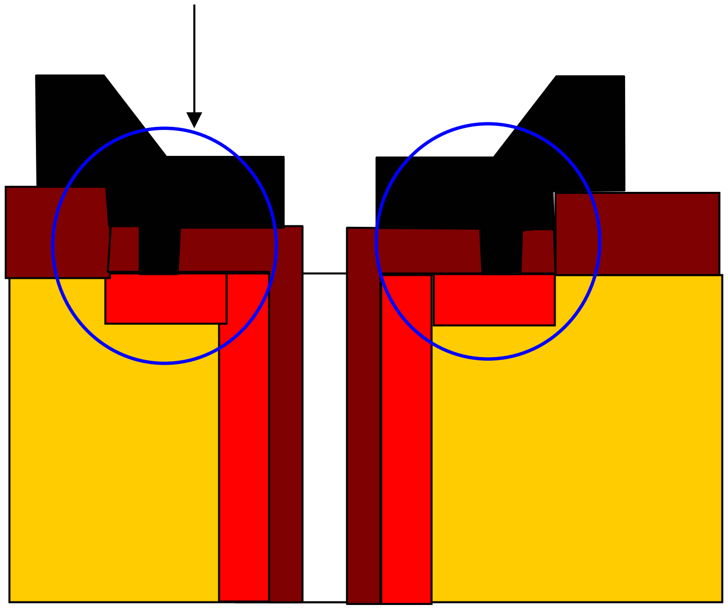


Fabrication process – metal sputtering

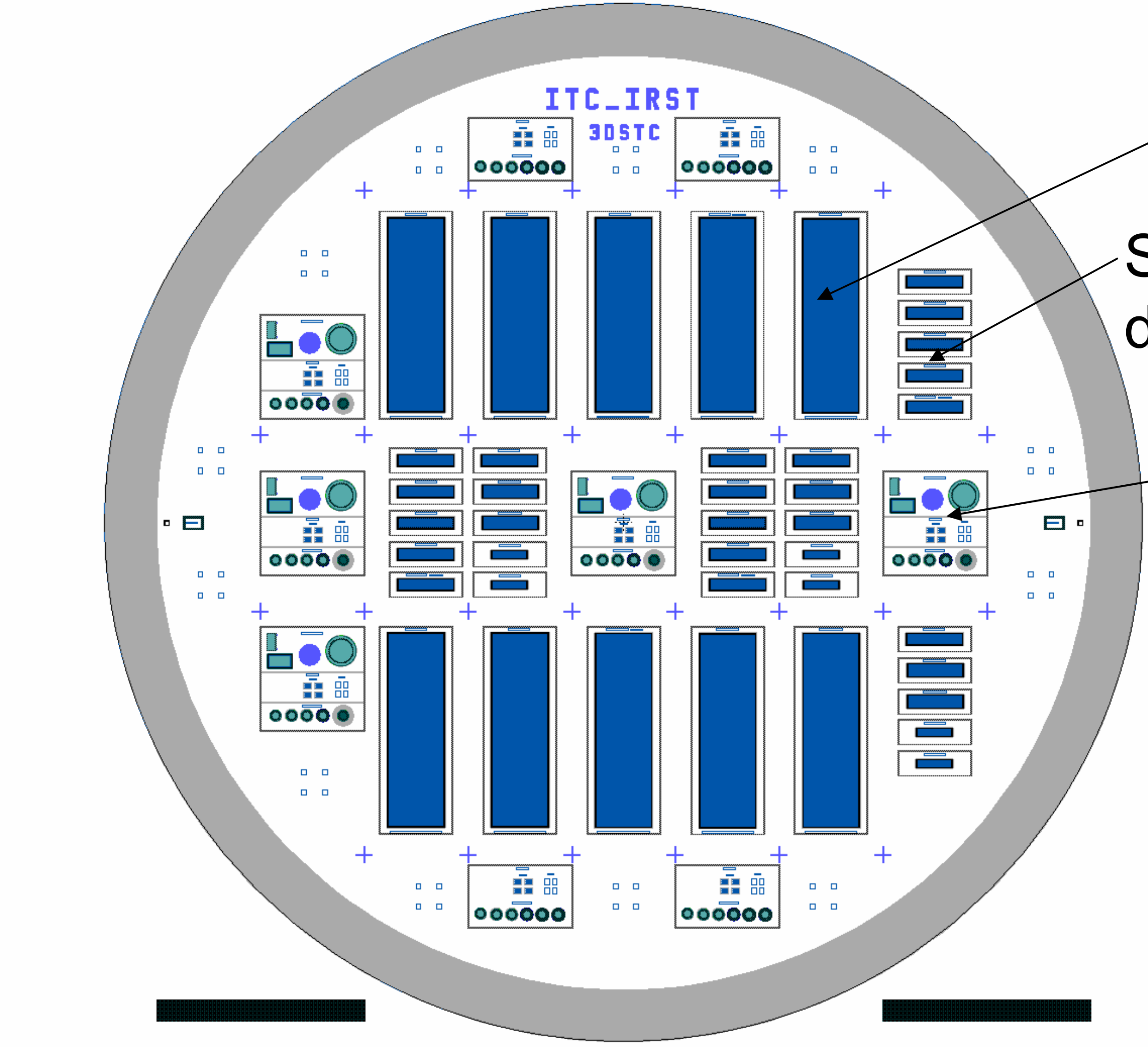


Aluminum does not penetrate inside the hole

➡ contacts have to be realized on the wafer surface



Mask layout



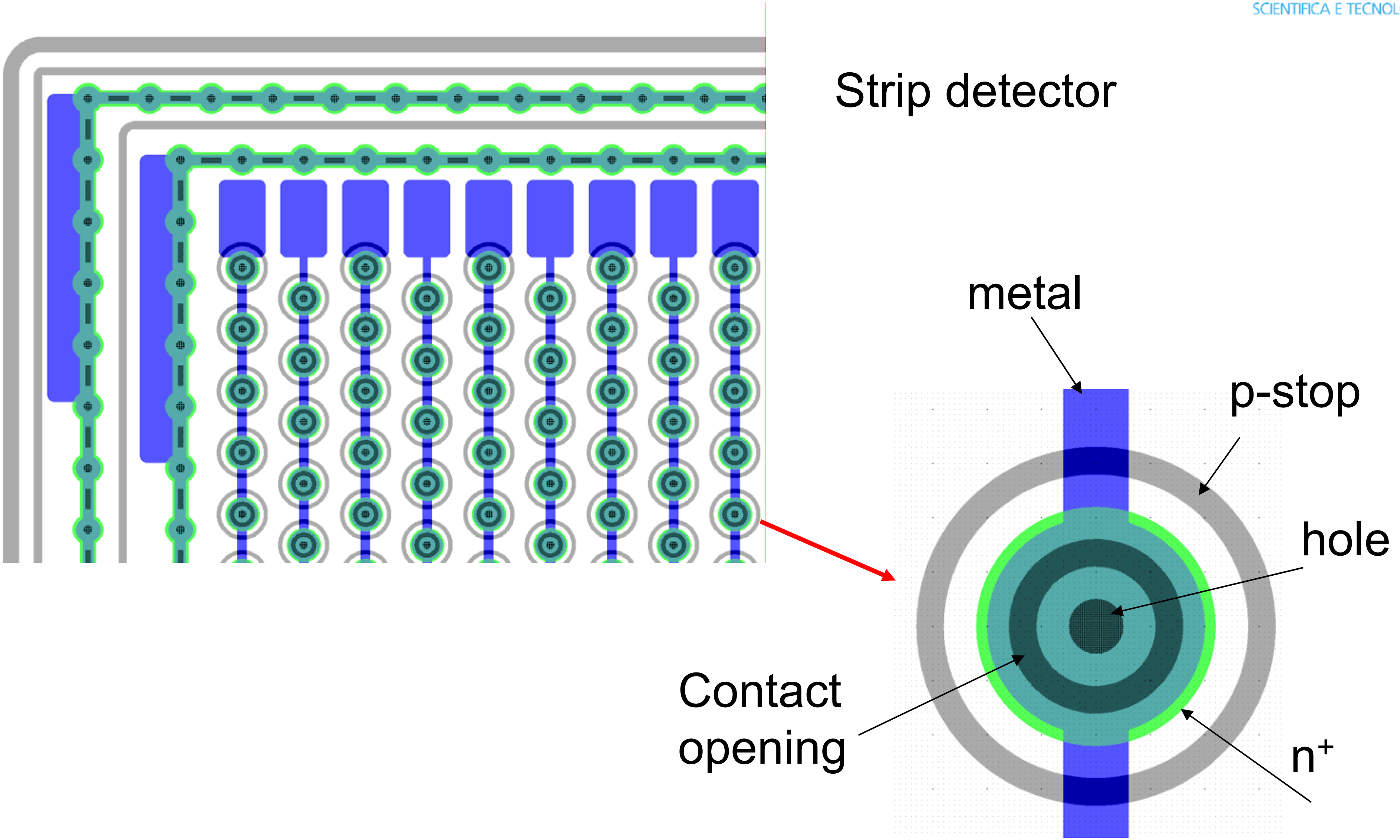
“Large” strip-like detectors

Small version of strip detectors

Planar and 3D test structures

“Low density layout” to increase mechanical robustness of the wafer

Mask layout - example



Conclusion

A new type of 3D detector has been conceived which leads to a significant simplification of the process:

- no wafer bonding;
- hole etching performed only once;
- no hole filling.

Disadvantages with respect to a standard 3D detector:

- more extended null-field regions;
- low tails on the current signal response.

Single process steps have been tested;
Layout completed;
➡ first production is starting.