RF Field Control for 12 GeV Upgrade

Tom Powers
K. Davis, J. Delayen, H. Dong, A, Hofler,
C. Hovater, S. Kauffman, G. Lahti,
J. Musson, T. Plawski,

12 GeV Cryomodule LLRF Requirements

Tight cavity field control is needed to meet CEBAF's energy spread specification.

Parameter	**Fast < 1s**	**Slow > 1s**
Phase Stability (correlated)	0.24^{o} (rms.)	infinite
Phase Stability (uncorrelated)	0.5^{o} (rms.)	3.0^{o}
Amplitude (correlated)	2.2×10^{-5}	NA
Amplitude (uncorrelated)	4.5×10^{-4}	NA

12 GeV Requirements (cont'd)

- Fault Recovery < 1 s
  - Must compensate for large Lorentz detuning on cavity turn on.
- Keep down-time low
  - Intelligent diagnostics that can quickly isolate problem RF-cavity systems.
  - Hot swap capable for all modules.
- Seamless integration with existing RF-Klystron-Cavity systems.
  - LLRF system should be compatible with existing RF HPA and cavity.

Recent LLRF Development Activities

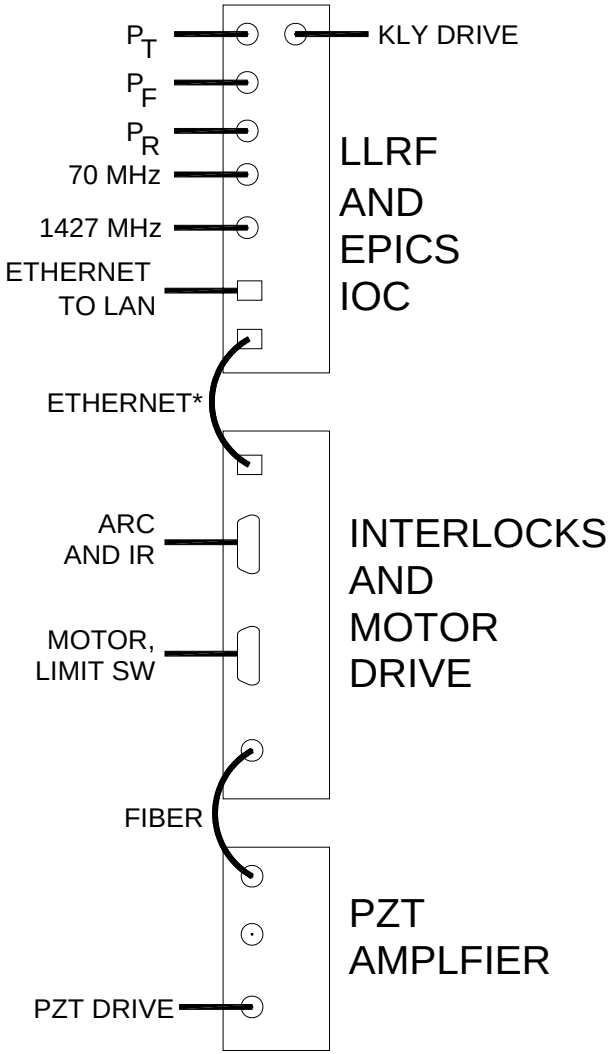
- **Cornell – JLAB Collaboration**
  - **A very successful collaboration between the two institutions tested the Cornell LLRF system in the JLAB FEL and in CEBAF**

- **LLRF Requirements:**
  - **An in-depth requirement package detailing, top level, functional and hardware requirements was completed May 30.**
    Many thanks to S. Simrock, B. Chase, M. Champion and R. Ursic for review!

- **Subsystem Prototyping**
  - **1497 MHz Receiver/Transmitter prototype: Tested on cryomodule**
  - **499 MHz LLRF System: In production.**
  - **Piezo tuner concepts: tested with Cornell LLRF system**
  - **Digital signal processing modeled and streamlined**

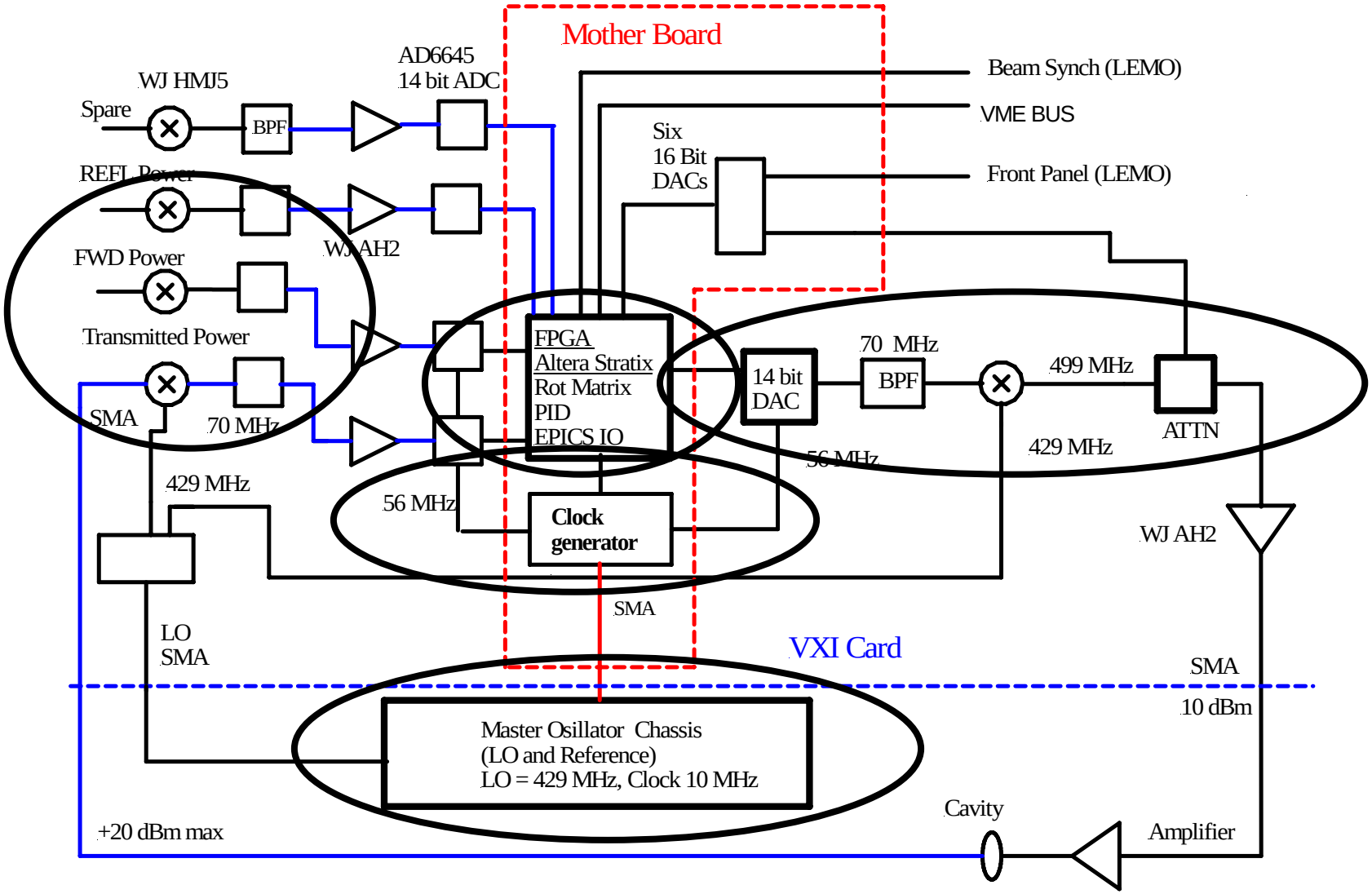
- **Model/ Algorithm Development/Firmware**
  - **Electronic Damping Modeled: PAC 2005 (A. Hofler and J. Delayen)**
  - **Resonance Control: (Collaborating with Cornell) test in CMTF/FEL fall 2005**

Proposed System Layout



- Three modules in baseline design, LLRF, Interlocks and PZT Amplifier.
- Modules may be VME format. However, the primary function of the backplane is power distribution and shared signal distribution.
- IOC imbedded in LLRF module with direct Ethernet connection to operating system local area network.
  - Working towards a NIOS core imbedded in the FPGA.
  - May change to imbedded processor.
- Ethernet* protocol for communication between interlocks and LLRF.
  - Four wires standard two-way Ethernet protocol.
  - Two wires RF permit from interlocks.
  - Two wires serial DAC link for the PZT amplifier.
- Fiber optic link to PZT amplifier, which is a 750 V, 0.5 A output device.

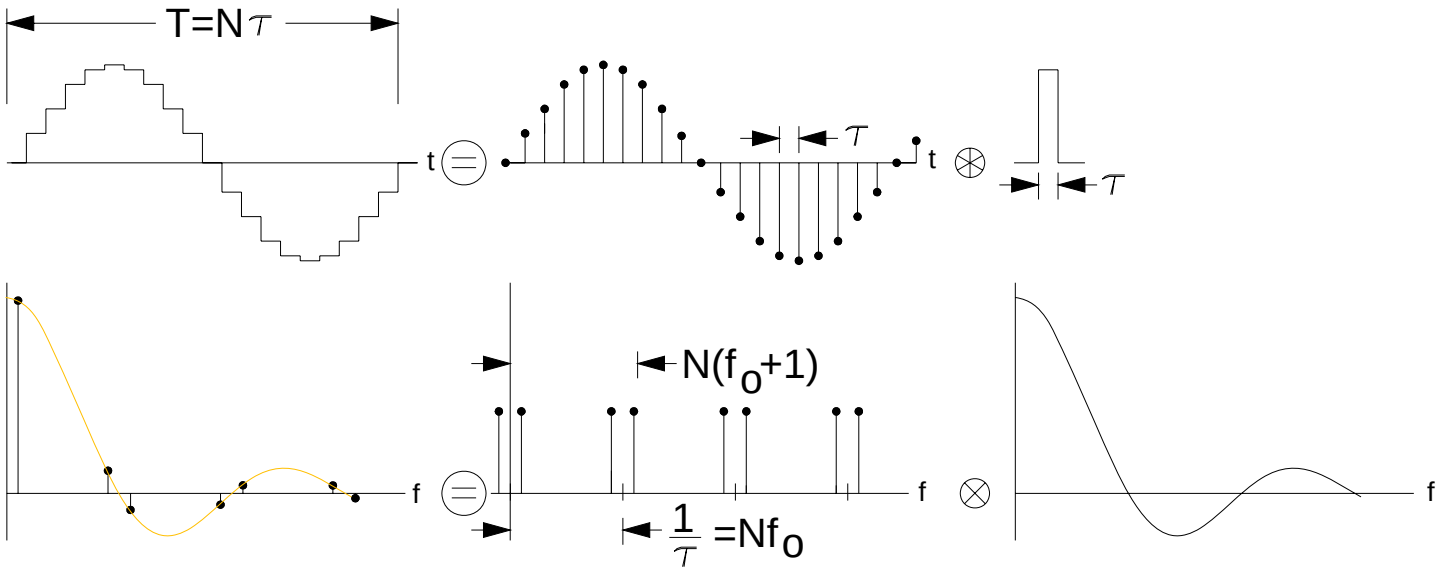
LLRF Block Diagram



LLRF FEATURES

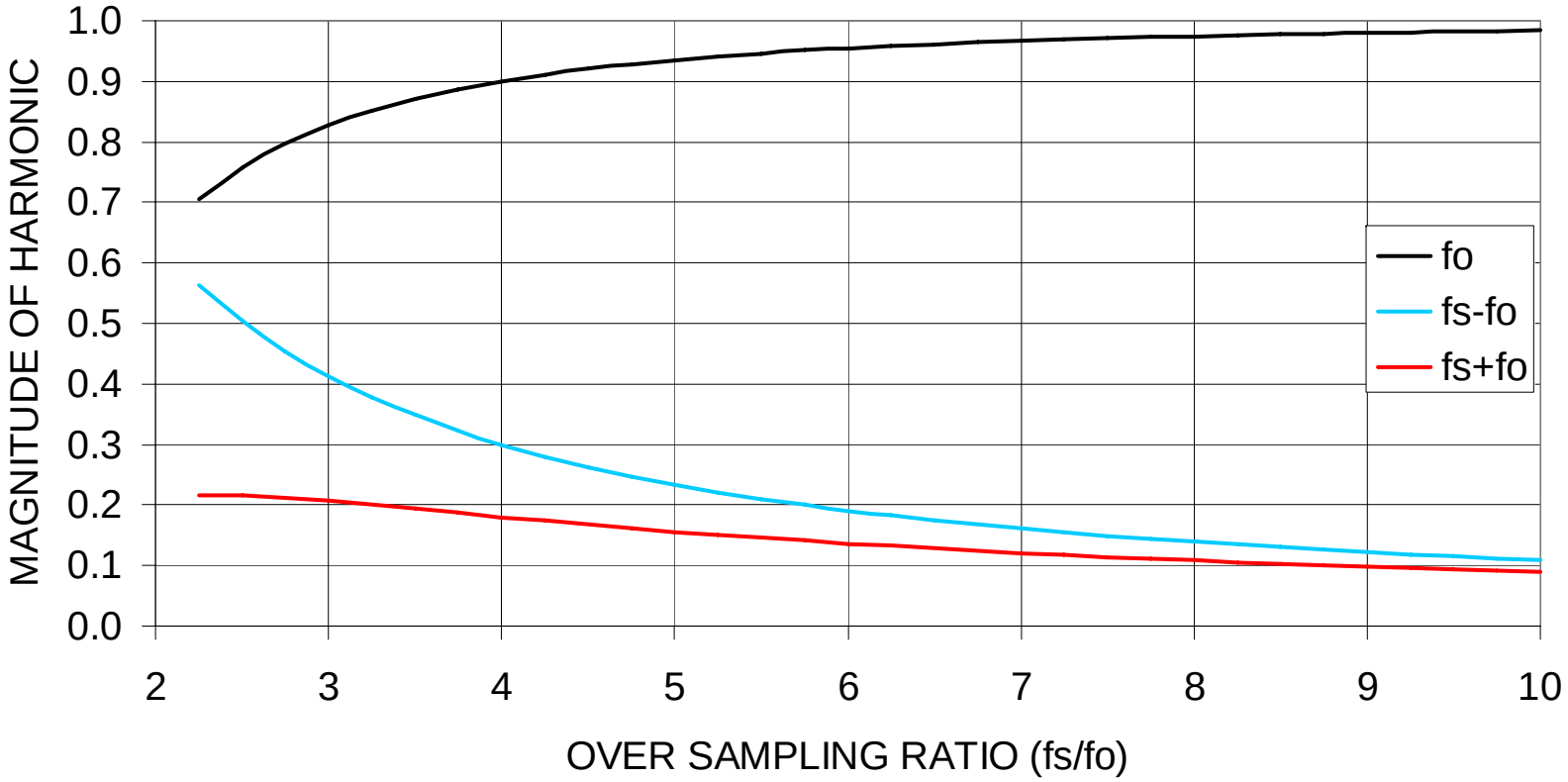
- Makes used of existing master oscillator distribution system at 1427 MHz, 70 MHz and 10 MHz.
- 56 MHz sample clock generated on mother board.
- Down convert to 70 MHz IF.
- ADC clock frequency is 1.25 cycles of 70 MHz, providing +I, +Q, -I, -Q, +I, +Q . . . data stream or I and Q at 14 MHz.
- Altera Stratix FPGA for phase and amplitude control as well as interface to control system.
- Direct digital synthesis for IF generation using the third sideband of the ADC output. (Larry Doolittle "Plan for 50 MHz Analog Output" Aug. 8, 2002)
- Because ADC and DAC are run with the same 56 MHz clock, slow phase drifts, etc. of the clock are not seen on the output.

Direct Digital IF Signal Generation



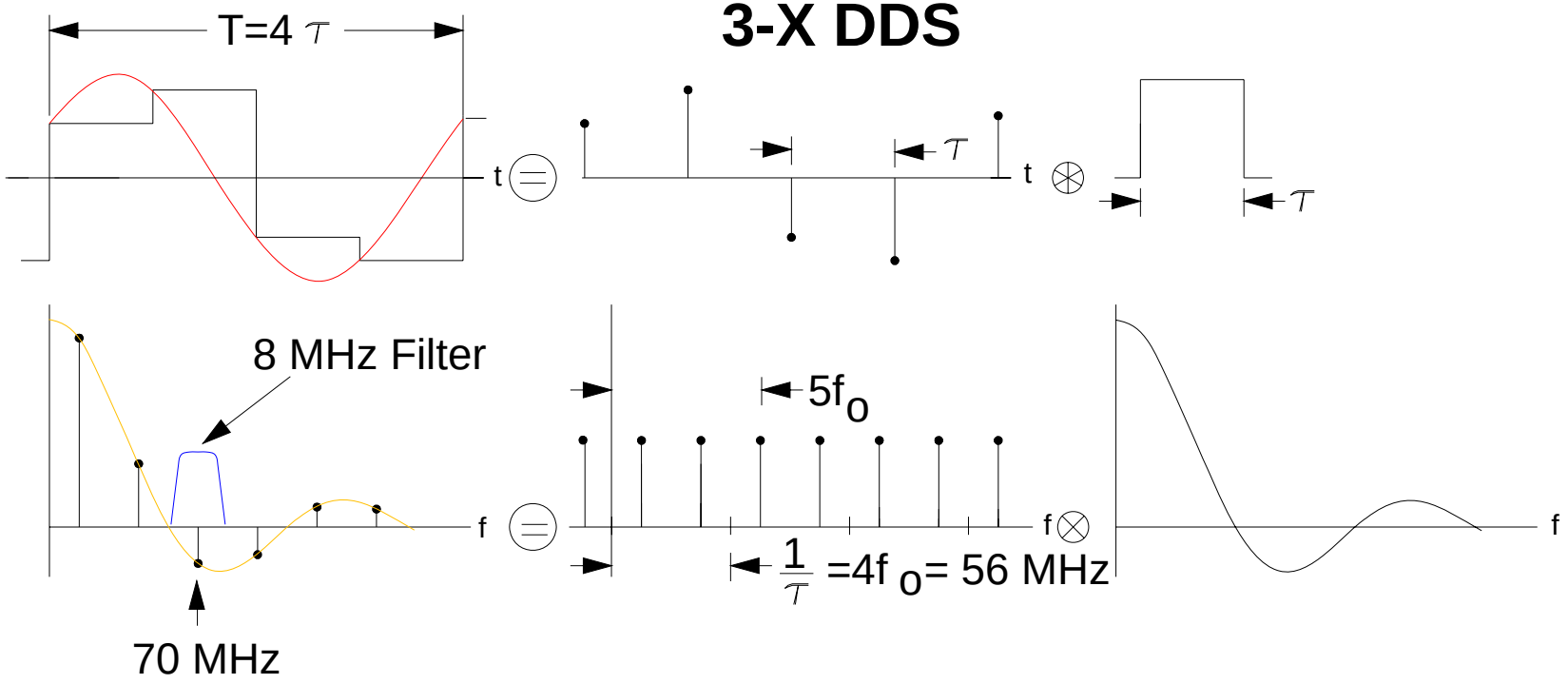
- Concept use one of the harmonics out of your ADC for your IF frequency.
- For a 10-X system two disadvantages to using second or third harmonic frequencies are:
  - Small signal content.
  - Analog filter requirements.

Relative Magnitude of Harmonics



- Relative magnitude of the three harmonics out of an ADC when the sampling frequency, fs, is near the signal frequency, fo.

3-X DDS



- Ratios of f3 to f1 is 1:5.
- 70 MHz component is 14 MHz away from nearest neighbor.
- Commercial drop in 8 MHz BW filter available for $30.
- One can show that the harmonic contains the proper phase signal and is: $A\sin(2\pi f_0 + \varphi) \Rightarrow B_k A\sin(2\pi(kf_S \pm f_0)t + \varphi)$ where $k = 0, 1, 2 \ldots$

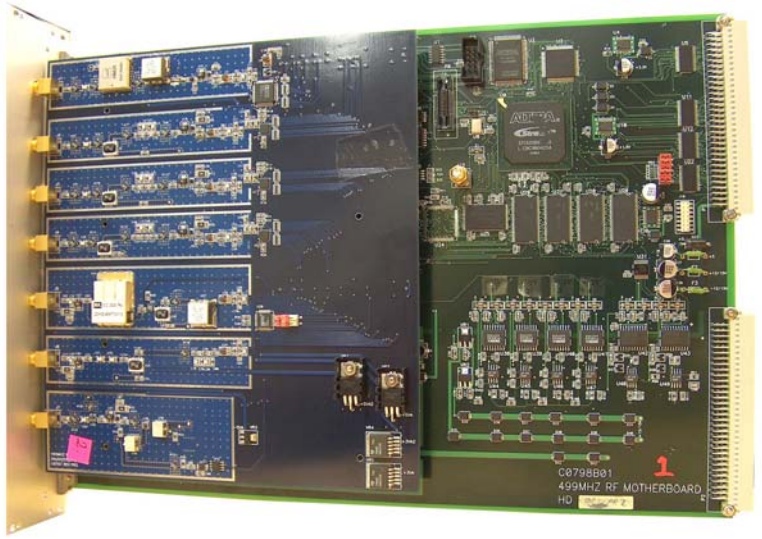
Minimizing Thermal Drifts

- Receiver designed with “Thermopad” variable tempco attenuators in an effort to null out drifts.
- Monitored phase and amplitude of the new LLRF system for drifts between 10^{o} to 50^{o} C
- Results
  - Phase: 0.13^{o}/C
  - Amplitude: 0.1%/C

>10x better than present CEBAF LLRF

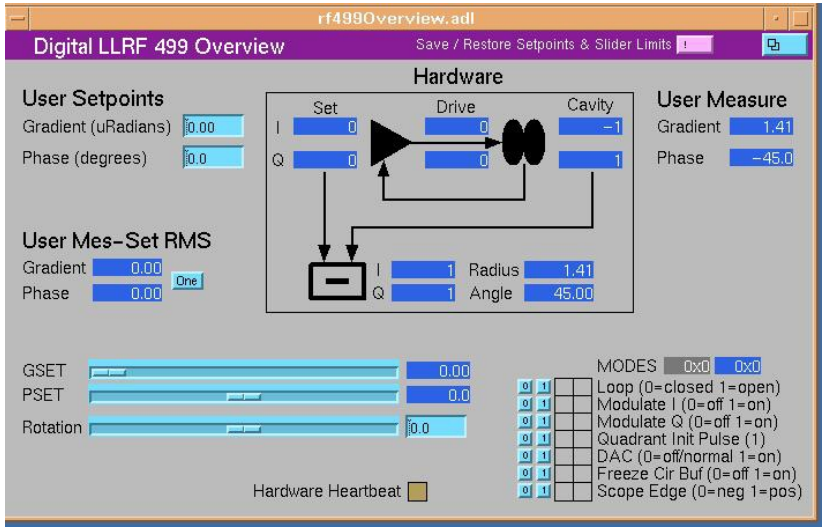
Current 1497 MHz Prototype System

- Prototype 1497 MHz and production 499 MHz LLRF systems designed around a “generic” processor motherboard
  - Extended VME motherboard uses Altera Stratix FPGA for PID and cavity resonance control.
  - Can support transceivers at our different cavity frequencies (499 MHz & 1497 MHz).
  - RF receivers, RF transmitter, ADC and DAC located on the daughter card.



VME Motherboard & 499 MHz Transceiver 2005

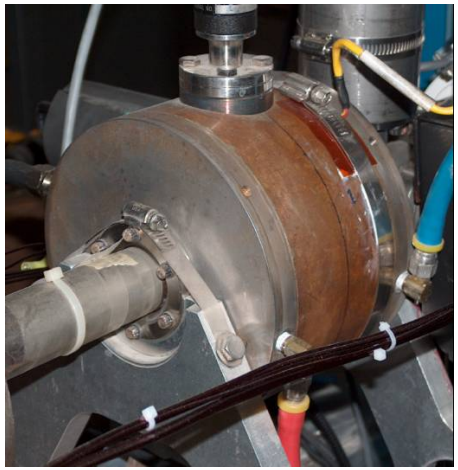
- Prototype testing controlled through EPICS



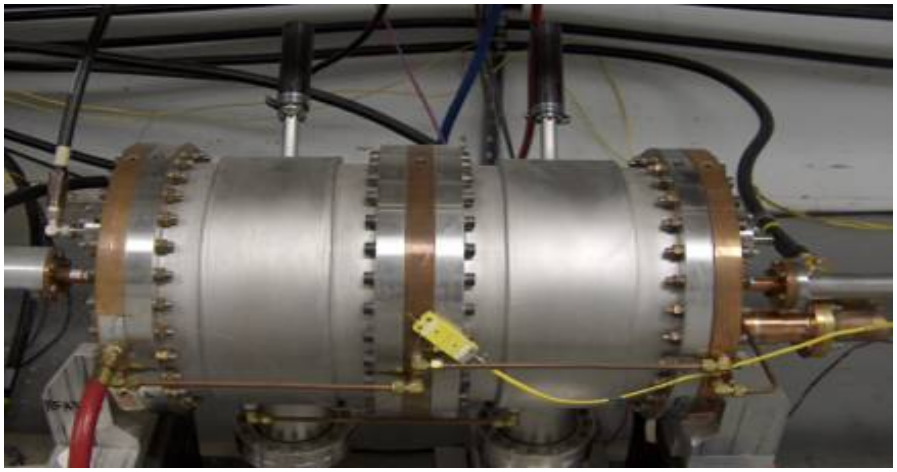
Proto - EPICS Control Screen

Normal Conducting LLRF at 499 MHz: Status

- Prototype system has been tested on a Separator cavity in CEBAF
- 15 Production systems are being manufactured
- Eight systems to be installed and commissioned in January 2006



CEBAF buncher cavity



CEBAF separator cavity

System Modeling

- Matlab/Simulink Modeling
  - Simulink models are based on DESY's Simulink Library for SRF systems (Varadanyan, Ayvazyan, & Simrock EPAC'02)
  - Matlab modeling scripts based on transfer function representations of systems
- Electronic Damping for 12 GeV Upgrade Cavities
- Warm RF and SRF cavity systems

Electronic Damping

- Electronic damping uses ponderomotive forces to intentionally deform the cavity in a manner opposing microphonic effects.

- An analytical model for the system has been developed and verified using numerical simulations.

- Electronic Damping can be used to damp microphonic vibrations
  - In lightly beam loaded superconducting cavity applications (JLab 12 GeV Upgrade, RIA, and possibly ERLs)
  - Simulations indicate that one can achieve a 50% decrease in phase error accompanied by 3×10^{-5} increase in amplitude error

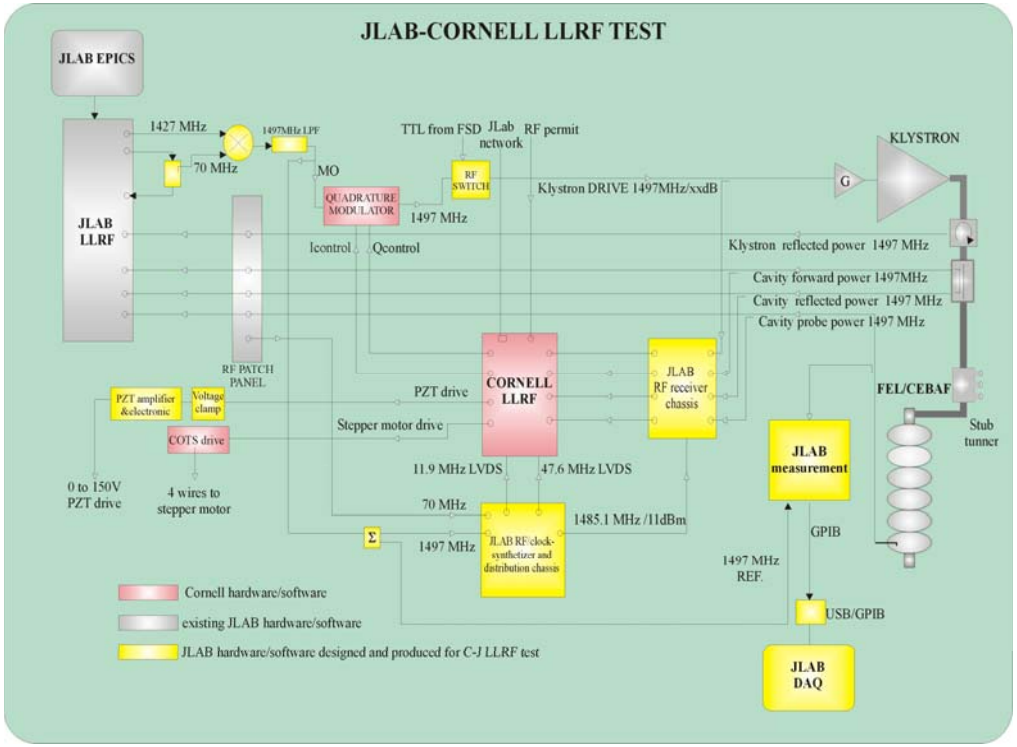
- We are currently expanding model to include effect of multiple mechanical modes.

Test Programs

- Proof of principal system built with Altera Stratix development kit. March 2004
- JLAB-Cornell Digital-LLRF Collaboration Sept. 2004 through Jan. 2005.
- Environmental testing of 499 MHz system April 2005
- 499 MHz System tested with warm cavity May 2005.
- 1497 MHz System low power tests with cold CEBAF upgrade cavity Aug. 2005
- 1497 MHz system high power tests with cold cavity NEXT WEEK
- 1497 MHz system high power tests with resonance controls THE WEEK AFTER NEXT.

CORNELL - JEFFERSON LAB COLLABRATION

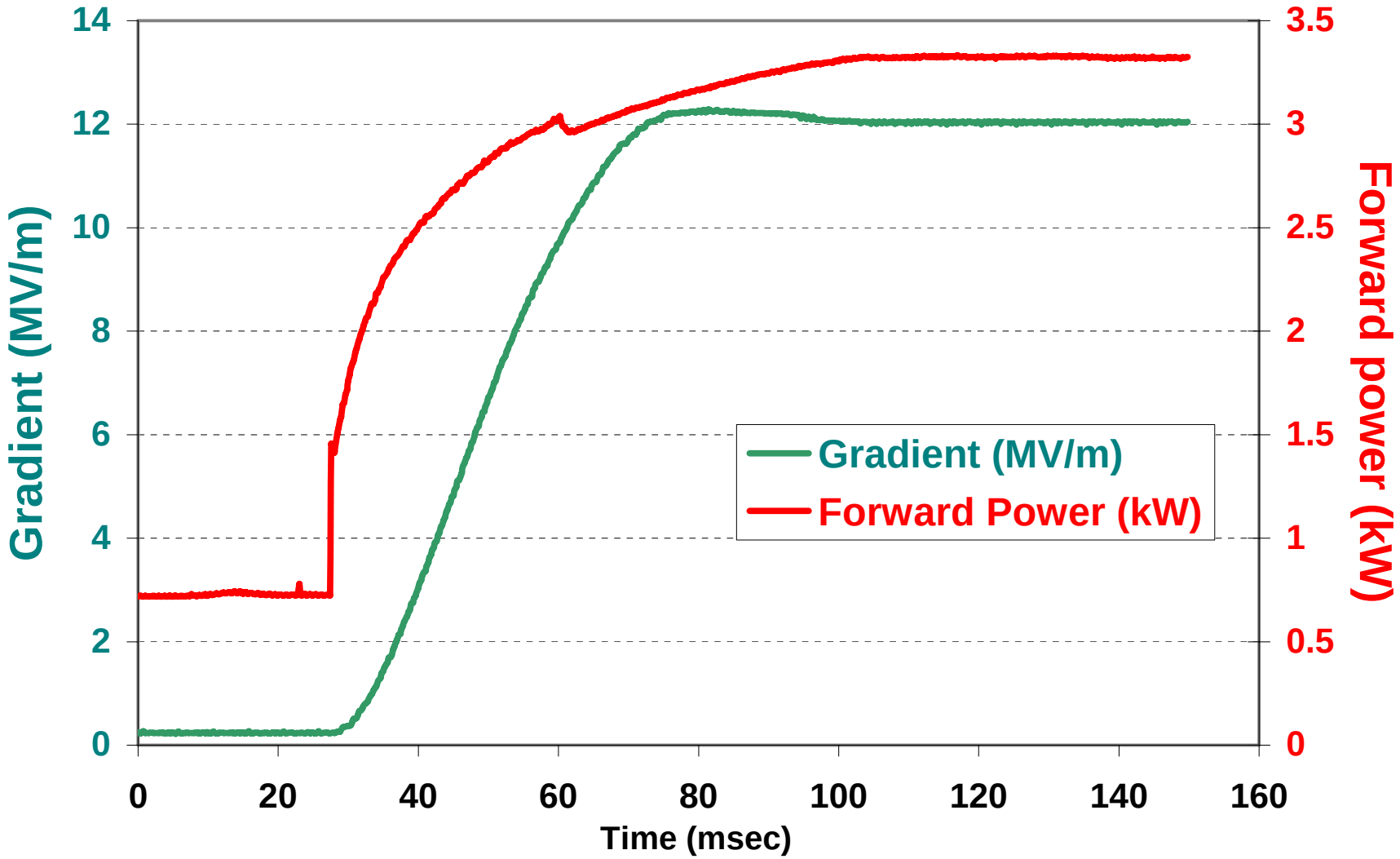
- Opportunity for two labs to test and operate hardware and firm ware algorithms on a height loaded-Q superconducting cavity.
- Cornell provided the
  - Digital LLRF system
  - DSP/FPGA algorithms,
  - PZT analog drive and
  - Tuner motor drive.
- JLAB provided the:
  - Downconverters,
  - up converters
  - reference clocks
  - PZT amplifer
  - Operating accelerators with beam.



JLAB-Cornell Digital-LLRF Collaboration

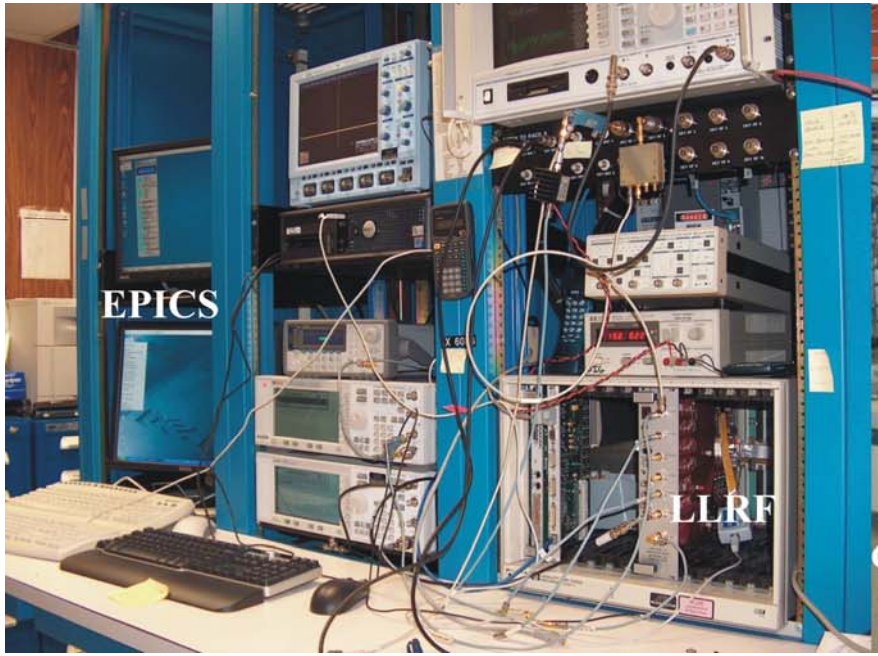
- Phase and amplitude control on a real cavity with beam loading
  - Conditions: CW beam up to 400 uA
  - Result: Met specifications
    - Phase stability: ~ 0.02 degrees rms.
    - Amplitude stability: ~ 2×10^{-4} rms.
- Cavity recovery under strong Lorentz detuning
  - Result: 0 to 12 MV/m in ~80 ms using Piezo Tuner (PZT)
- Cavity recovery from simulated CHL crash
  - Initial condition: Cavity resonance frequency 30 kHz off master oscillator frequency
  - Result: Successful hands-off recovery.
- Operated cavity at high Q_L ~ 1×10^8
  - Result: Met phase and amplitude control specifications

Cavity Recovery after Fault

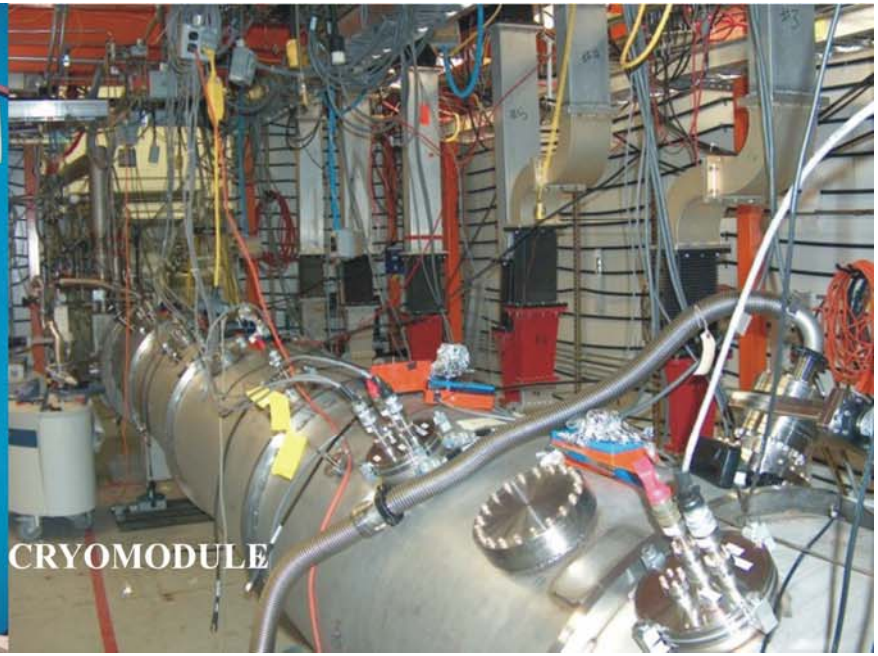


FEL03-3 with $Q_L = 2x10^7$

LLRF Test with 1497 MHz SC Cavity /Renascence Cryomodule



Control Room



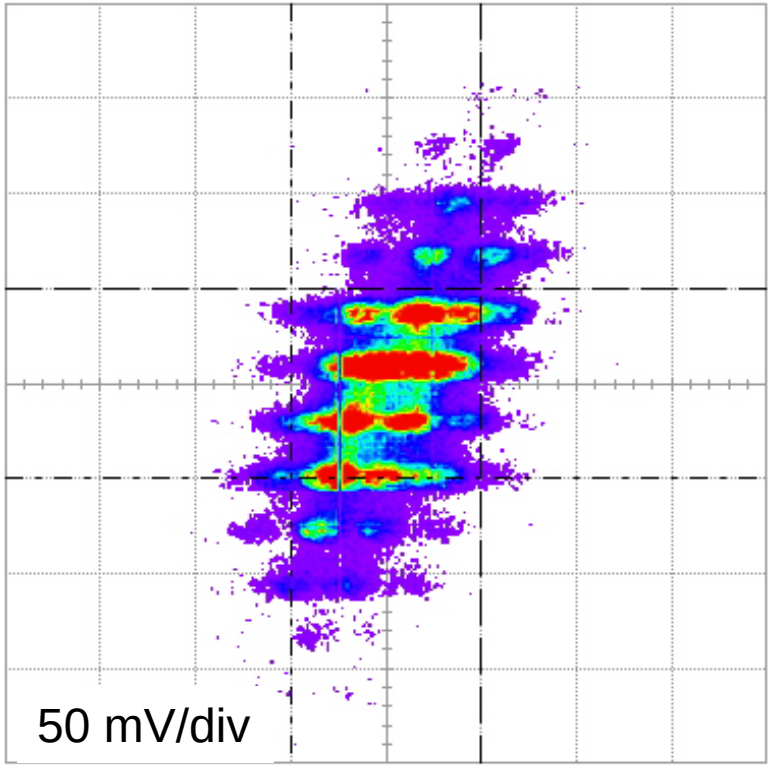
Test cave with cryomodule “Renascence”

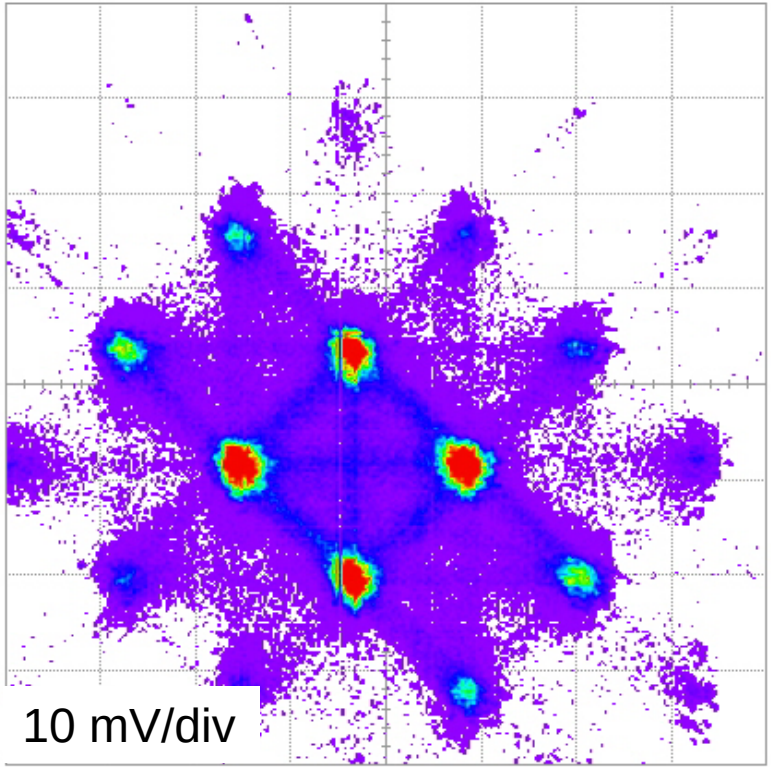
Low RF power (1W) test result for SC cavity (Loaded-Q = 8e+6)

Closed Loop	yes	RMS Phase Noise	**0.06 deg**
Open Loop Gain	183	RMS Gradient Noise	**0.02 %**
Integral Gain	4		
Integral Time	840 ms		

I/Q Space Measurements

(Low Power SRF Cavity)



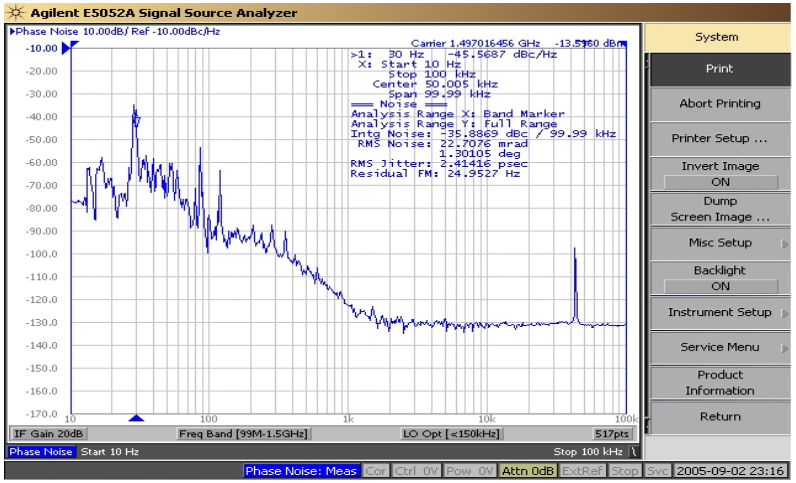


System on the edge of stability.

PID Loop optimized

(D = zero gain)

Phase noise measurement for 1497 MHz SC cavity



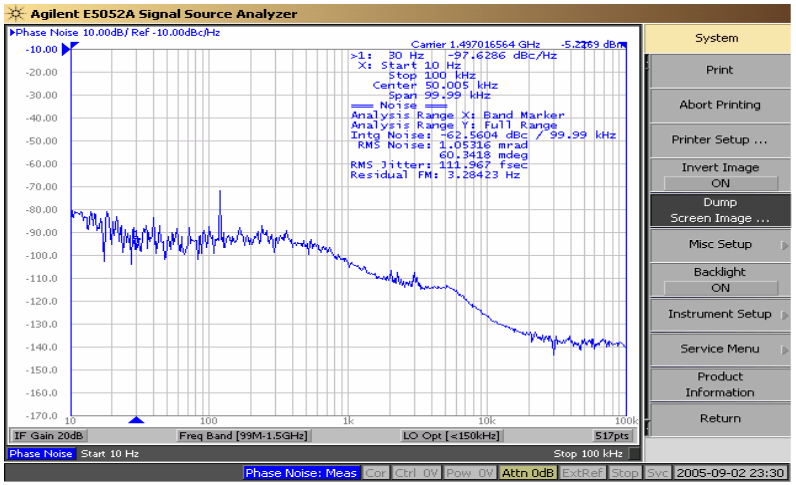
Carrier 1.497 GHz

X: Start 10 Hz Stop 100 kHz

RMS Noise: 22.7076 mrad / 1.30105 deg

RMS Jitter: 2.41416 psec

Fig.1 open loop- cavity microphonics cause extensive phase noise of 1.3 deg RMS



Carrier 1.497 GHz

X: Start 10 Hz Stop 100 kHz

RMS Noise: 1.0532 mrad / 60.34 mdeg

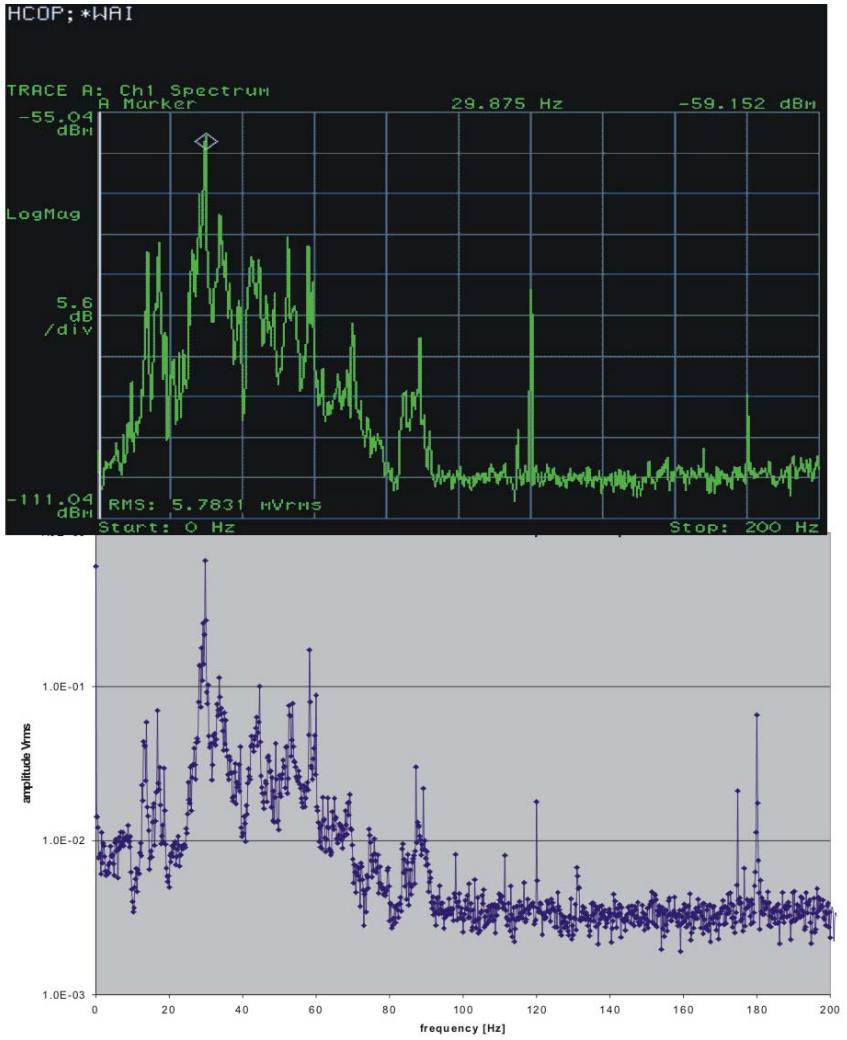
RMS Jitter: 111.967 fsec

Fig.2 closed loop- RMS phase noise reduced from 1.3 deg down to 0.06 deg

Digital LLRF system makes microphonic measurements easier !

Upper part of the picture shows forward power spectrum for closed loop and optimized regulation. It reflects microphonics compensation.

Lower graph shows cavity microphonics spectrum measured with PLL and dedicated instrument “Cavity Resonance Monitor” , performed for the same cavity a few days earlier.



LLRF Next Steps

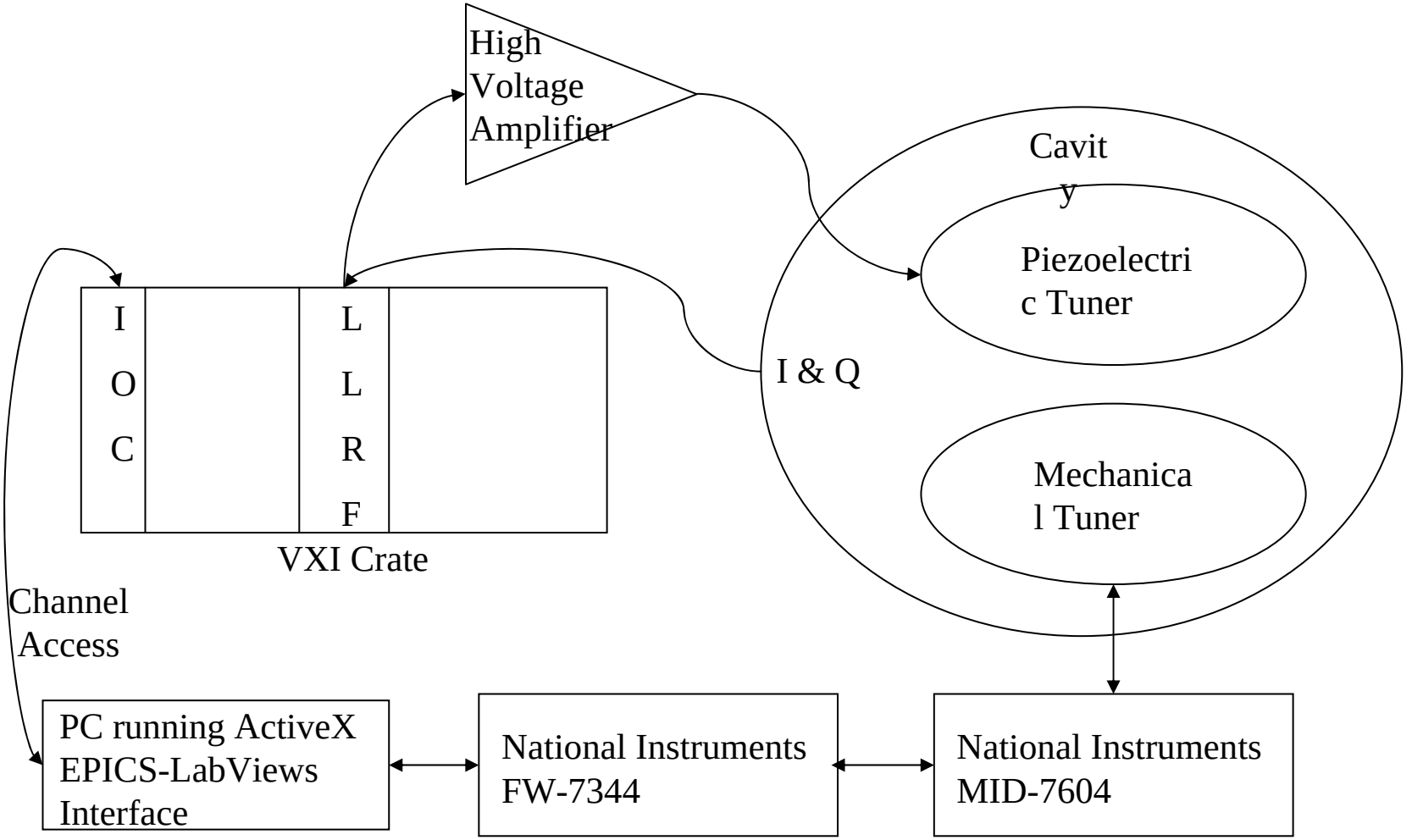
- 1497 MHz tests in CMTF/FEL — Fall 05
- Instalation & Comm. of NC LLRF — January ‘06
- Complete vertical slice tests with 13 kW tube and high gradient cavity (>15 MV/m) LLRF on a cavity in CMTF — Winter ’07
- 8-seat test cryomodule test of LLRF on FEL-3 — fall, 07

Summary

- We continue to have a successful collaborations with Cornell, DESY, SNS and Berkley during the development process.
- Cornell Collaboration: Demonstrated that a Digital LLRF system is capable of meeting the CEBAF phase & amplitude control specifications using SRF cavities.
- Successful operation of both warm and cold structures with the JLAB prototype systems.
- High power testing of JLAB prototype system with SRF cavities to occur in the next few weeks.
- JLAB is well on the way to developing a LLRF system for it's 12 GeV upgrade. However, much work remains in hardware, firmware and software optimization.

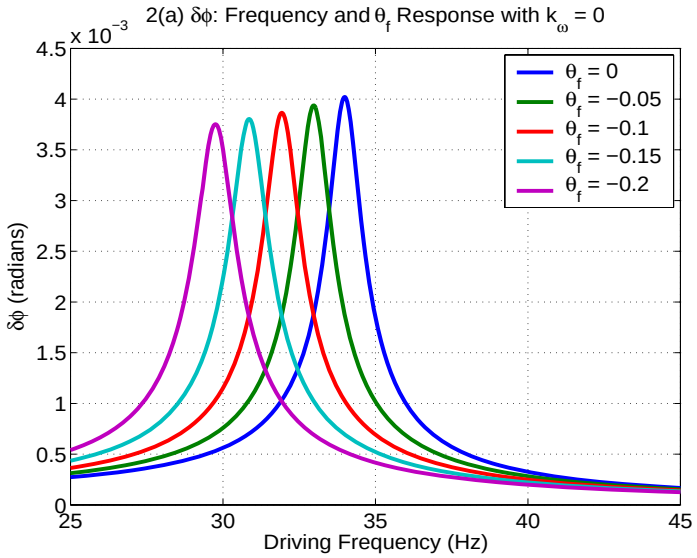
Digital Signal Processing

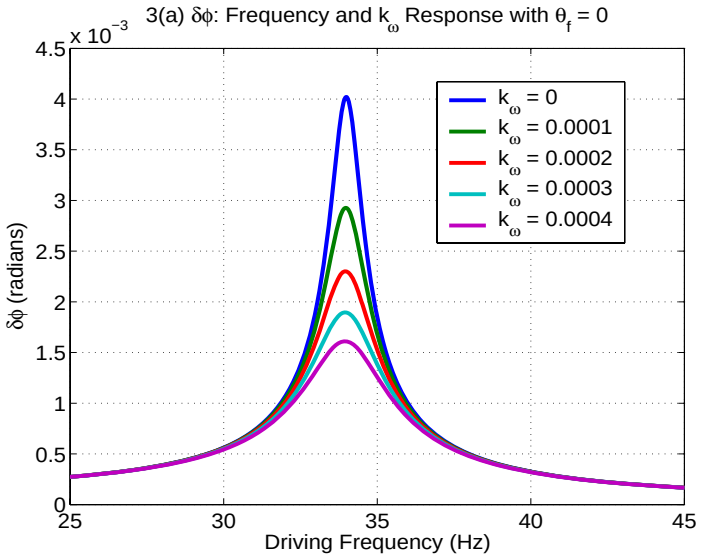
Resonance Control
(Hardware Schematic)

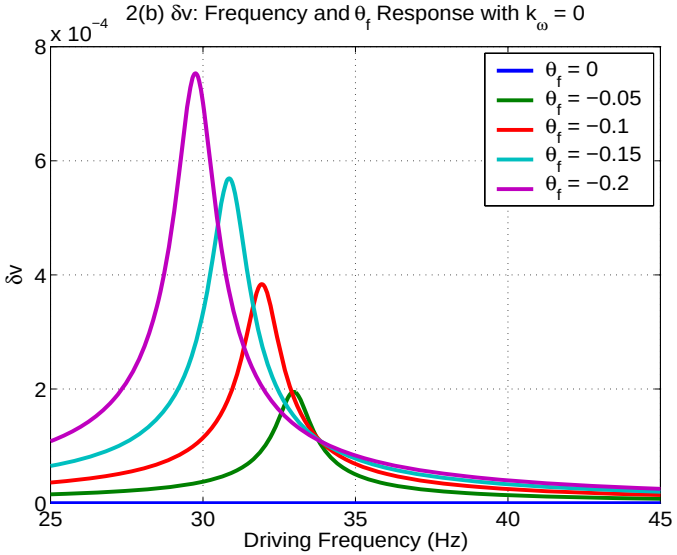


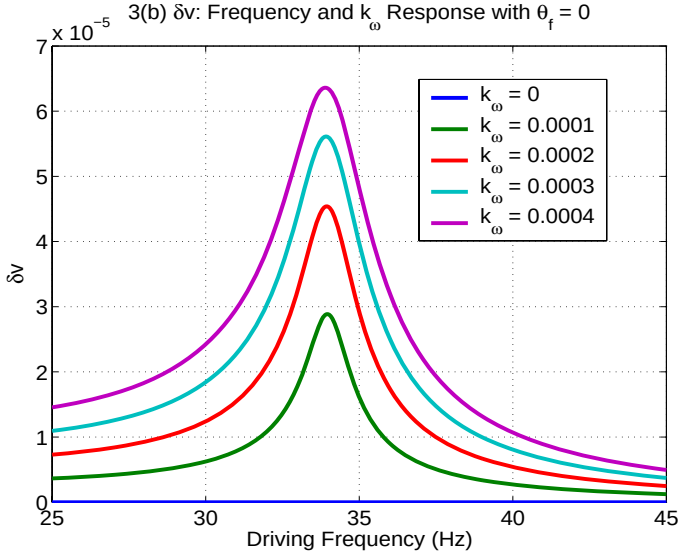
Electronic Damping

Comparison of Phase (left) vs. Frequency (right) Feedback for a Single Mechanical Mode at 34 Hz

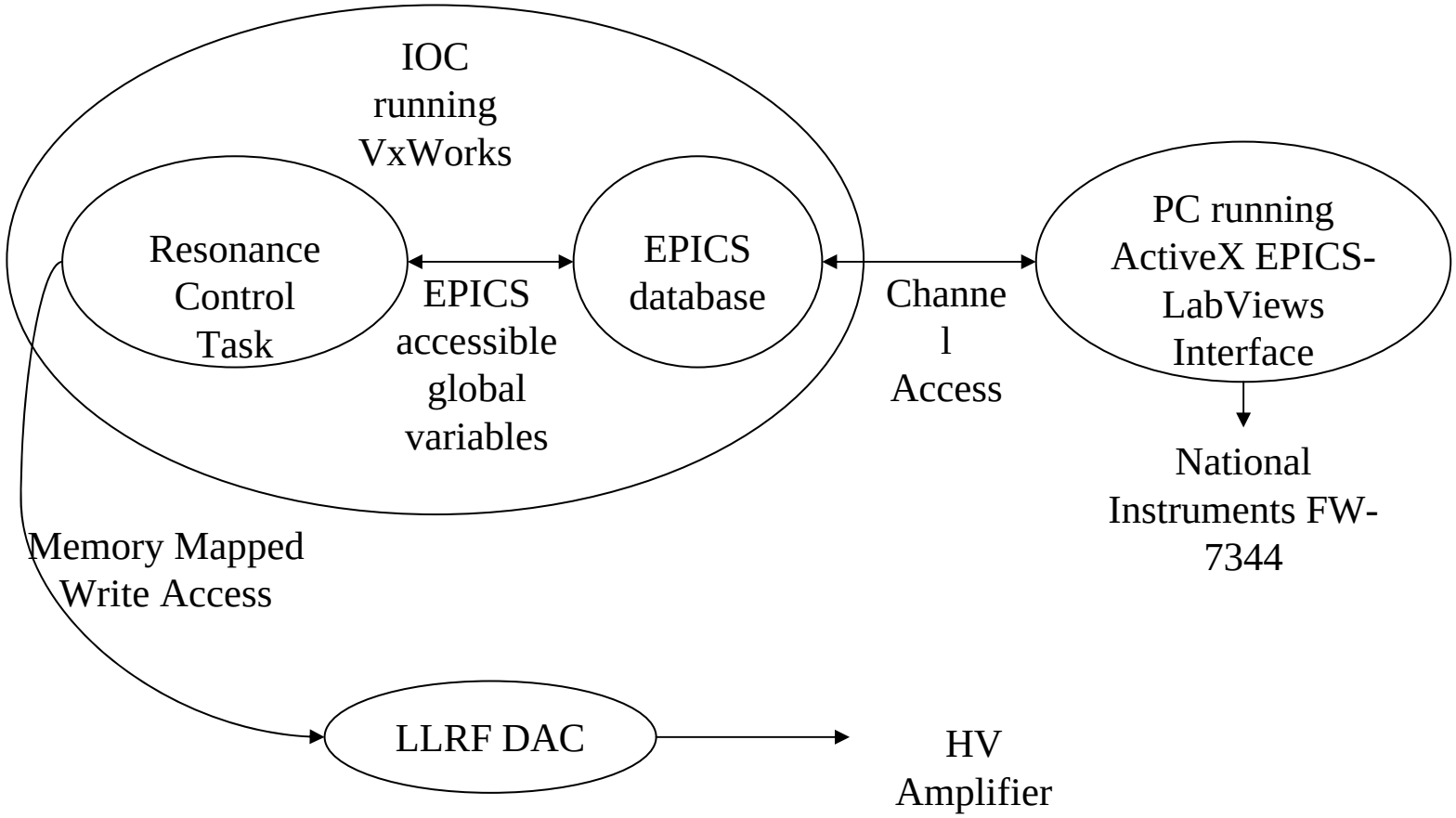








Resonance Control
(Software Layout)



Resonance Control

- Prototype system
  - Based on two systems
    - Cornell's digital LLRF system under development for its proposed ERL and CESR-c RF systems
    - Auto-track resonance tacking system used for the CEBAF 6 GeV cavities
  - vxWorks-based task
    - memory mapped write access to DAC to high voltage amplifier for piezoelectric tuner
    - communicate through EPICS and ActiveX EPICS-LabViews interface to mechanical tuner system
- Ready for testing in Cryomodule Test Facility

Digital LLRF subsystems