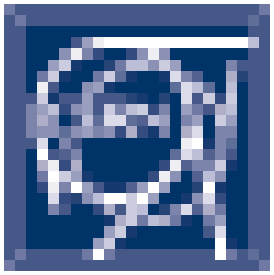

Contribution ID: **26** Type: **invited**

Characterization of SNS low-level RF control system

Wednesday 12 October 2005 12:30 (20 minutes)

A single high-density FPGA XC2V1500 plus 14-bit ADCs/DAC and 128Mb SRAM forms the digital hardware platform of SNS low-level RF control system. The carefully designed HDL implementation has limited controller latency under 150 ns (6 clock cycles) which allows the possibility for obtaining a rapid real-time feedback control. Given the typical 1 us external loop delay , a small signal control bandwidth over 100kHz has been demonstrated on a NC cavity with a classic SISO/P-I control only configuration. The large on-chip dual-port RAM and logic as well as the off-chip SRAM supports the implementations of more sophisticated dsp/feed forward algorithms required for pulsed super-conducting LINAC.

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Session Classification: Talks Session 3