An IQ-based low-level RF prototype for ALBA

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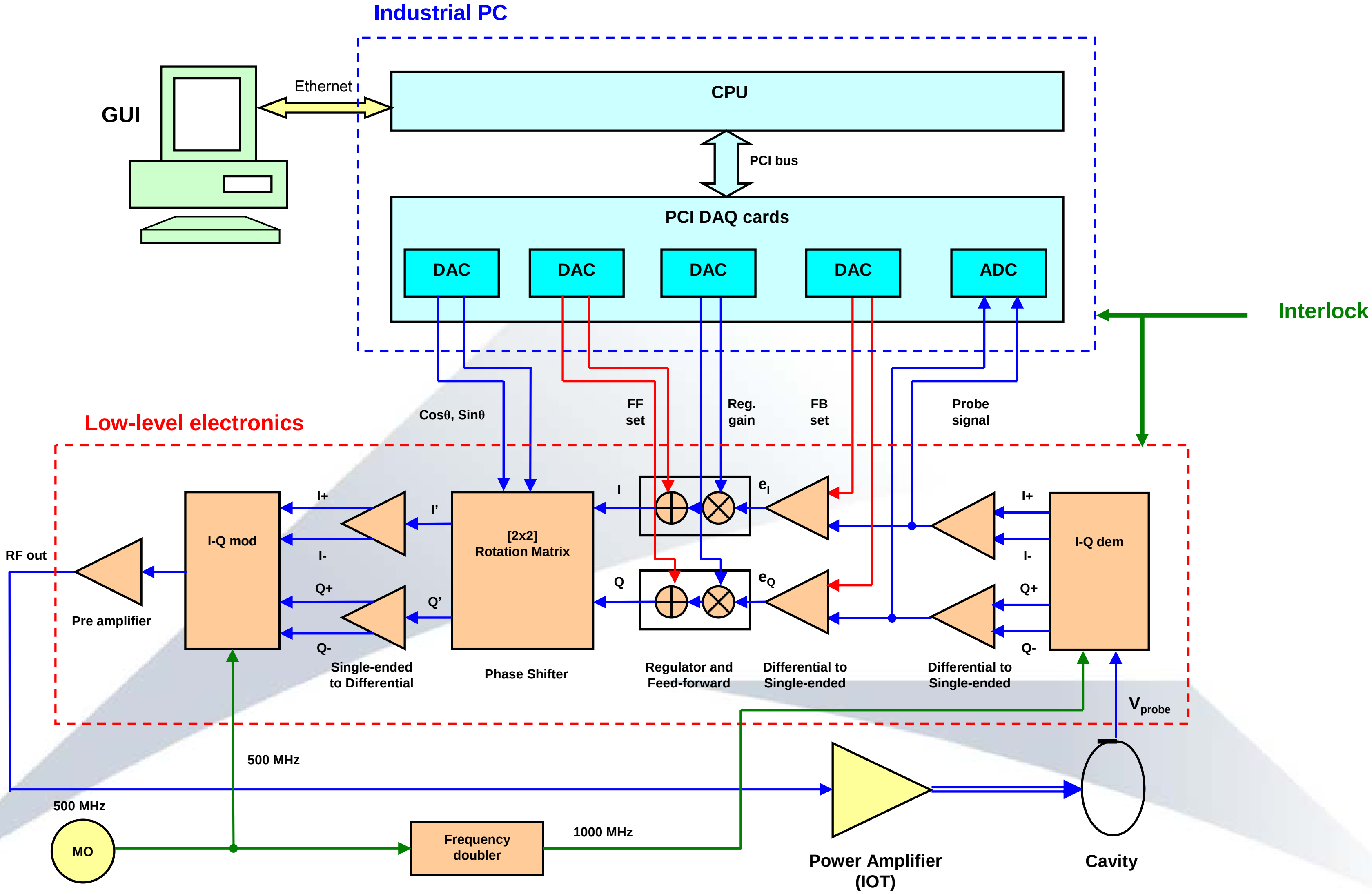
Design of the analog LLRF prototype



Specifications

Measured EU cavity parameters (E. Weihreter)

Nominal frequency	499.65	MHz
Tuning range	2	MHz
Shunt impedance	3.1	MΩ
Unloaded Q	26692	
Waveguide cut-off	615	MHz

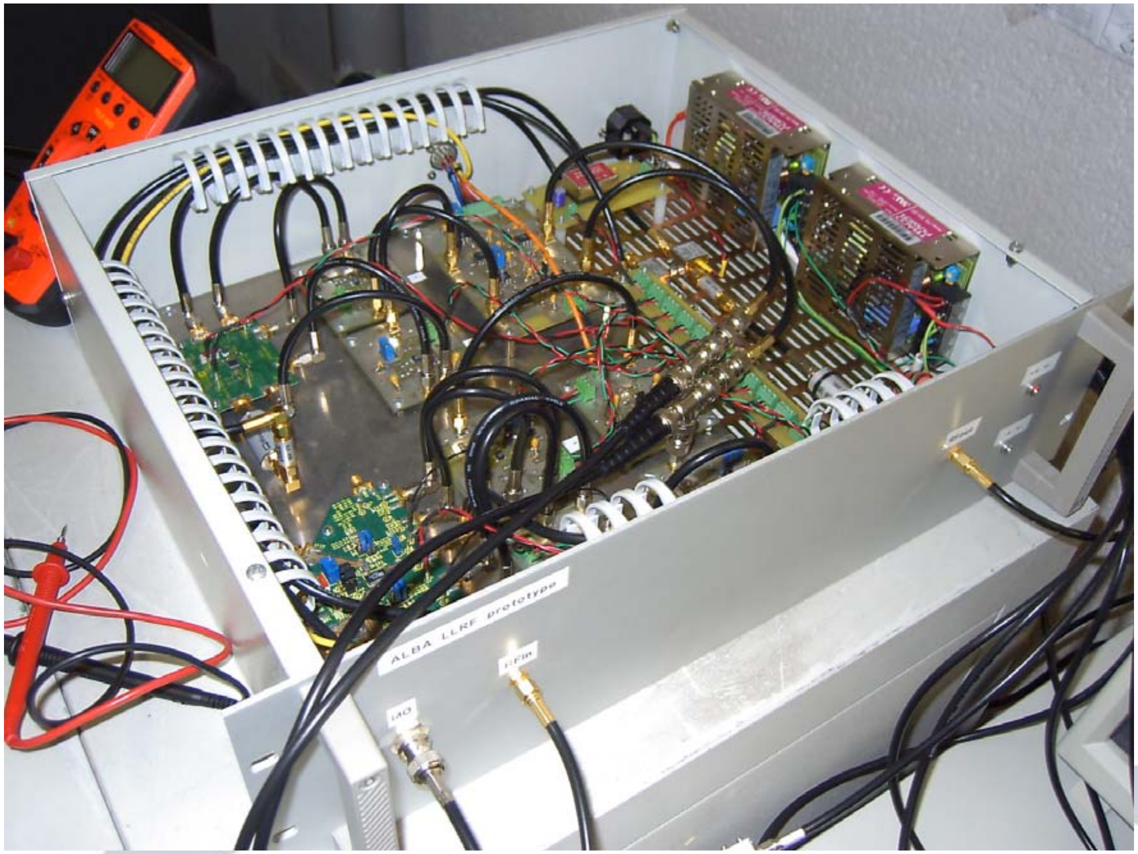
ALBA storage-ring RF specifications

Master oscillator frequency	500	MHz
Cavity nominal frequency	499.654	MHz
Phase stability	±1	deg
Amplitude stability	±1	%
No. of cavities	6	
RF power (per cavity)	150	kW
RF voltage (per cavity)	600	kV
Overvoltage factor	2.8	
Synchronous phase	159	deg

ALBA LLRF specifications (analog prototype)

Phase loop			
	Design	**Practice**	
Type	Analog IQ with 'P' regulator	Analog IQ with 'P' regulator	
Bandwidth	1-2	~1 (measured)	MHz
No. of bits	16	16	Bits
DAC throughput	100	100	kHz
Phase stability	±1	?	deg
Amplitude loop			
	Design	**Practice**	
Type	Analog IQ with 'P' regulator	Analog IQ with 'P' regulator	
Bandwidth	1-2	~1 (measured)	MHz
No. of bits	16	16	Bits
DAC throughput	100	100	kHz
Amp. stability	±1	?	%
Tuning loop			
	Design		
Type	IQ dem and PCI tuner driver		
Bandwidth	~100		Hz
Tuning range	2		MHz
Tuning resolution	0.1 - 1		kHz

Current status

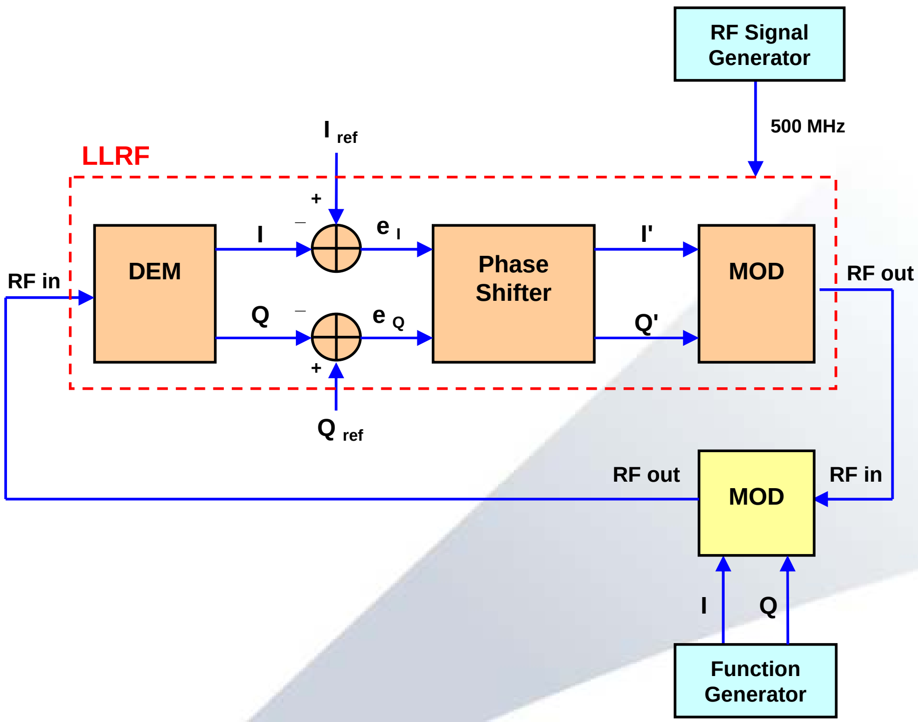


The low-level electronics

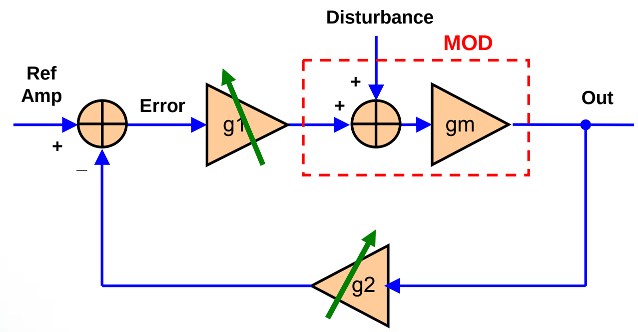
The industrial PC

The mockup cavity

Closed-loop test setup for amplitude and phase regulation



Setup for closed-loop test

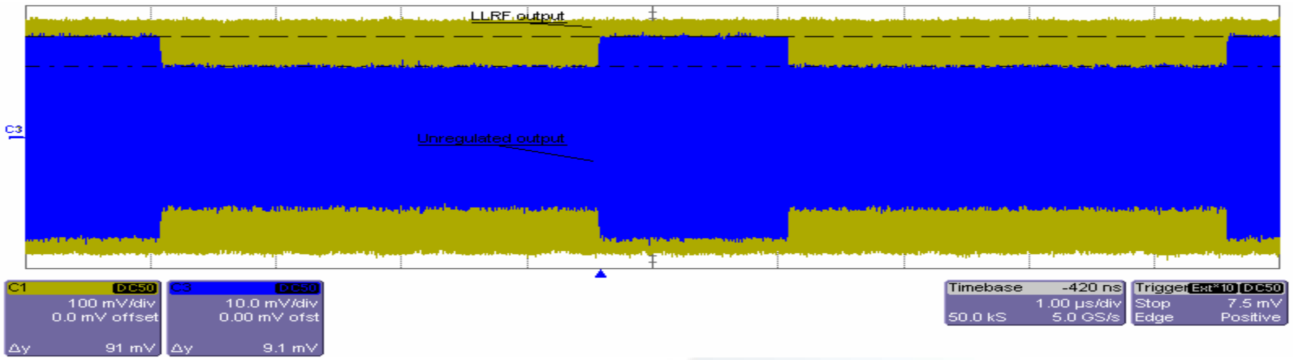


$$Out = ref.\frac{g1.gm}{1+g1.g2.gm} + dist.\frac{gm}{1+g1.g2.gm}$$

Simplified model of the loops

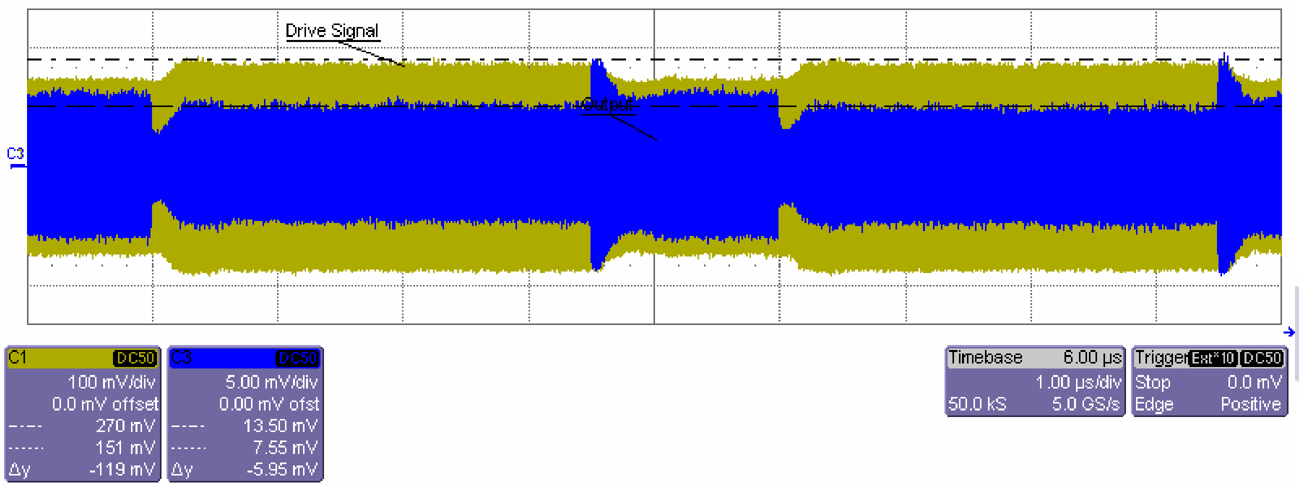
Closed loop test – amplitude regulation

→ 1 µs ←



Amplitude without regulation

Regulation



Amplitude with 'P' regulation

Steady state output

Measured:	7.6 mV
Calculated:	7.5 mV

Ripple

Measured:	~2 mV
Calculated:	3.5 mV

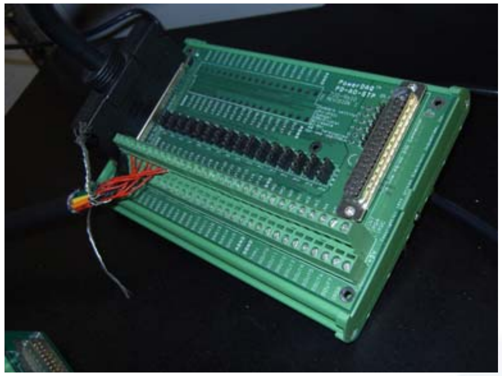
Loop delay

Measured:	~200 ns

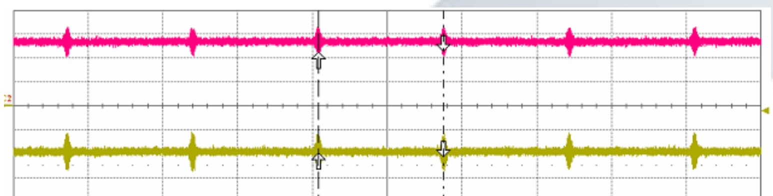
Band width

Measured:	~1 MHz

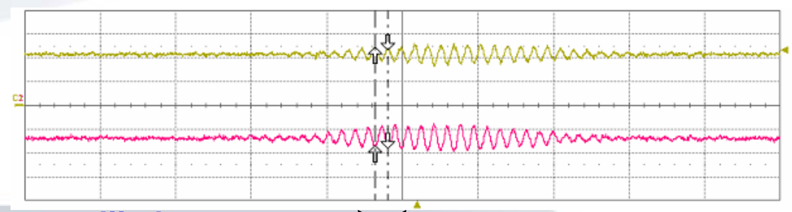
Main problems we have faced



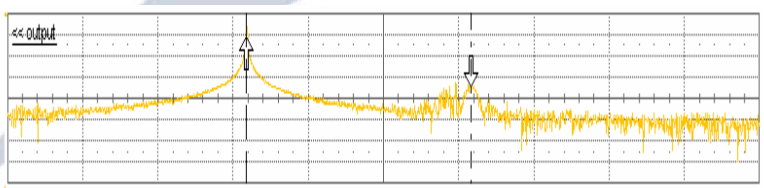
	Problem		Solution
1.	Noise and disturbance	=>	Careful PCB design, filtering, grounding, good components, shielding, etc.
2.	DC offsets	=>	Variable resistors for DC adjust
3.	Voltage ranges of the ICs	=>	Careful circuit design



Spikes → f= 300 kHz ←

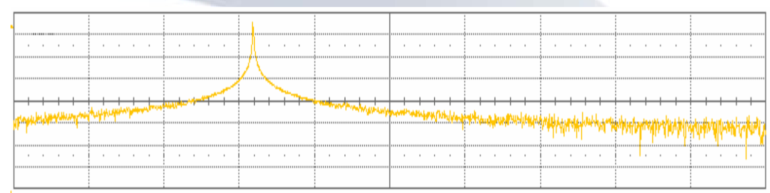


Oscillations → ← f= 114 MHz



500 MHz 614 MHz

Filtering



Next steps

1. Use of a 'PI' regulator instead of 'P' to eliminate the steady-state error
2. Noise/disturbance reduction
3. Closed-loop tests with the mockup cavity for amplitude and phase regulation