Complex Digital Circuit Design for LHC Low Level RF

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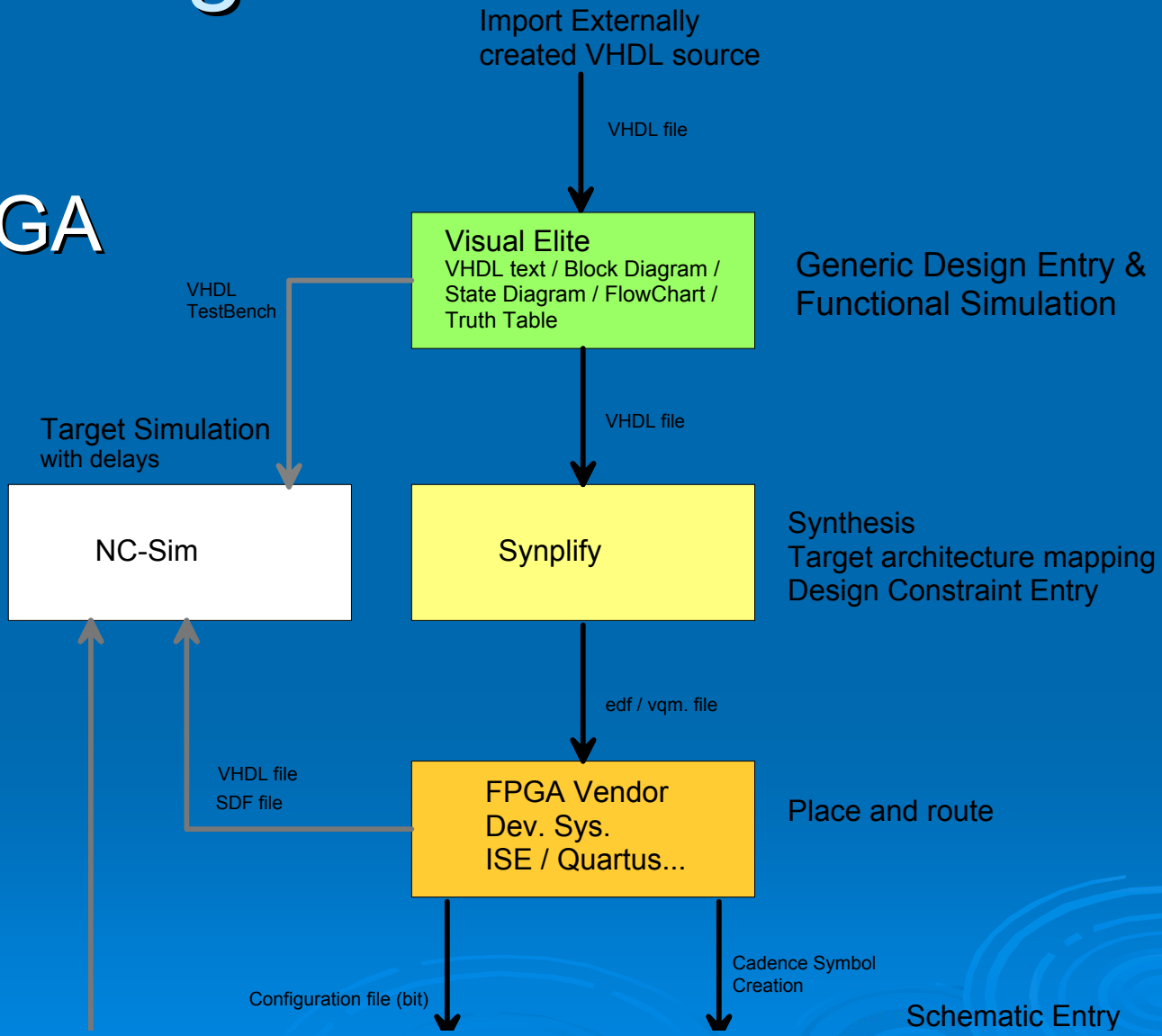
Presentation

- *Design Flow Overview*
  - FPGA Design Tools
  - PCB Related Tools
- Implementations
  - Digital Signal Treatment Modules
  - General Controls Modules
- Acquisition Examples
  - Tuner Calibrate Sweep
  - Tuner Stepping Noise Observation

Design Flow Overview 1/2

- FPGA

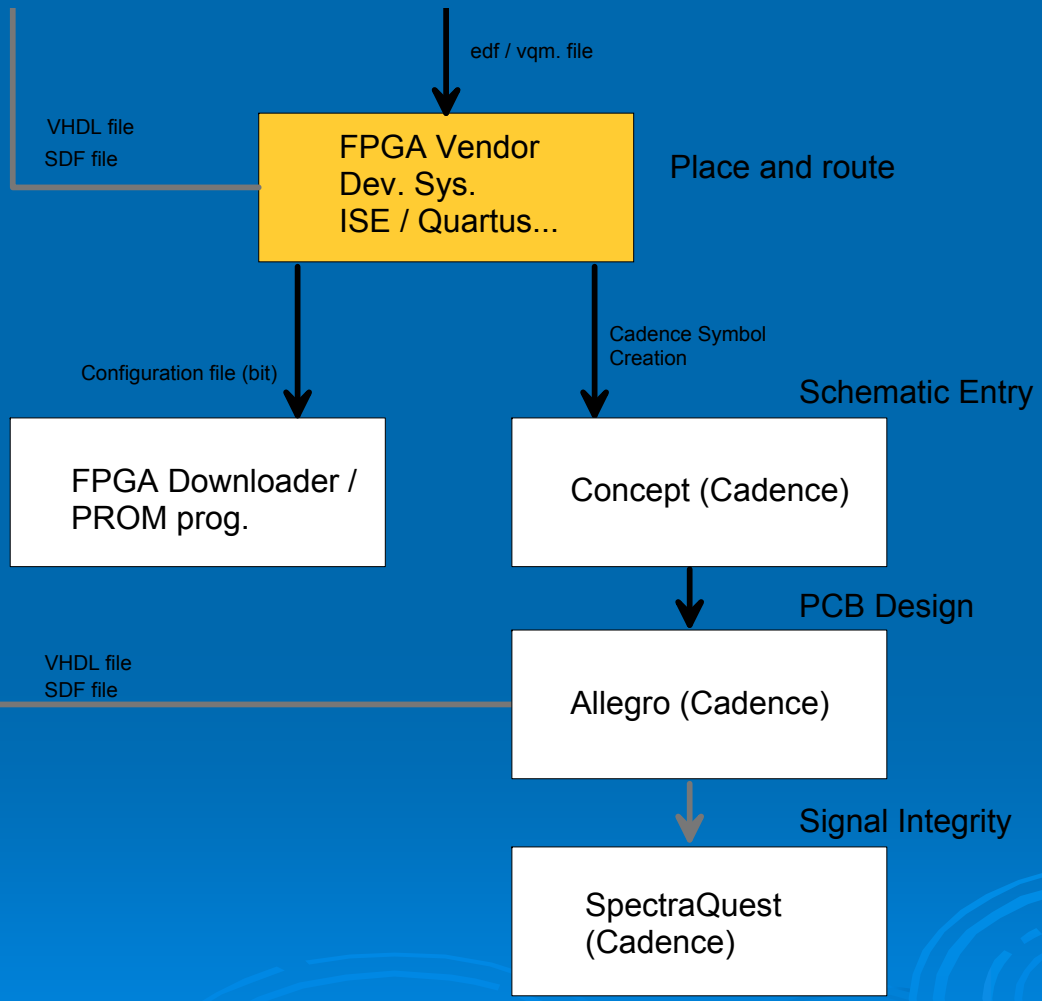


Visual Elite

- Advantages Visual Elite tool
  - Generates Device independent portable VHDL code.
  - Code reusability
  - Graphical Design Builder
  - Graphics to text, text to graphics conversion
  - Powerful auto-documenting creates html
- Disadvantages
  - Need a synthesizer AND the FPGA dev. Sys.
  - Multiple work directories, more complex environment
  - Need to include Device / Vendor specific library if device specific features are required (reducing portability)

Design Flow Overview 2/2

- PCB



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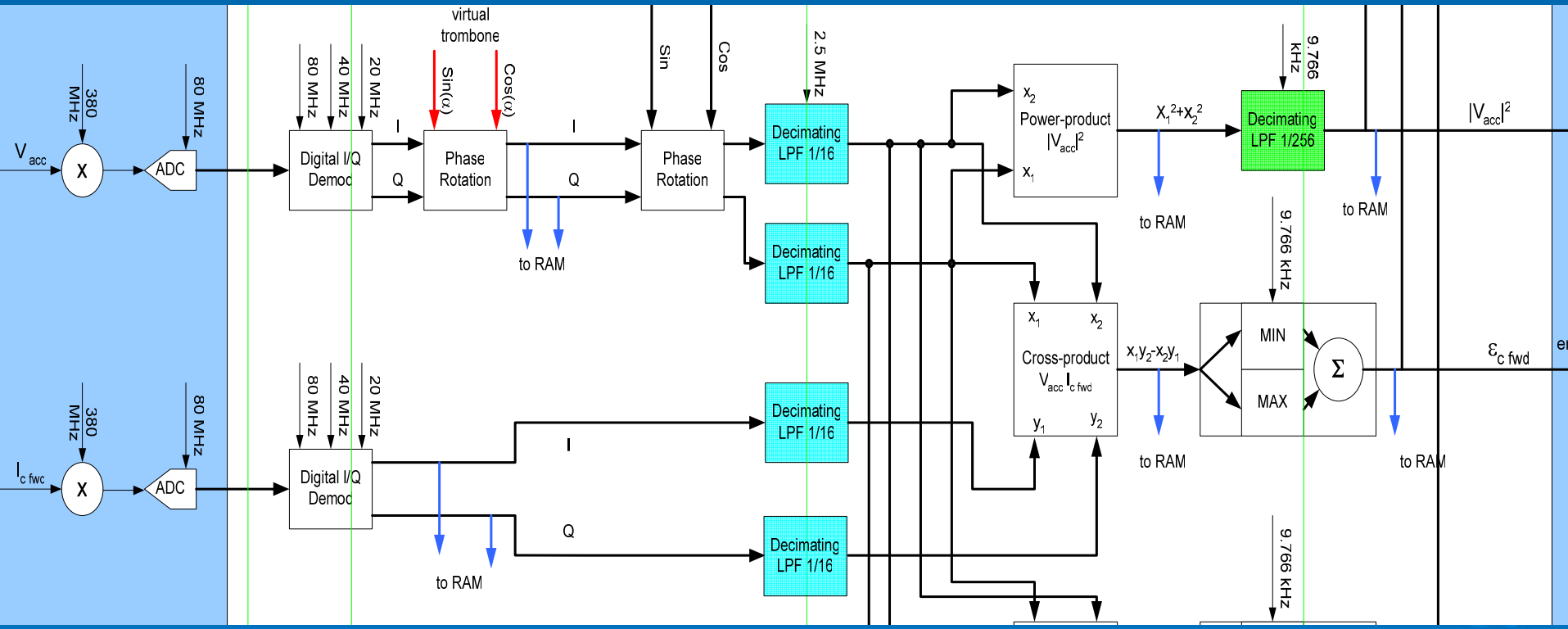
Tuner Loop Module [7],[8]

- Vacc Reference Channel &
- IcFwd Channel

to DSP tuning algorithm:

$$(\Delta f/f_0)_{n+1}=(\Delta f/f_0)_n+a\,\varepsilon_n/|V_{acc}|^2$$

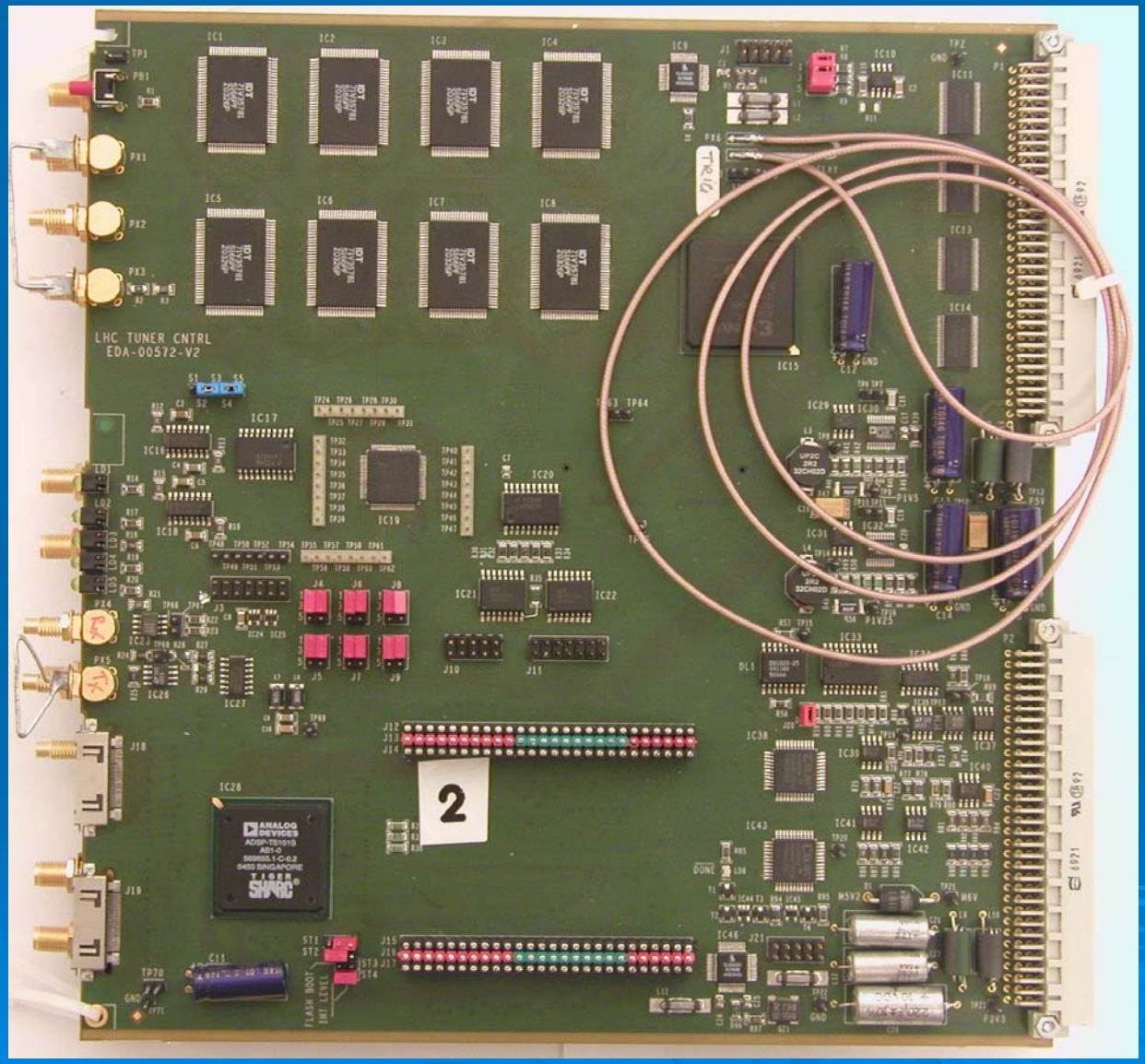


80MSPS 40MSPS 2.5MSPS 9.766kSPS \ 1.22kSPS

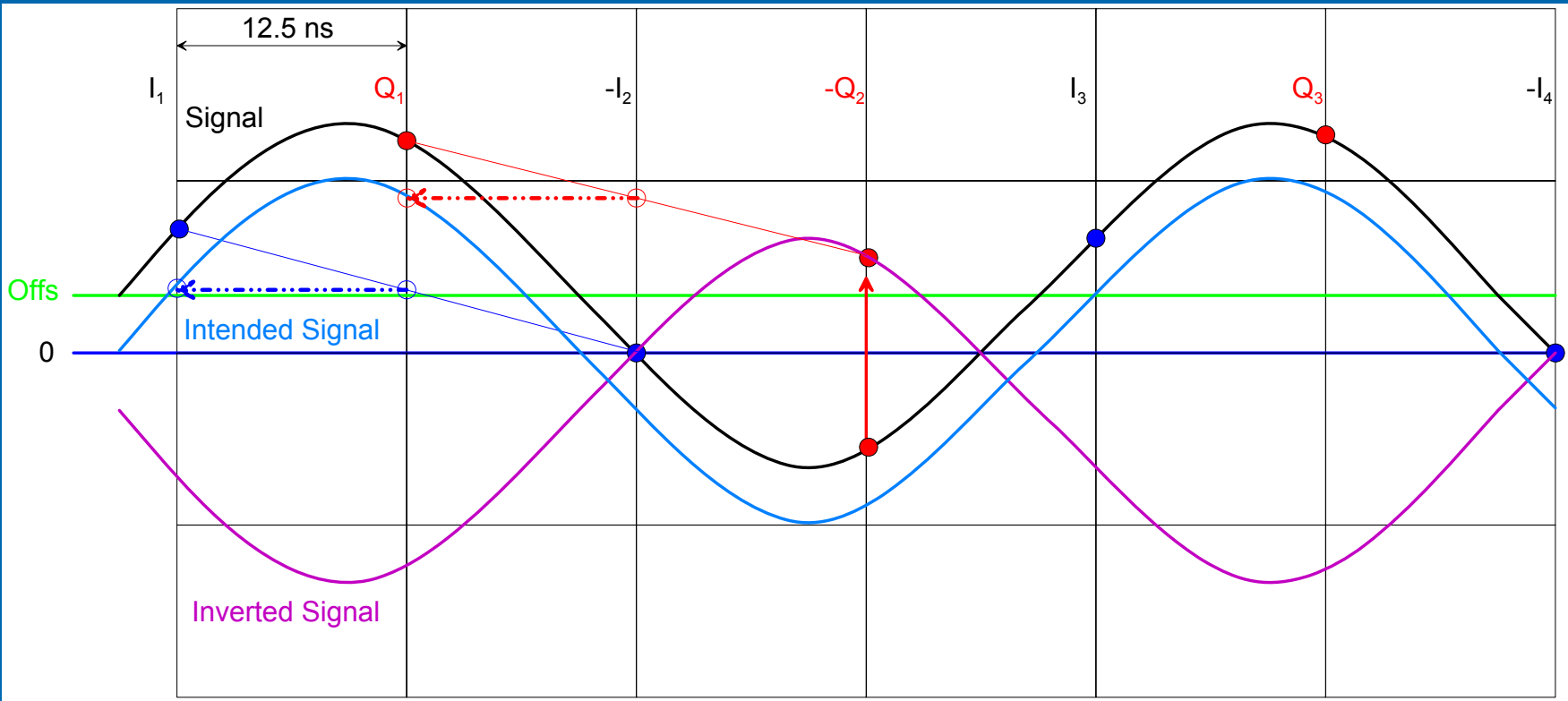
FPGA: XC2V2000-6FG676C

DSP: ADSP TS101S BGA625

Tuner Loop Module



Digital I/Q Demodulator 1/2 [1]

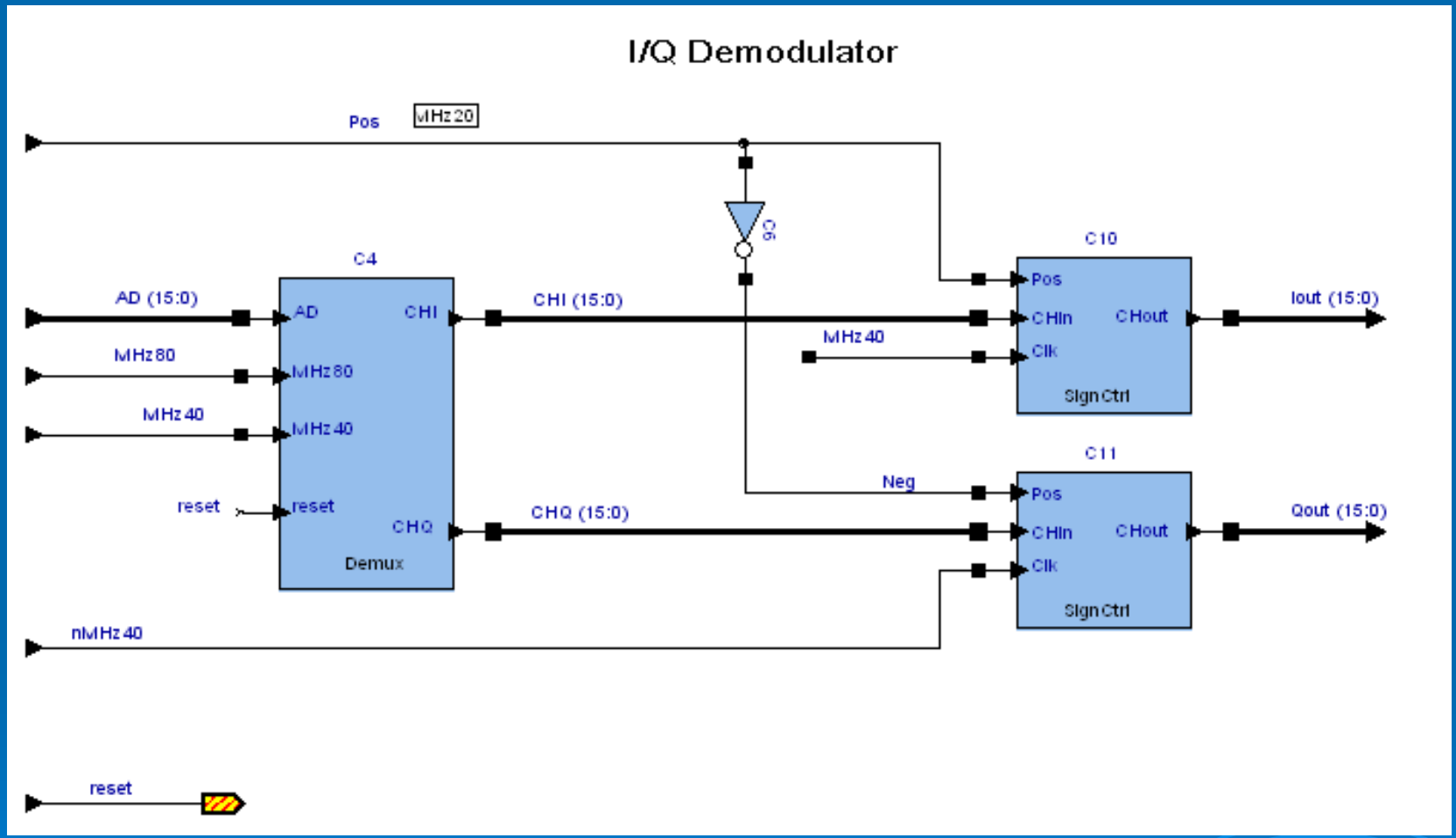


Moving Average over 1 cycle
for PM & Observation Memory
Full 40MSPS rate & Offset compensation!

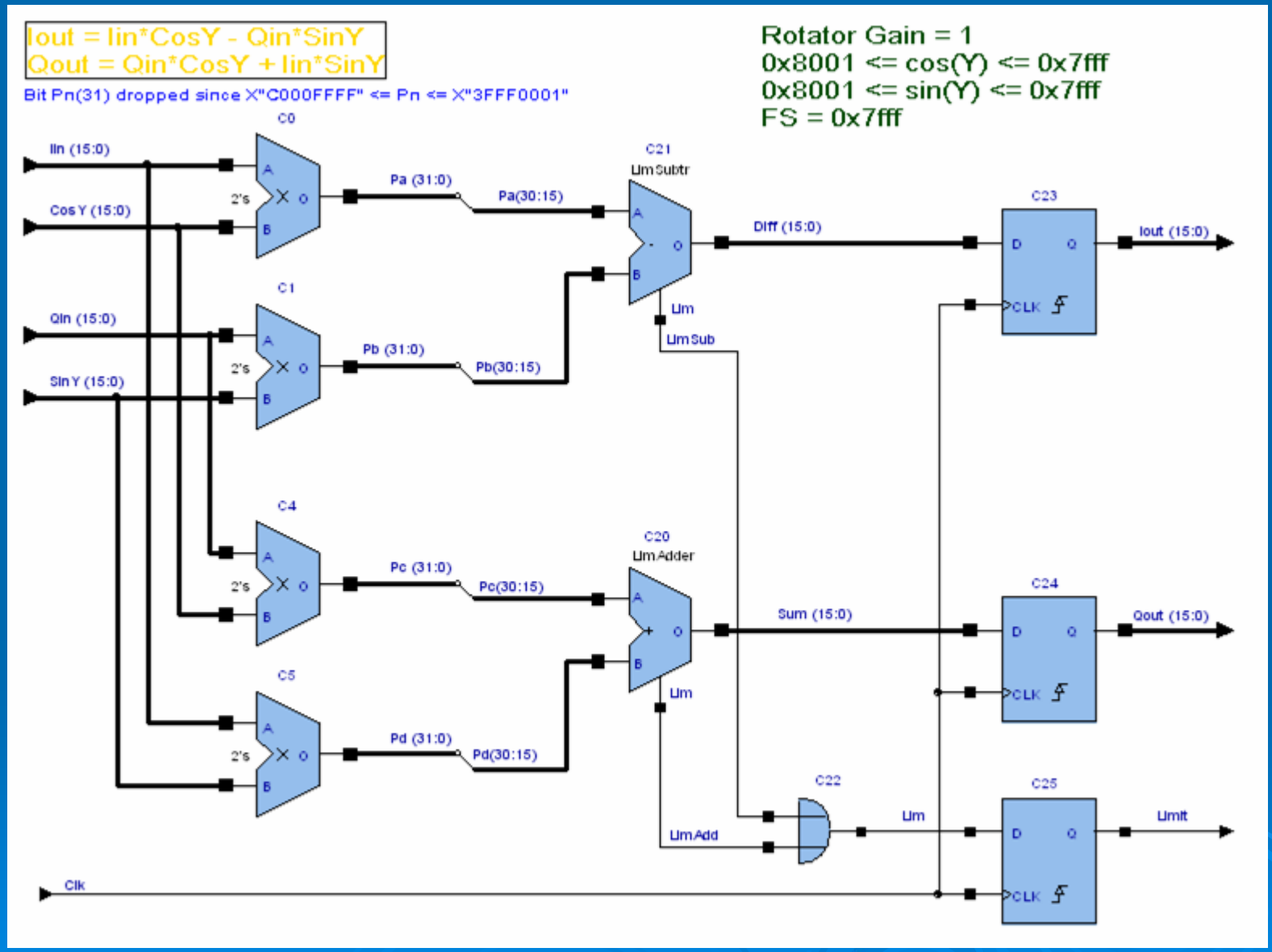
$$\begin{cases} I'_i = \dfrac{(I_i + Offs) - (-I_{i+1} + Offs)}{2} \\ Q'_i = \dfrac{(Q_i + Offs) - (-Q_{i+1} + Offs)}{2} \end{cases}$$

TunerCtrl applies 2 stage CIC with R=16 => Average over I/Q 16 (even) samples => Offset Cancelled.

Digital I/Q Demodulator 2/2

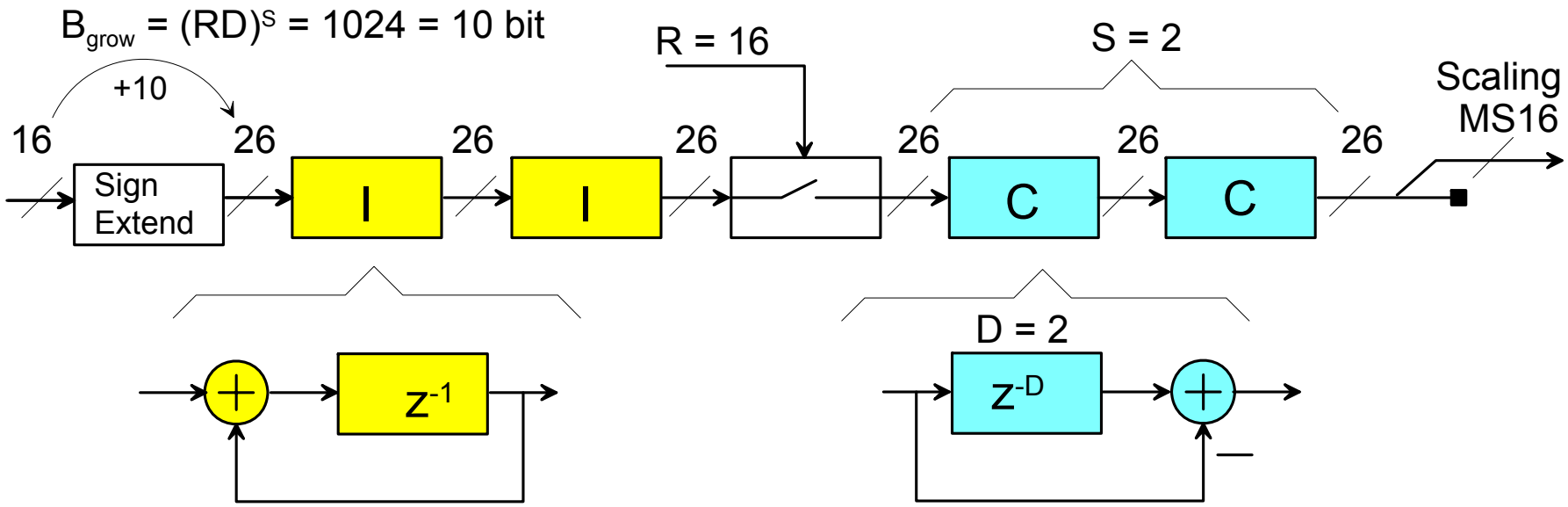


Phase Rotator



2 Stage CIC16 2/2 [3]

A 2 stage Decimate by 16 CIC filter



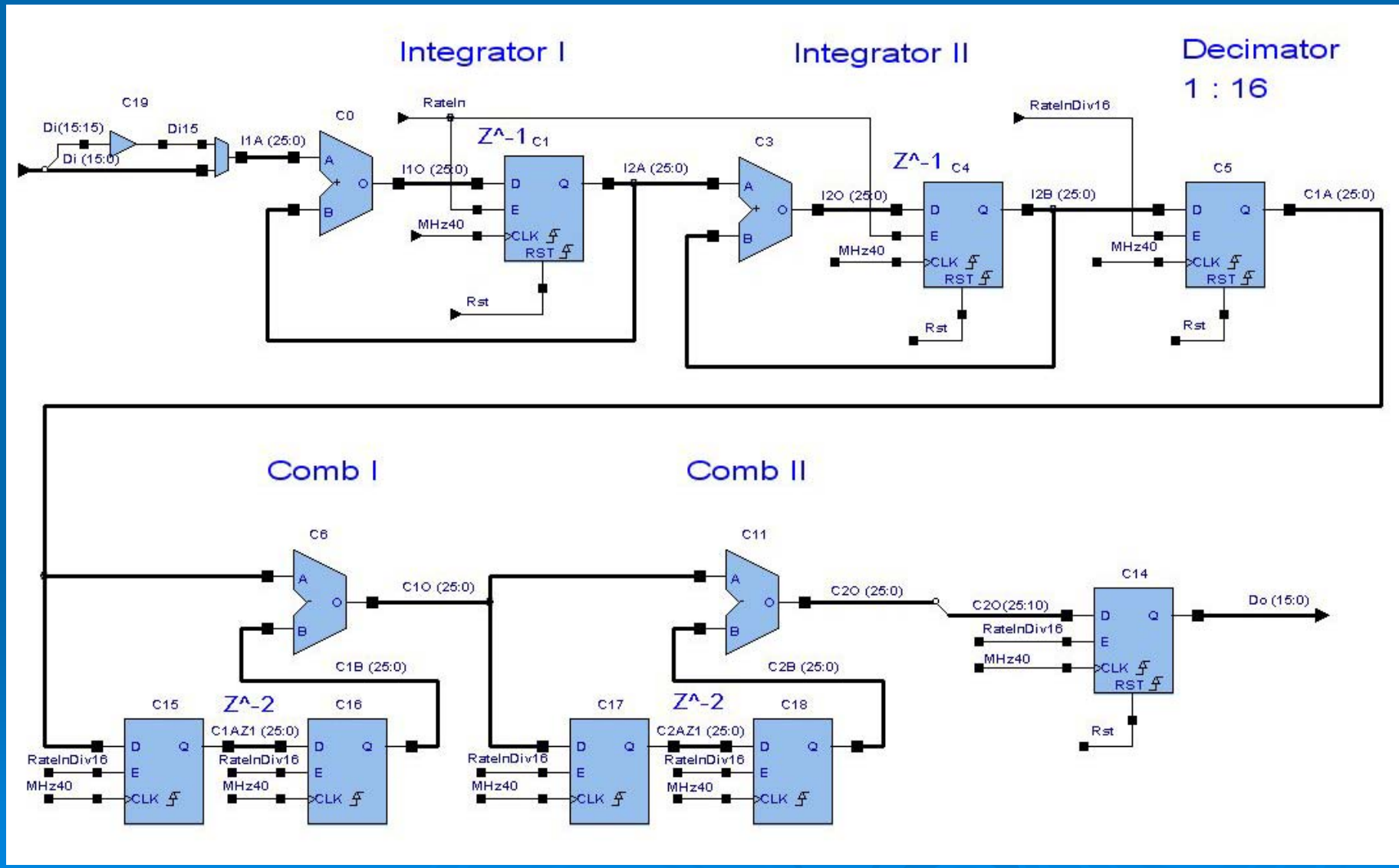
$$F(z) = \left[\frac{1 - z^{-RD}}{1 - z^{-1}}\right]^S = \left[\frac{1 - z^{-32}}{1 - z^{-1}}\right]^2$$

=> RDS (64) zeros and S poles (2)

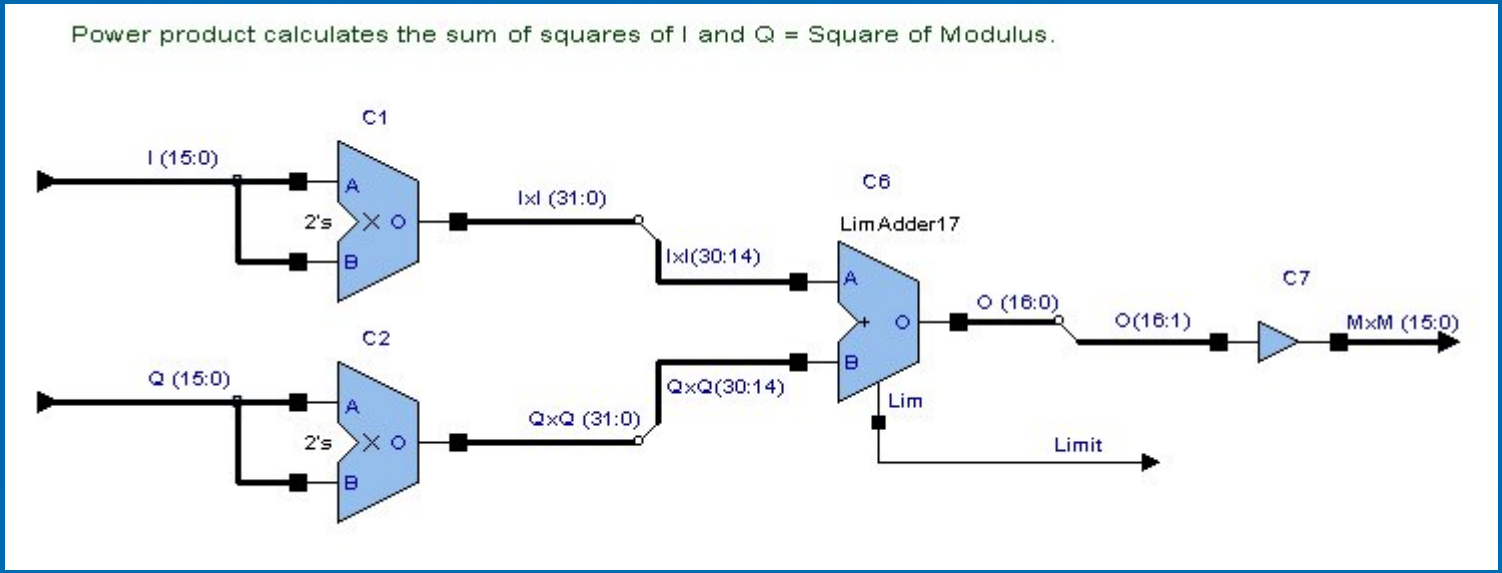
Resource economic solution for decimating filters.

Rise-time = 0.9 µs to allow LHC abort gap to remain visible

2 Stage CIC16 2/2

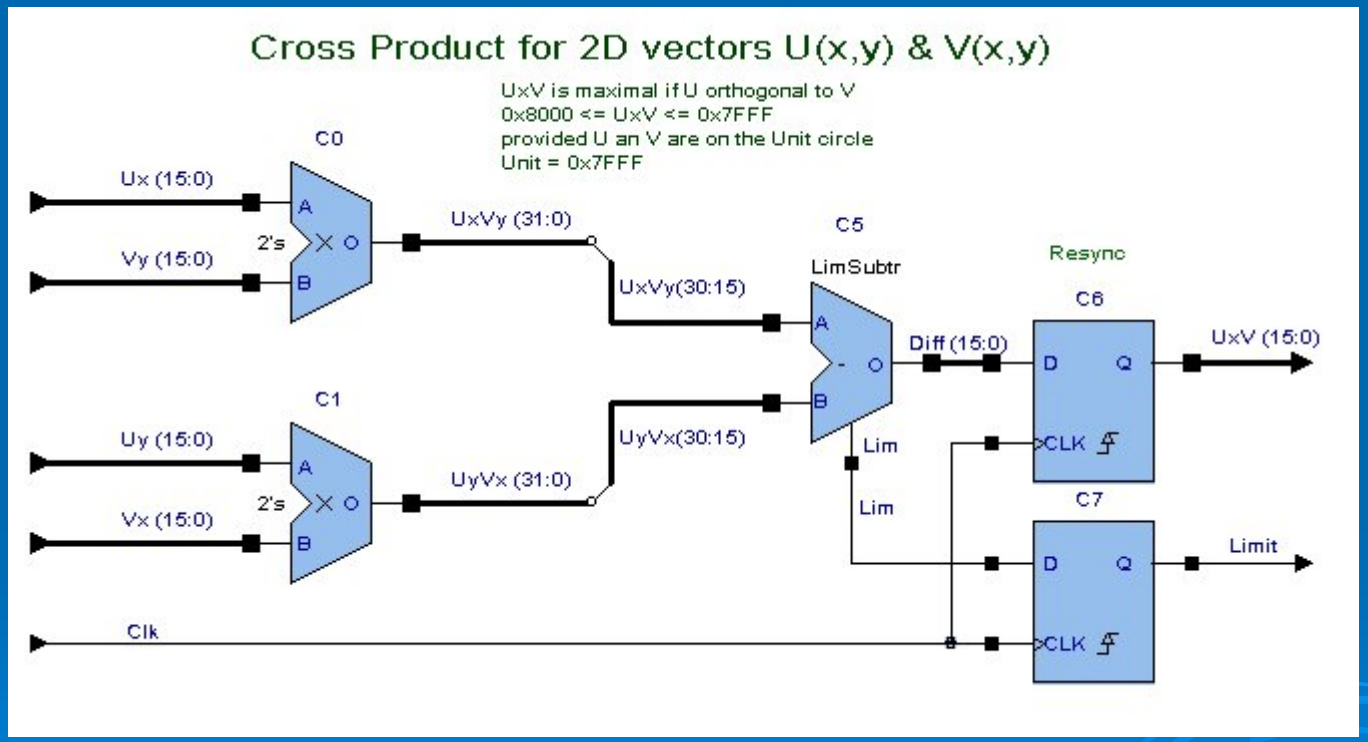


Power Product

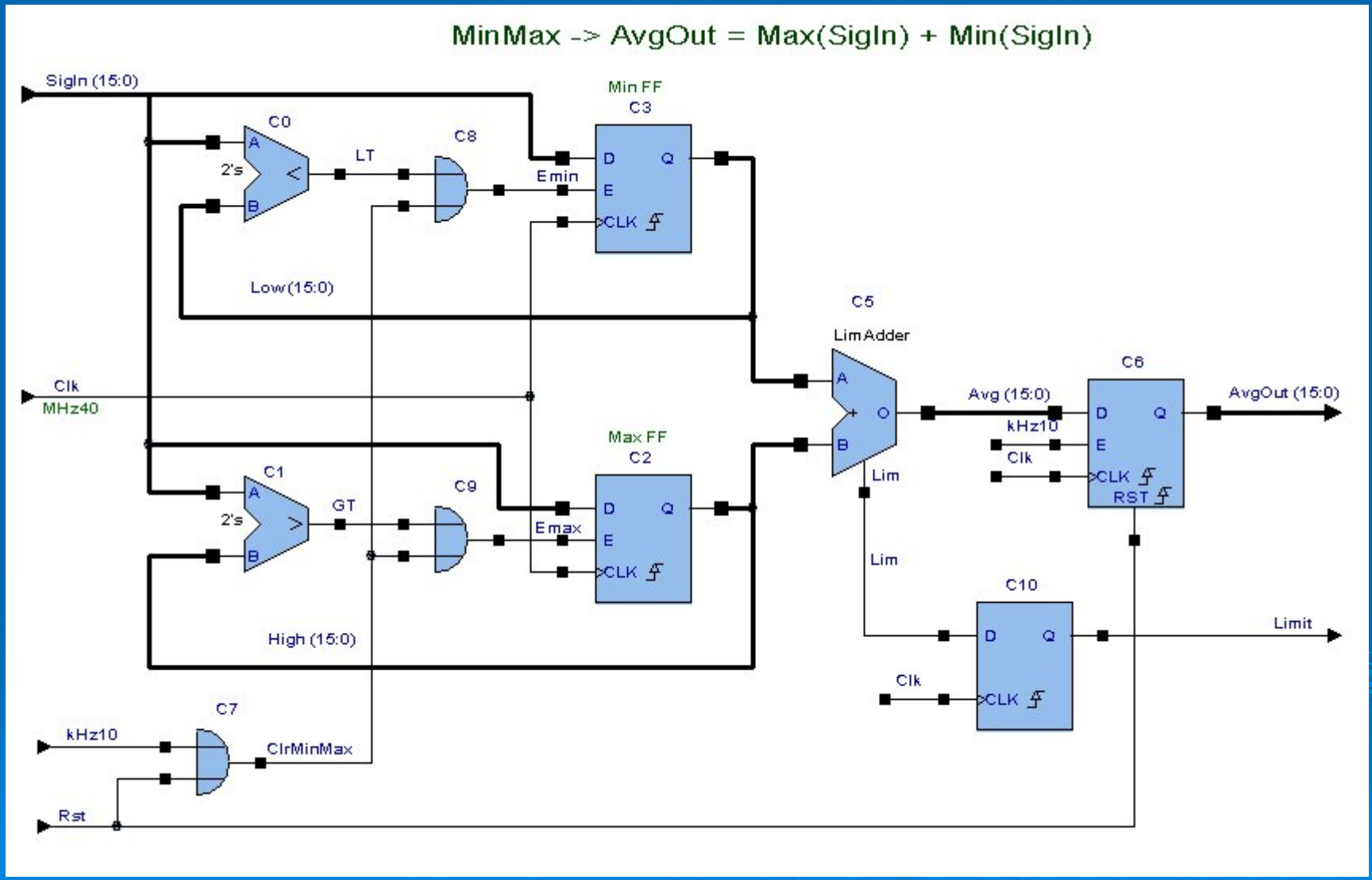


Cross Product as Phase Discri

- $u \times v = u_x v_y - u_y v_x$
- $|u \times v| = |u| \times |v| \sin\theta = \varepsilon$ IcFwd
- u = Vacc, v = IcFwd

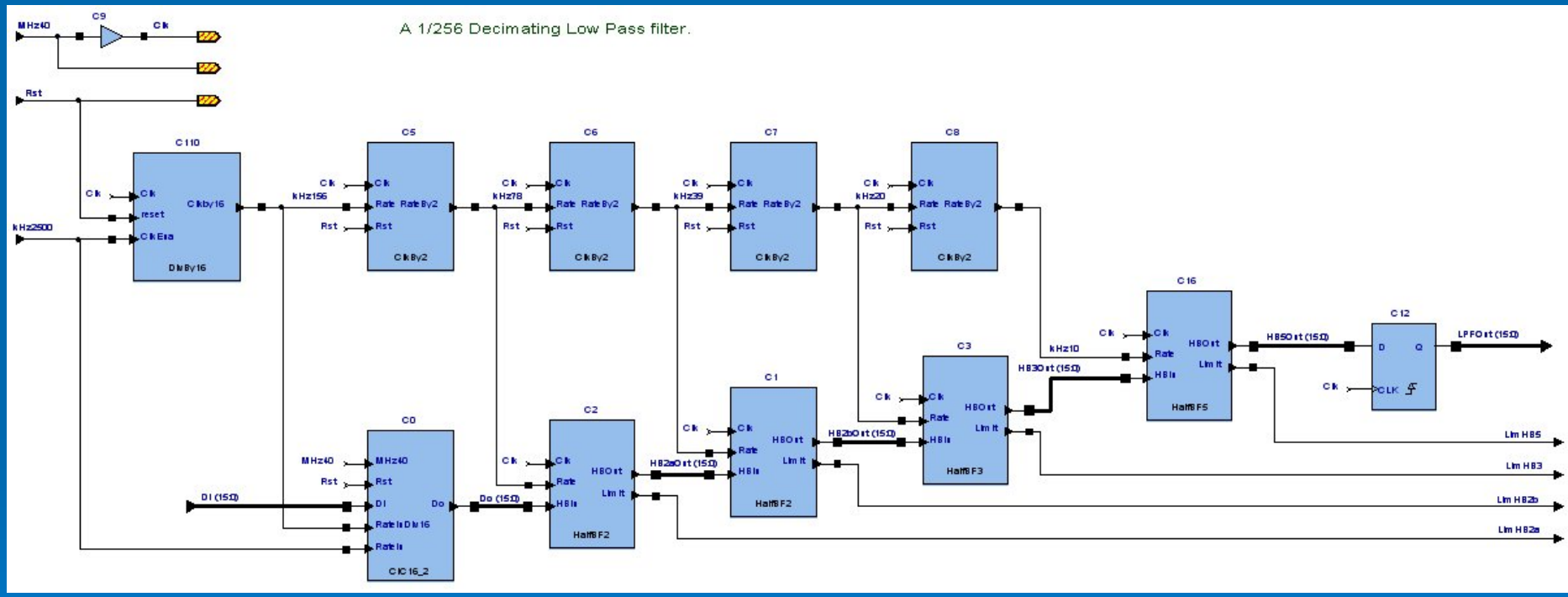


MinMax


MinMax -> AvgOut = Max(SigIn) + Min(SigIn)
SigIn (15:0)
C0
A
2's
<
B
LT
C8
Min FF
C3
D
Q
E
Emin
CLK
Low(15:0)
C5
LimAdder
A
+
O
B
Clk
MHz40
C6
Avg (15:0)
AvgOut (15:0)
kHz10
Clk
RST
Max FF
C2
C1
>
GT
C9
Emax
Lim
Lim
C10
Limit
High (15:0)
C7
kHz10
ClrMinMax
Rst

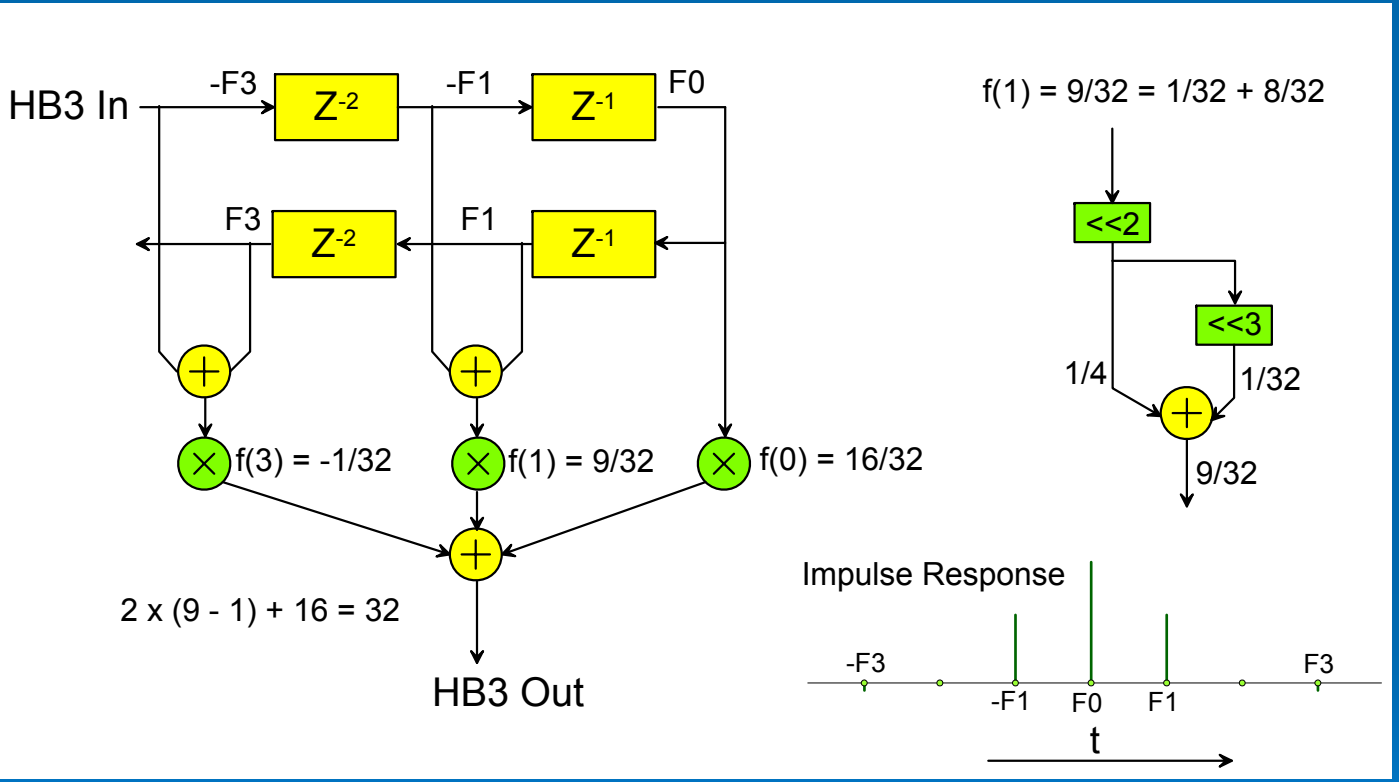
Decimating LPF256

- Cascade of CIC16_2, 2x F2, F3 & F5.
  calculates average |Vacc|^2 over an LHC turn.
- Design according to Goodman and Carey [2], [3]

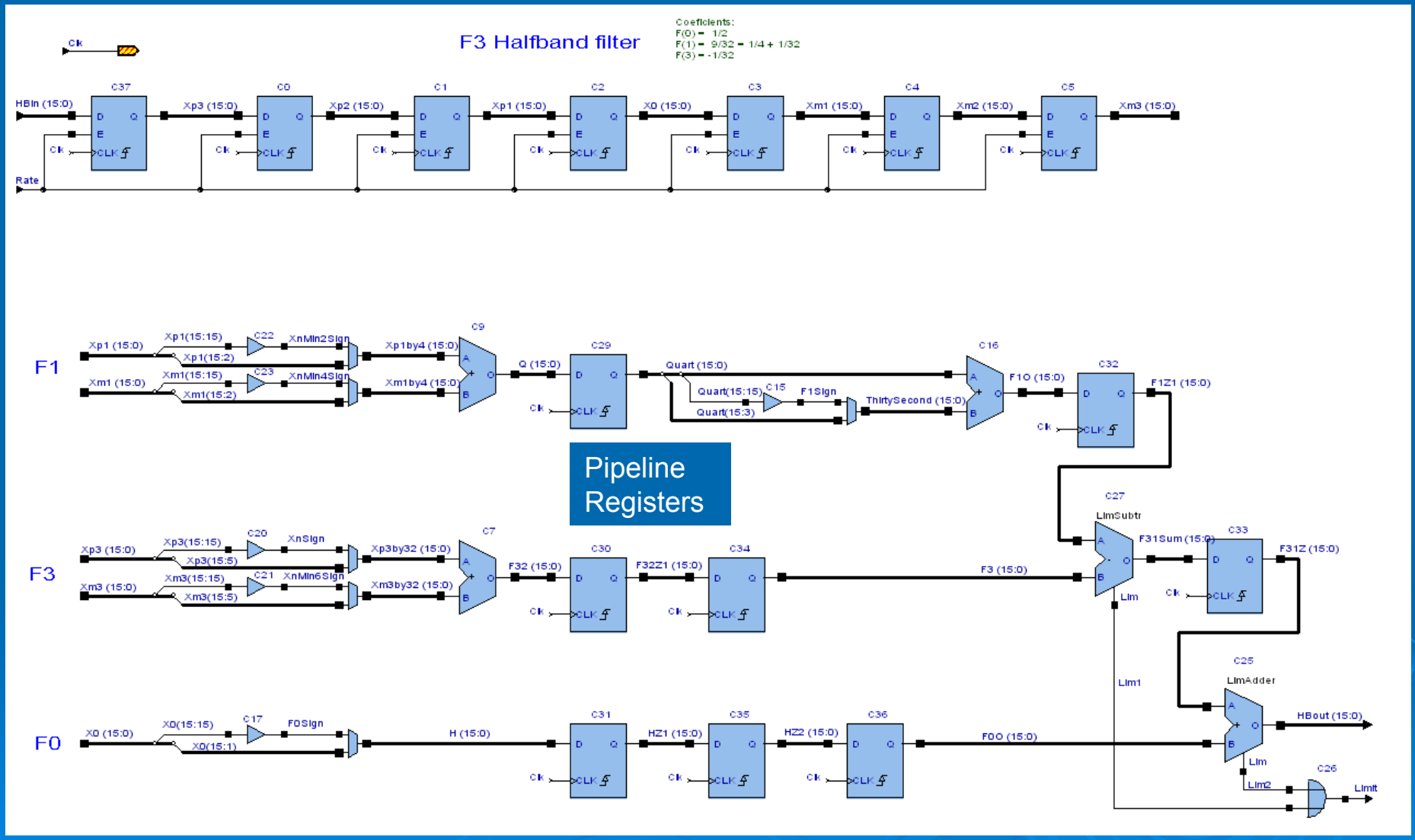


Rise-time = 200 µs ~ -60dB at LHC Frev of 11kHz

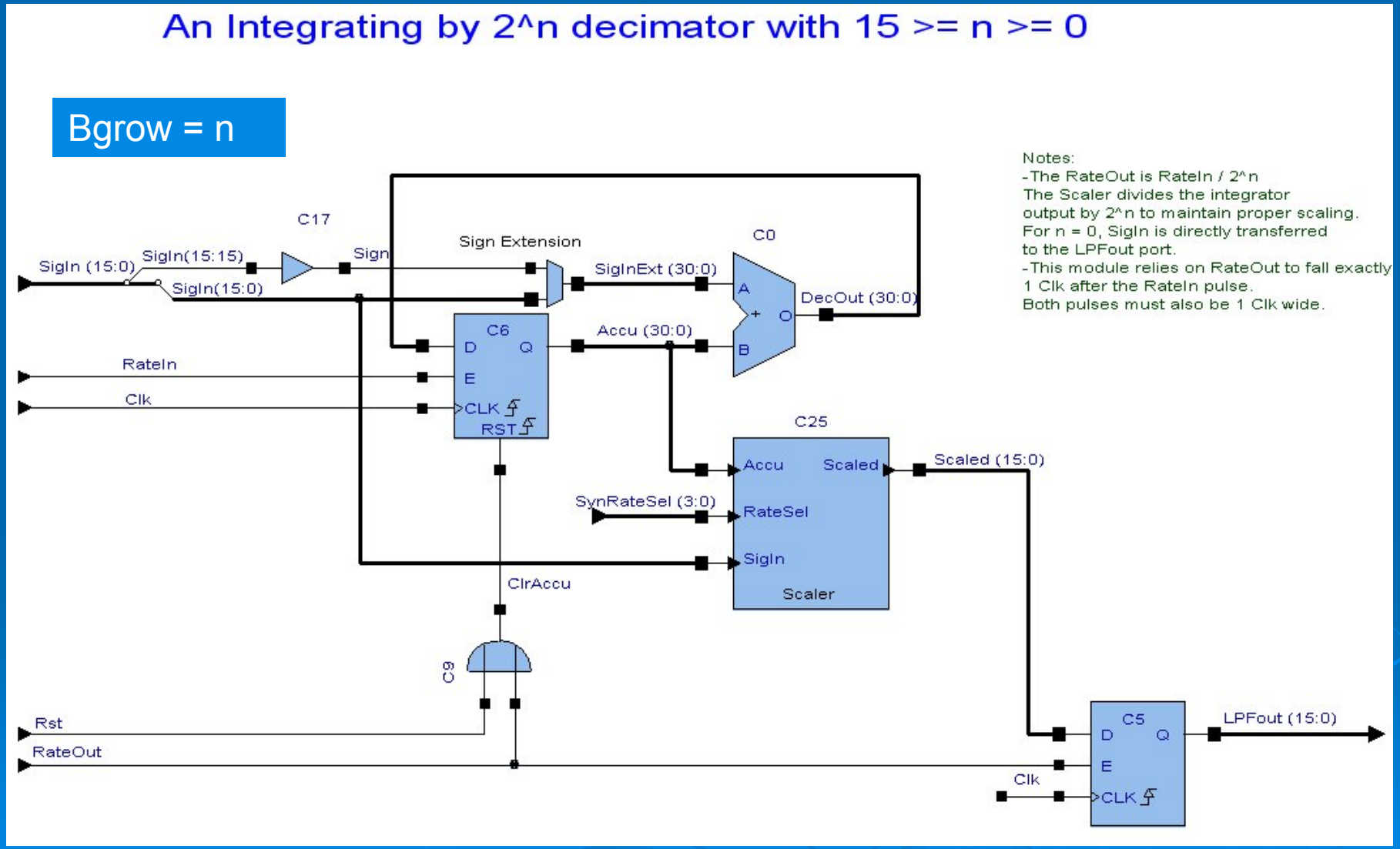
F3 Halfband filter 1/2



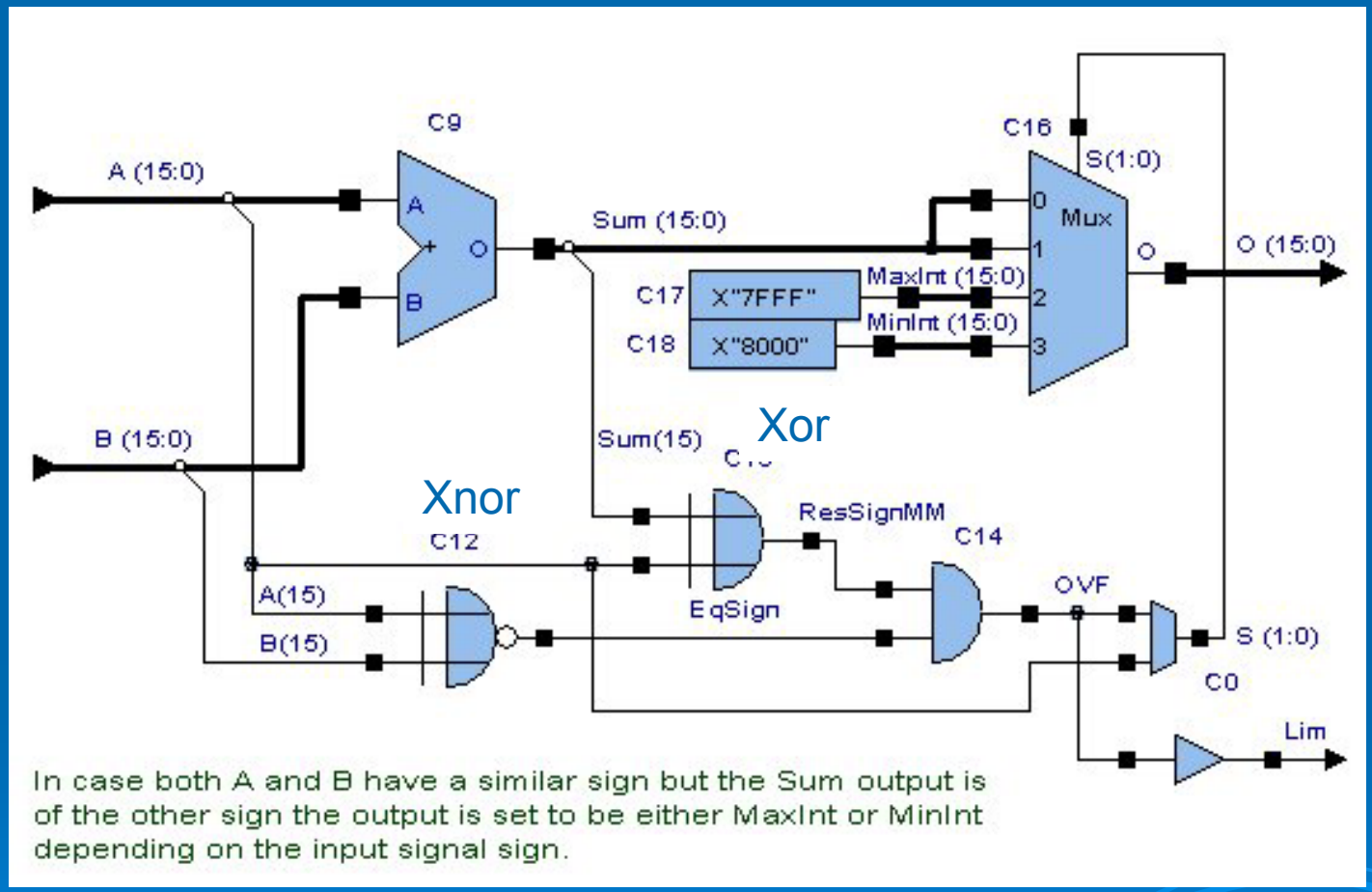
F3 Halfband Filter 2/2



Variable Rate Integrating filter for Observation Buffer



Limiting Adder



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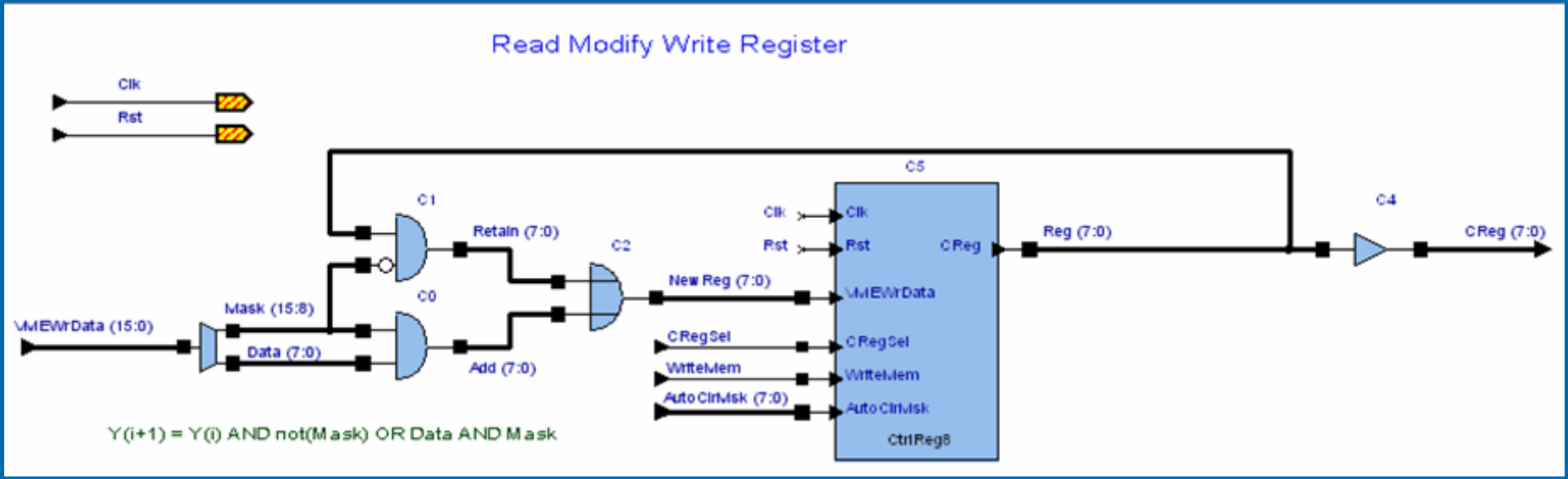
Read Modify Write Register

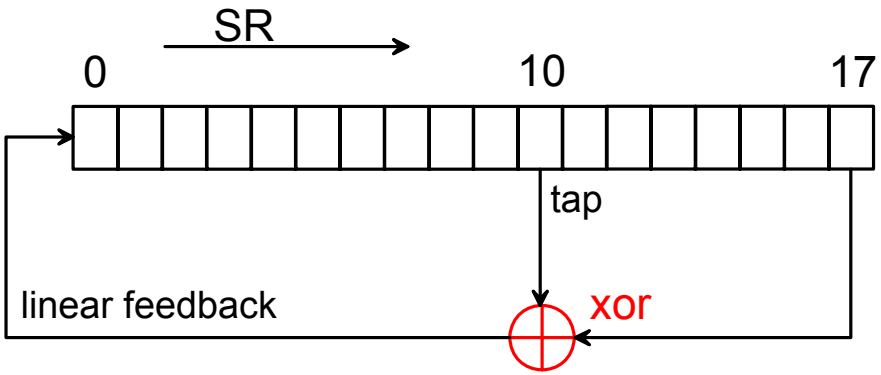


A Read Modify Write Register avoids data corruption if control register bits are used by different threads. The register is updated in 1 single access cycle.

LFSR Counter 1/2

18 bit LFSR example

Linear Feedback Shift Register



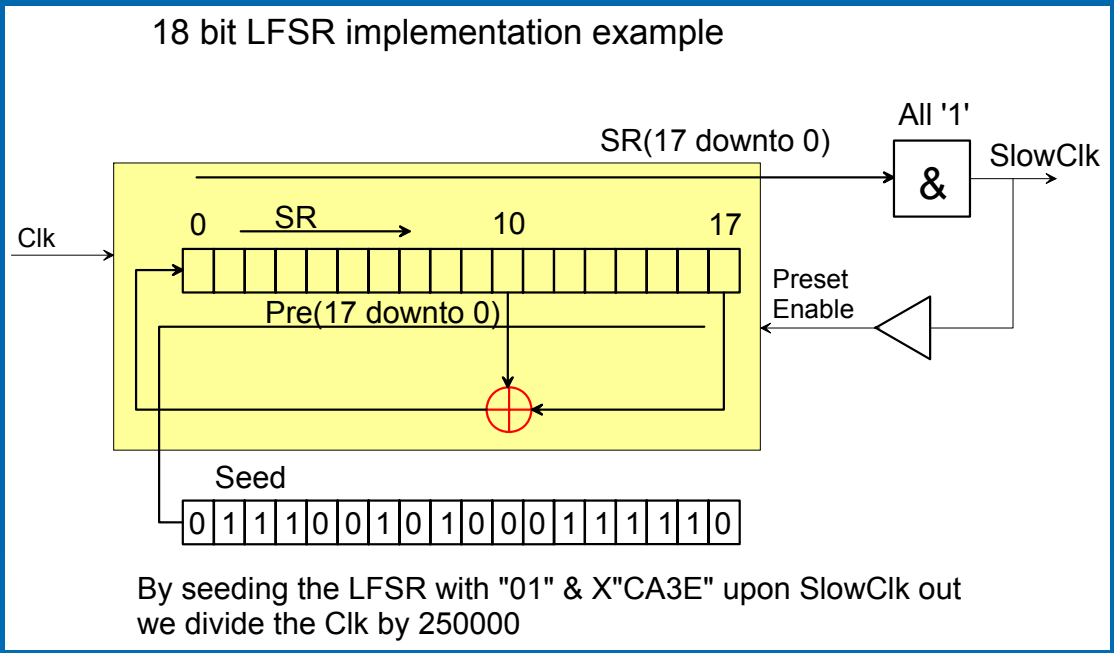
characteristic polynomial: $f(x) = X^{10} + X^{17}$

primitive non reducible polynomial yields

maximum sequence length => $2^n - 1$ => $2^{18} - 1 = 262143$

lockup state SR = 0 needs detection and recovery.

LFSR Counter 2/2




```
entity LFSR18 is
port (reset   : in std_logic ;
      MHz50   : in std_logic ;
      TimeOut : out std_logic );
end;

architecture  V1 of LFSR18 is

constant SR_ini : Std_logic_vector:=X"FFFF" & "10";
constant AllOne : Std_logic_vector:=X"FFFF" & "11";
constant AllZero: Std_logic_vector:=X"0000" & "00";
constant Del5ms : Std_logic_vector:="01" & X"CA3E";

signal SR: Std_logic_vector(17 downto 0);

begin

  process(MHz50,reset)
    begin
      if (reset = '1')
        then
          SR <= Del5ms;
          TimeOut <= '0';
      elsif (MHz50'event and MHz50 = '1')
        then
          for i in 16 downto 0
            loop
              SR(i+1) <= SR(i);
            end loop;
          SR(0) <= SR(17) xor SR(10);
          if SR = AllOne
            then
              TimeOut <= '1';
              SR <= Del5ms;
            else TimeOut <= '0';
          end if;
          if SR = AllZero   --just in case
            then SR <= SR_ini;
          end if;
      end if;
    end process;

end;
```

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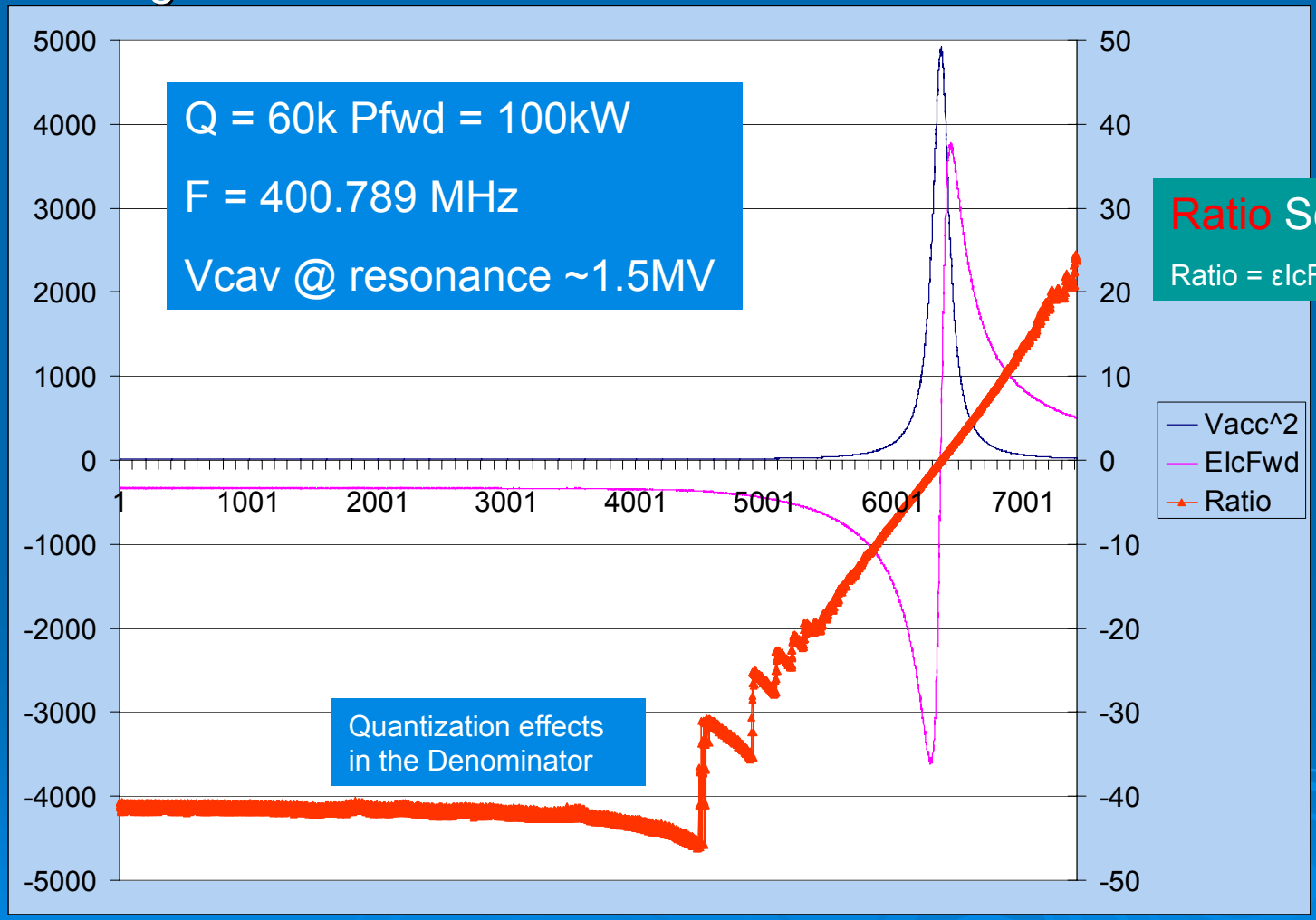
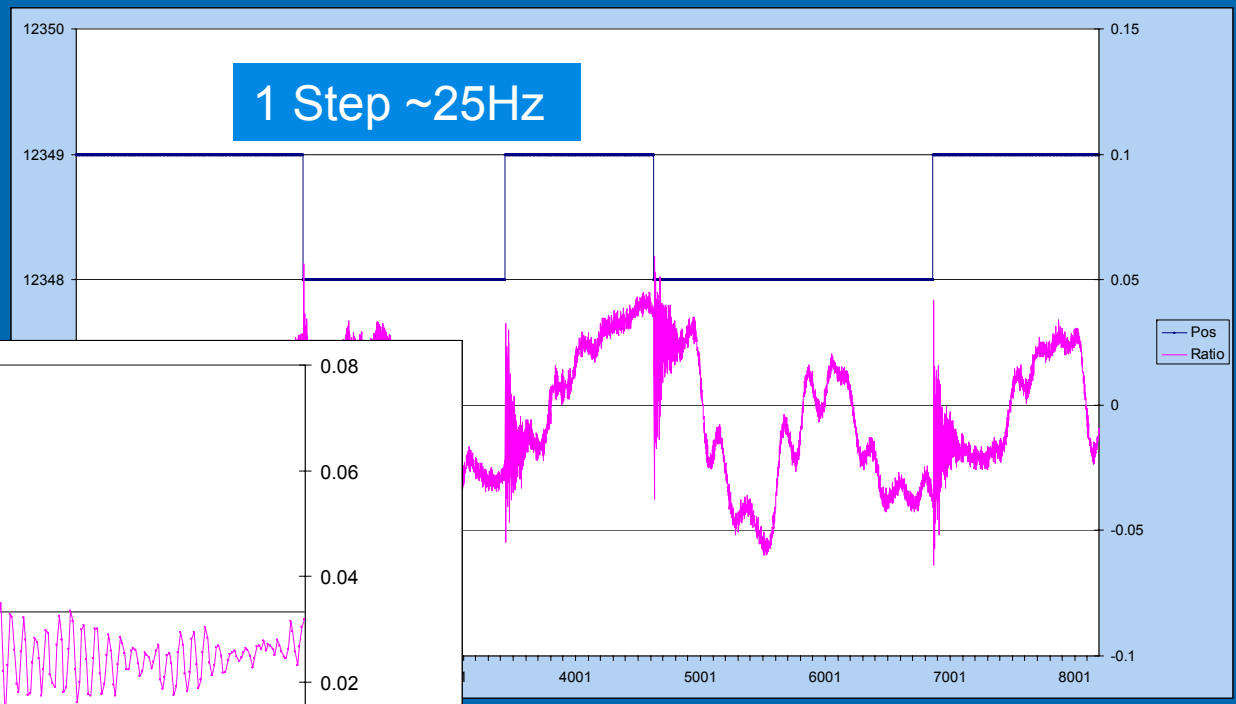
Tuner Calibration Sweep

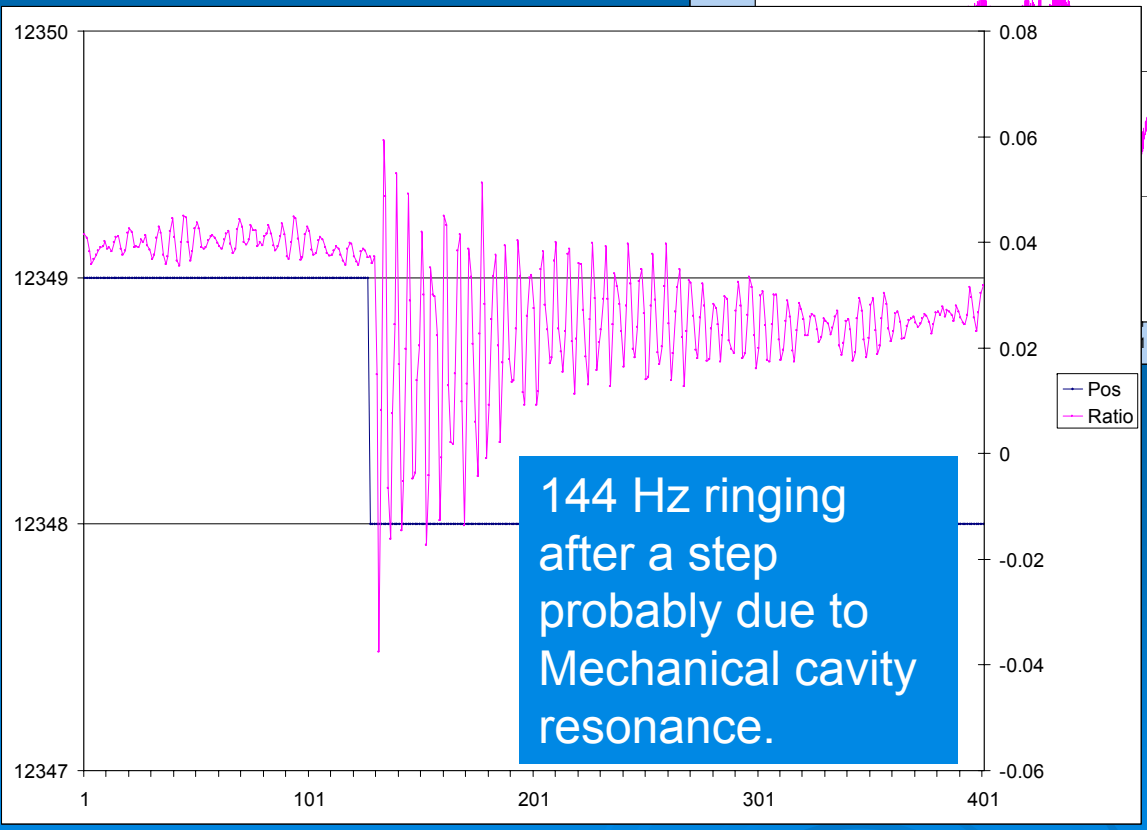
- Output buffer $|Vacc|^2$ & εIcFwd acquired with Tsample = 1.635 ms, buffer length = 13.4s



Tuner Stepping, Noise Observation

- Output buffer |Vacc²| & εIcFwd. Tsample = 1.635 ms, buffer length = 13.4s





Steady Tuned Condition, only 4 tuning steps (back and forth) over 13.4s. Slow Ratio drift phenomena probably due to He fluctuations.

References

- Digital I/Q demodulator
  - [1] Ziomek, C. and Corredoura, P: “Digital I/Q Demodulator” PAC’95
- CIC and Halfband filter design
  - [2] D.J. Goodman, M.J. Carey: “Nine Digital Filters for Decimation abd Interpolation,” IEEE transactions on acoustics, and signal processing, vol. ASSP-25, No. 2, April 1977
  - [3] Uwe Meyer-Baese: “Digital Signal Processing with Field Programmable Gate Arrays”.
- Principles of LHC Tuner Loop
  - [4] P. Baudrenghien: “Principles of the LHC Tuner Loop” (in work)
- LFSR
  - [5] http://direct.xilinx.com/bvdocs/appnotes/xapp052.pdf
  - [6] http://en.wikipedia.org/wiki/LFSR
- LHC Tuner Loop Module Hardware
  - https://edms.cern.ch -> Global Database -> Search
    - [7] LHC Tuner RF Front-end EDA-00331
    - [8] LHC Tuner Control card EDA-00572

Software

- Visual Elite (Summit)
- Synplify (Synplicity)
- ISE (Xilinx)
- Quartus (Altera)
- Concept, PartDeveloper, Allegro, Spectra Quest, NC-sim (Cadence)