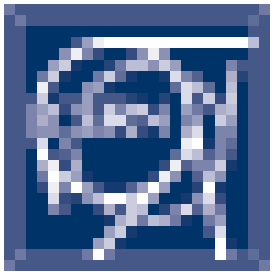

Contribution ID: **4** Type: **invited**

Complex digital circuit design for LHC Low Level RF

Wednesday, 12 October 2005 12:10 (20 minutes)

Modern Low-Level RF systems rely heavily on digital signal treatment. This evolution
has been mainly enabled by the recent availability of powerful FPGAs. Current FPGAs can implement almost all of the signal-treatment requirements e.g. post-mortem and observation memory management, base-band network analyzer functionality, the remote interface to the control systems front-end computer and implement an optional DSP interface bus. The FPGA hardware design language descriptions required for these tasks can easily be entered or imported in the Visual-Elite mixed graphical textual design environment used for the LHC Low Level RF. Standard features are the support of standard VHDL text modules as well as block-diagrams, graphical state-machines, truth-tables and flow-chart hardware descriptions, however the main interest lies in
the inherent code reusability between different projects and it's independence of target device architecture.
This presentation will give a short overview of the design flow, the tools employed and some examples of implementations like: Serial programmable delay controller, IQ demodulator, base-band network analyzer, CIC and half-band decimation / interpolation filters, cross product and power product calculators and a CORDIC based calculator.

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Session Classification: Talks Session 3