# Internal Interface

# Basics

Item Types

- II_WORD
- II_BITS
- II_AREA

Grouping Items

- II_PAGE
- II_VECT

# Permissions

Write permissions:

- WACCESS
- WNOACCESS

Read permissions:

- RINTERNAL
- REXTERNAL
- RNOACCESS

# Features

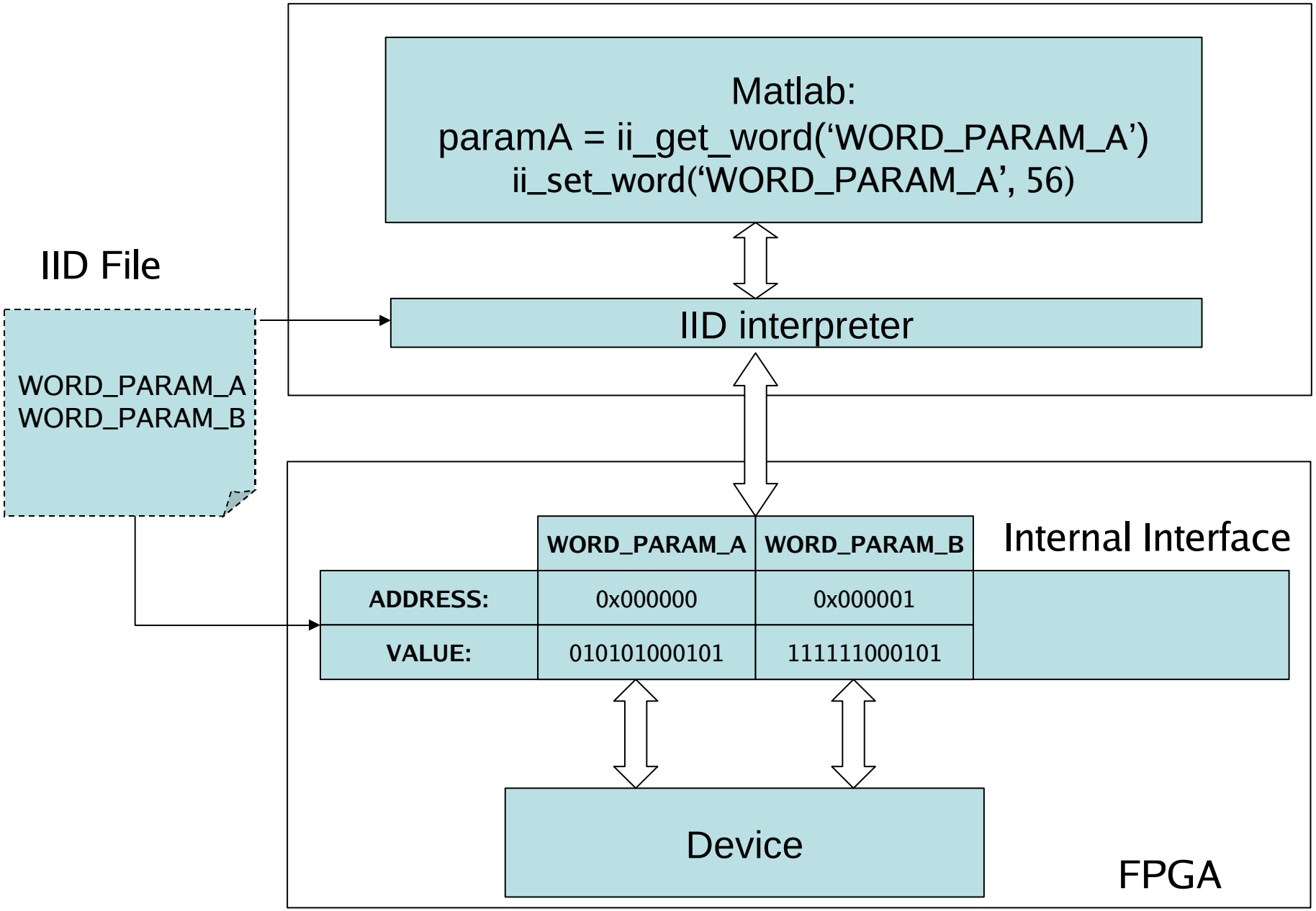
- access to registers is done using alphanumeric constants

- automatic address calculation
- variable address and data bus width

- it is possible to declare registers longer than bus width

- it is possible to declare arrays of register

# Internal Interface Concept



# Address space description

-one description file for VHDL and PC software

```
IIDEC_ITEM_BEG( VII_PAGE,PAGE_REGISTERS,0,0,PAGE_REGISTERS,VII_WNOACCESS,
     VII_RNOACCESS,VIINameConv(" "),VII_FUN_UNDEF,VIIDescrConv(" "))

IIDEC_ITEM_CON( VII_WORD,WORD_BOARD,32,1,PAGE_REGISTERS,VII_WNOACCESS,
     VII_REXTERNAL,VIINameConv(" "),VII_FUN_UNDEF,VIIDescrConv(" "))

IIDEC_ITEM_CON( VII_WORD,WORD_CHIP,32,1,PAGE_REGISTERS,VII_WNOACCESS,
     VII_REXTERNAL,VIINameConv(" "),VII_FUN_UNDEF,VIIDescrConv(" "))

IIDEC_ITEM_CON( VII_WORD,WORD_VERSION,32,1,PAGE_REGISTERS,VII_WNOACCESS,
     VII_REXTERNAL,VIINameConv(" "),VII_FUN_UNDEF,VIIDescrConv(" "))
```

# Summary

- projects using this communication interface can be easily ported to other FPGA platforms ( different chip, different physical layout )

- transparent addressing