W. Hofle
CERN AB/RF

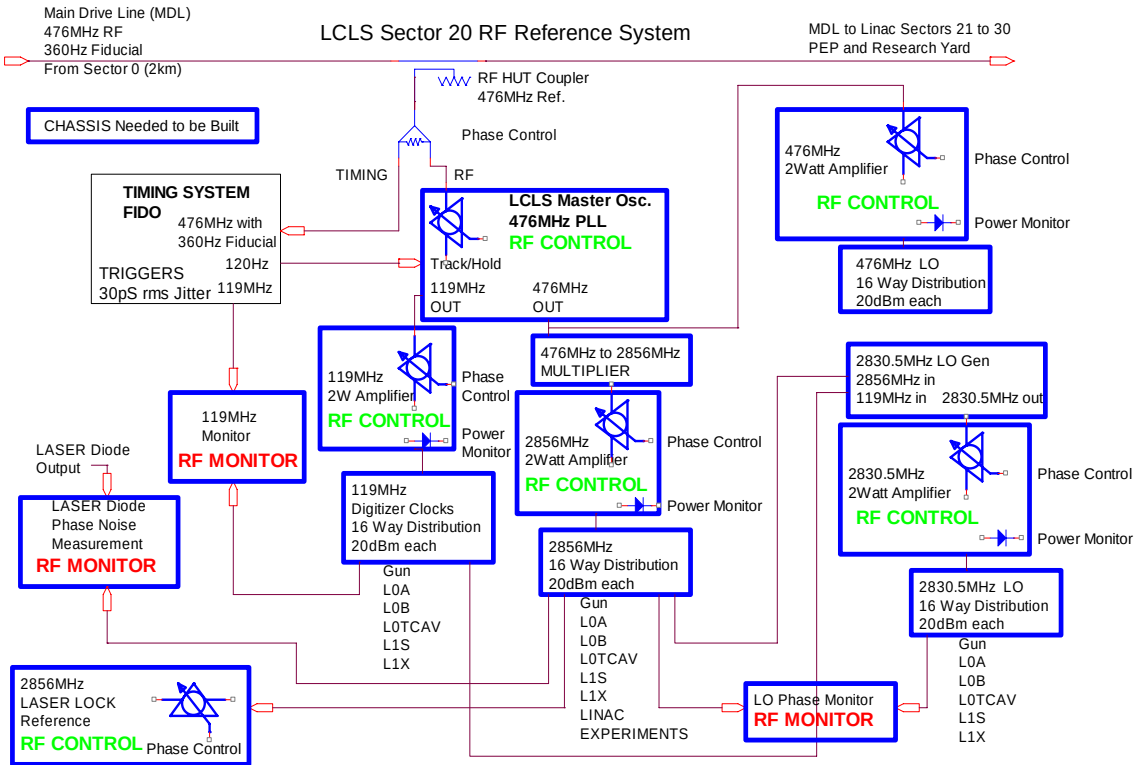
Summary of Poster Session

Wolfgang Hofle
CERN AB/RF

- 17 posters on display covering whole range of RF low-level issues treated in workshop (only seven uploaded on web page)
- Low-level for light sources: issues fS phase stability, distribution of RF reference frequency over large area, many RF stations (VUV-FEL at DESY for example)
- Superconducting cavities control going digital
- Modelling using Matlab/Simulink
- Proton driver RF systems, with RF frequencies of a few MHz use of DSP frequent, often combined with FPGA
- Reliability issues not treated in depth (one Poster on radiation issues and measurements), technology advancing fast, few authors addressed issues such as boards and components (and also software!) becoming obsolete before design goes into production and exploitation. Future will show how to maintain such systems over ~10 years

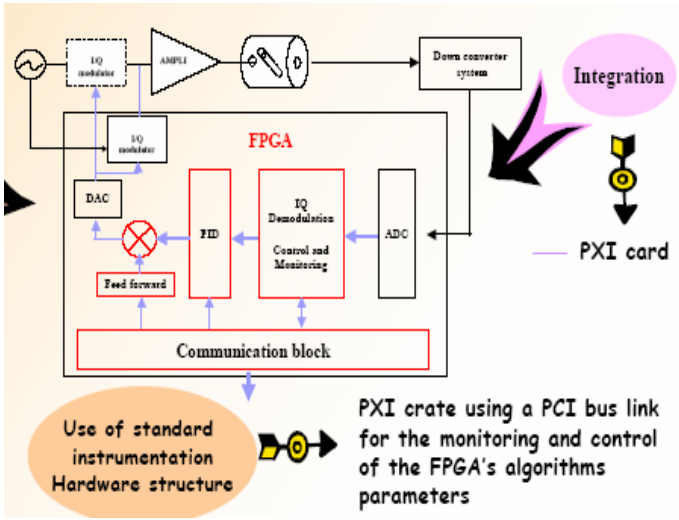
SLAC LCLS RF reference distribution system

- Analogue techniques still have their place, use of coax for distribution
- Similar RF distribution systems required for XFEL VUV at DESY, ILC, use of optical fibers
- Low noise, low jitter very important, down to tens of femto seconds stability



LLRF system for superconducting SPOKE cavities (collaboration CNRS, financed by Eurotrans/Eurosil) for high intensity proton driver accelerator

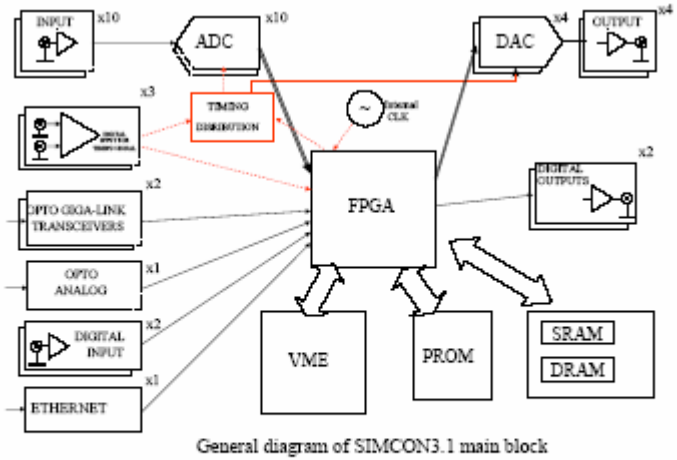
- Analogue down conversion from 352 MHz to IF of 10 MHz
- Digital IQ demodulation of IF signal implemented on an FPGA
- Digital hardware is a custom design, 80 MHz clocked, hardware in standard crate (PXI)
- Simulation of system with Simulink
- First tests will be done on a warm cavity



Simcon 3.1 board (DESY in collaboration with Warsaw University of Technology and Lodz University)

- Development started off initially with a commercial board with Xilinx Virtex II, switched to all-in-one board developed in house
- Simcon 3.1 is a multi-channel, multi-purpose board comprising a total of 10 ADCs and 4 DACs, VME standard
- Very interesting development due to the many planned embedded options (powerPC, they are writing their own floating point core)
- Development aimed for future XFEL VUV at DESY

SIMCON 3.1 board is our last child developed in 9 months. It is well equipped version of SIMCON with 2 PowerPC processors embeded into FPGA chip (Xilinx Virtex Pro30) 2 opto-giga links with throughput of 3.125MBPS, 10 ADCs channels (14bits, 10 5MSPS) & 4 DACs (14bits, 210 MSPS), 10/100MBPS ETHERNET, dynamic and static memory and special clock distribution scheme with clock jitter lower than 1ps. Many universal digital Inputs and outputs were also added for triggering inputs and outputs.



General diagram of SIMCON3.1 main block

One schematic project has been spited into two physical realization of the PCB board (presented Below)

Digital Beam phase control using DSP (FAIR at GSI, FH Fulda)

- Simulations with simulink
- Use of a commercial DSP board for the phase detection
- DDS on FPGA
- Mixed approach DSP/FPGA is flexible due to DSP

simulink model

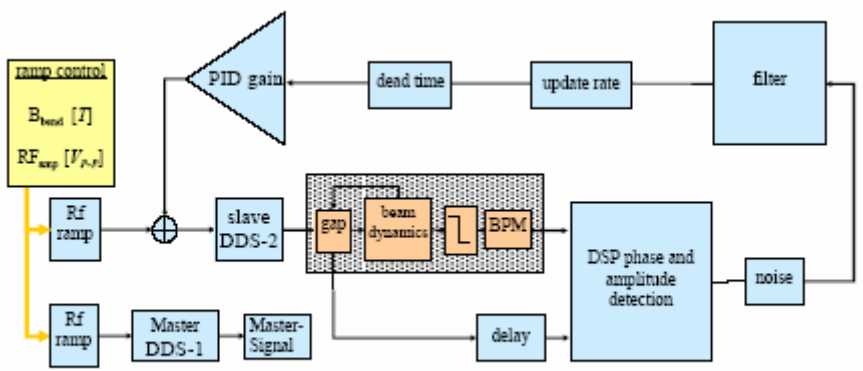


Fig. 1: Control Loop Diagram of Simulation

Conclusions

- Wide spread use of digital techniques well established in LLRF
- Still very different approaches: commercial boards vs in-house, FPGA versus DSP, generic versus built to a specific application
- Future will show whether some of these approaches are superior in terms of reliability, maintainability, and cost in terms of development time "time to market"
- Analogue techniques will still have their place in RF front-ends low group delay feedbacks, reference distribution