

Low Level RF System in KEK-STF

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KEK Accelerator Laboratory

- KEK-STF phase 1
- LLRF system at KEK-STF phase 1
- RF modeling and Simulation
- Cavity simulator
- Future plan (IF Mixture method)

Introduction

- KEK started to construct the super-conducting rf test facility (STF) from FY2004 to contribute for the international linear collider (ILC).

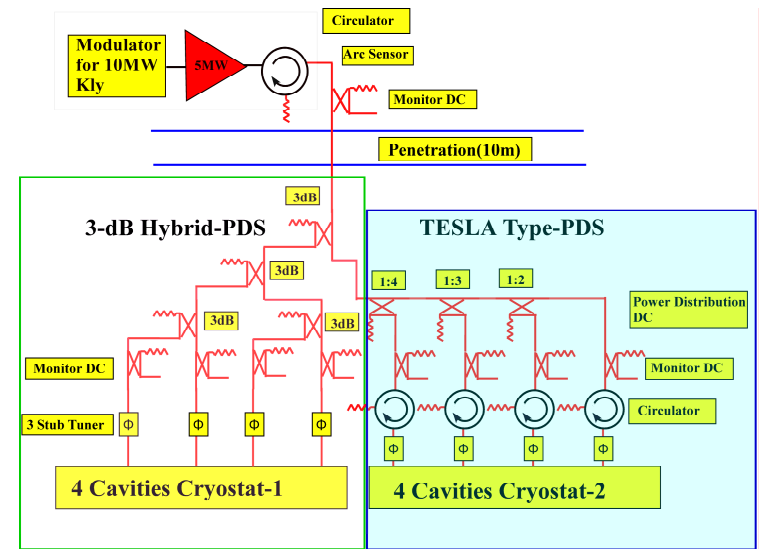
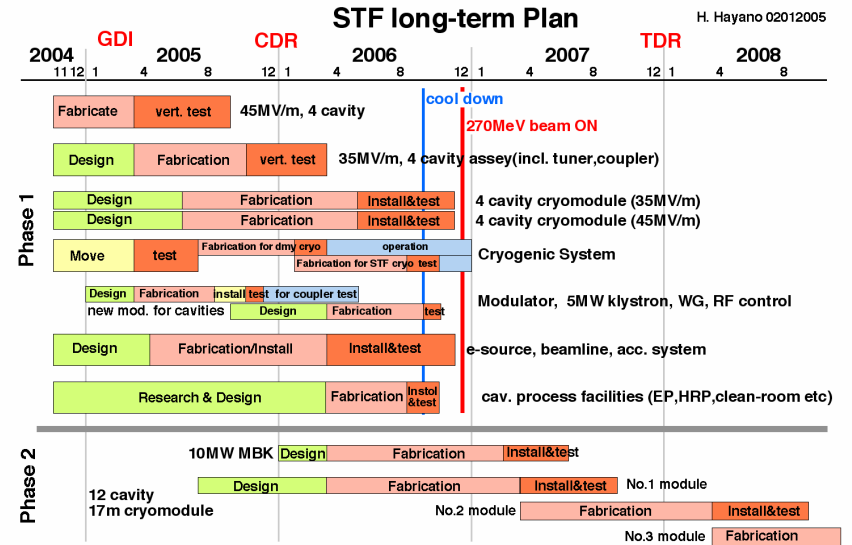
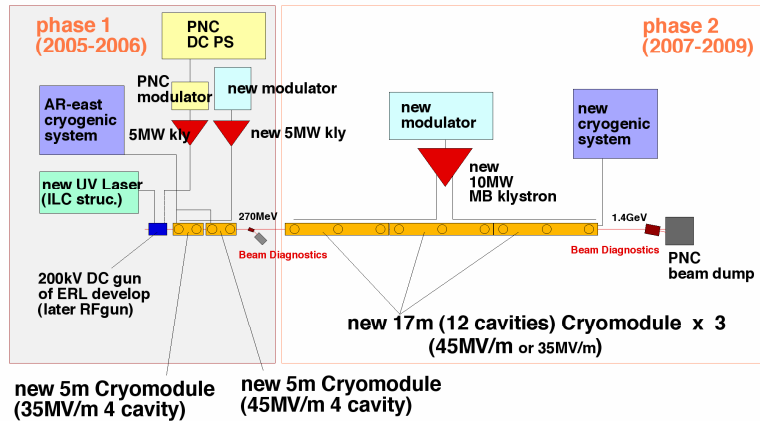
- KEK-STF project**
 Operation frequency : 1.3GHz
 RF pulse width : 1.5ms
 Repetition rate : 5Hz

- STF Phase 1 (FY2005-FY06)**
 4 TESLA-type cavities and 4 LL-type cavities in **one cryomodule**
Goal: high accelerating field gradient
 35MV/m : TESLA-type cavity
 45MV/m : LL-type cavity



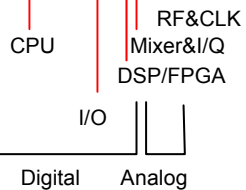
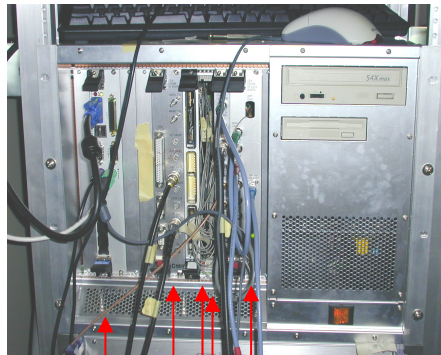
- STF Phase 2(FY2007-FY08)**
 To build one RF unit for ILC main linac

Plan of Superconducting RF Test Facility (STF)



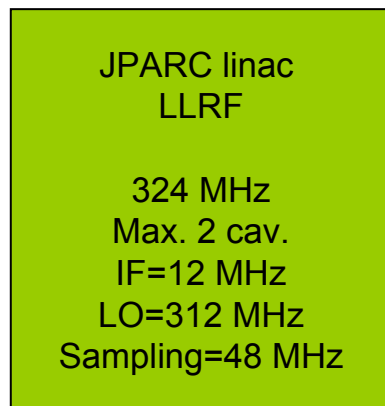
Power distribution system for STF Phase 1

Schedule for LLRF in the KEK-STF

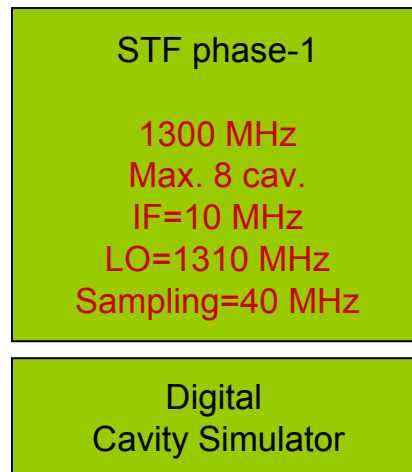


JPARC LLRF SYSTEM

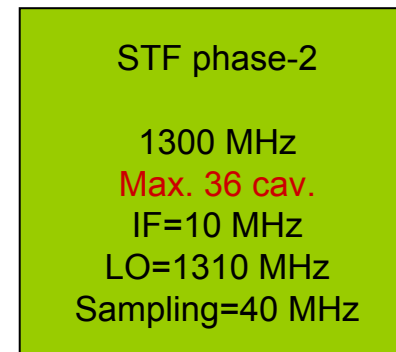
- The LLRF system for STF is based on the JPARC LLRF system for quick preparation.
- Analog rf delivery system (~2005)
Digital LLRF system based on JPARC LLRF (8 cavities)
⇒FY2005: Digital system (FPGA and DSP board) and Analog system (Mixer and RF&CLK) design and manufacture
⇒FY2006: Software development
- Digital LLRF system for Phase- II (max. 36 cavities)
⇒FY2006: additional FPGA board manufacture
⇒FY2007: software development, Tuner control



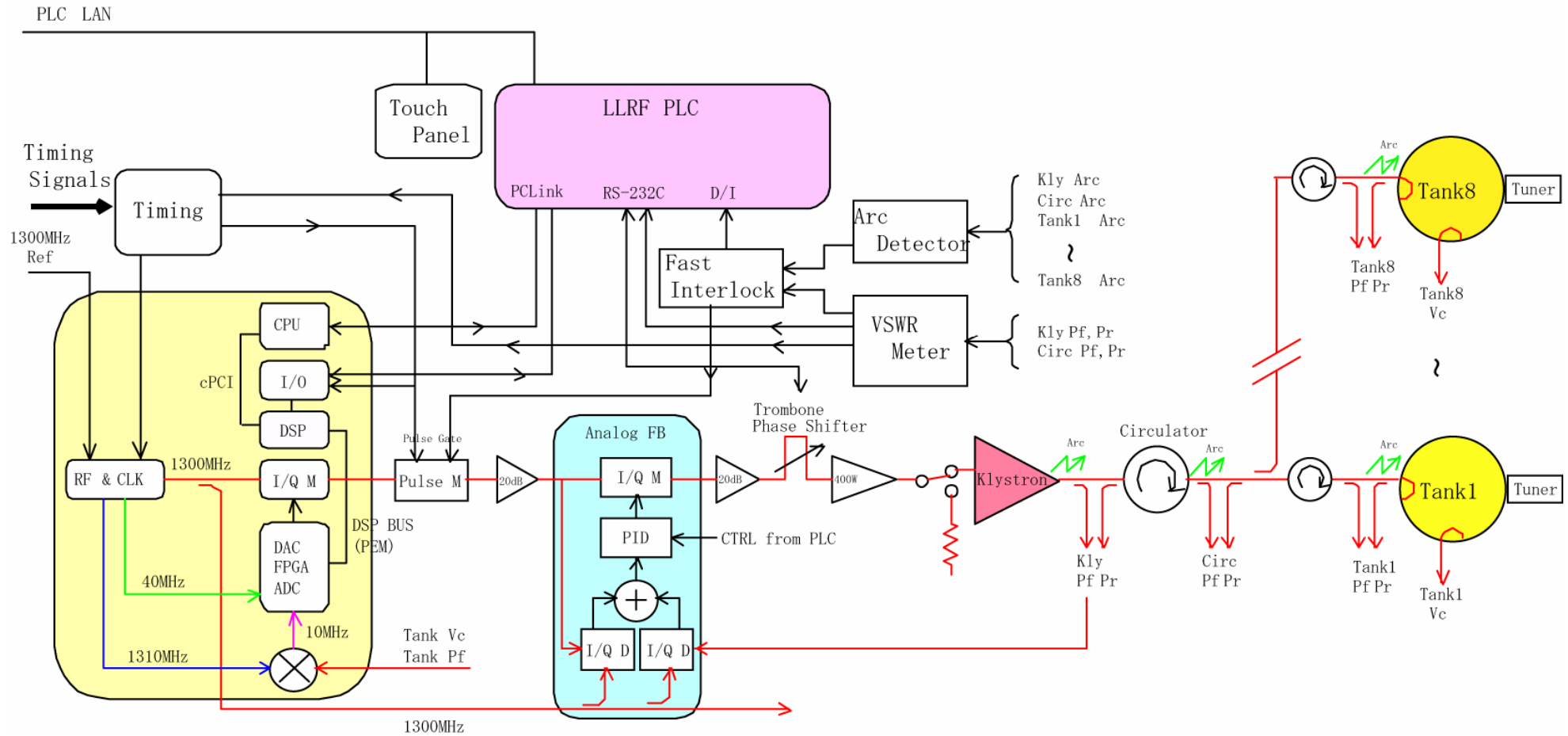
Achievement:
<+-0.15% in amplitude
<+-0.15deg. in phase



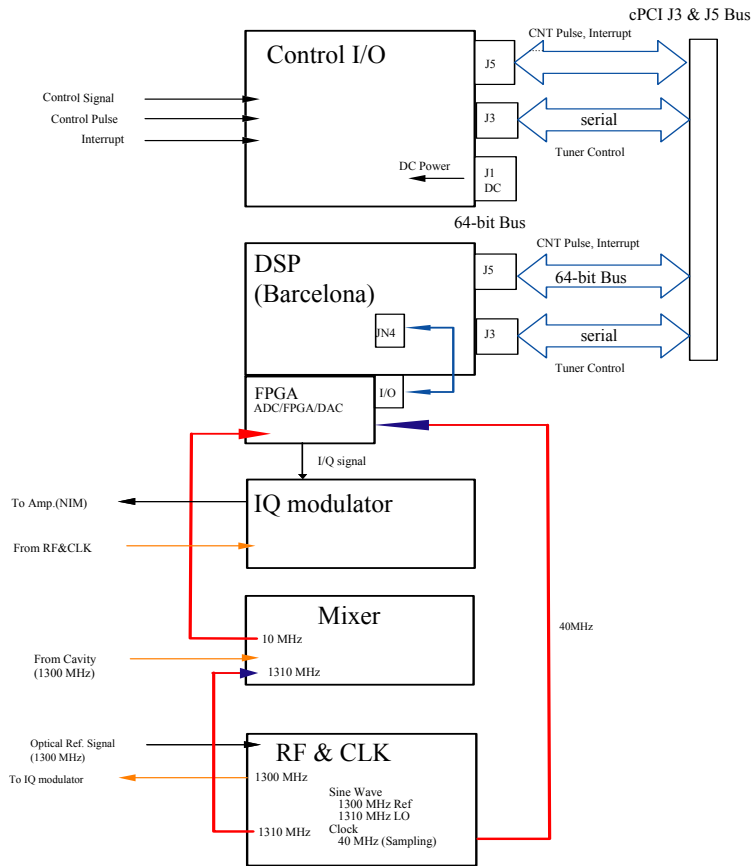
Requirement:
<+-0.1% in amplitude
<+-0.1deg. in phase



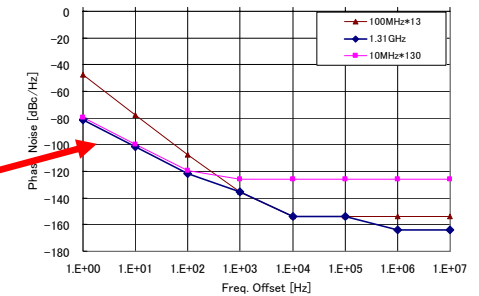
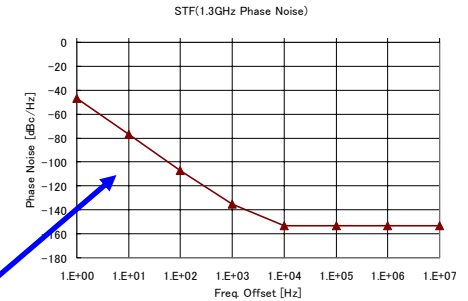
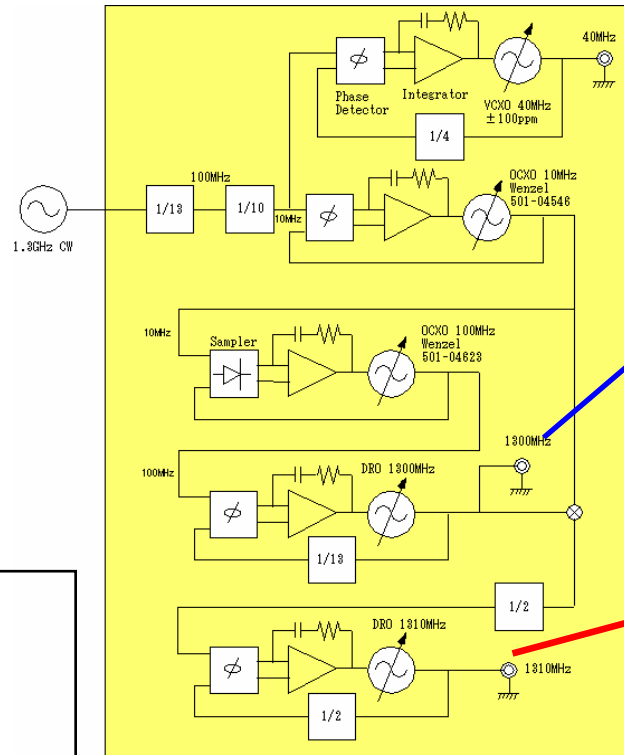
Overview of the LLRF System



- The RF system for STF is based on the LLRF system developed for JPARC. The components for controlling the LLRF system are the PLC, Touch Panel, cPCI System, and Fast Interlock.



• **RF & CLK Unit**
 Input : 1300MHz
 Output: 1300MHz
 1310MHz (LO signal at the Mixer Unit)
 40MHz (Sampling/Clock signal of FPGA, ADC, DAC at FPGA board)

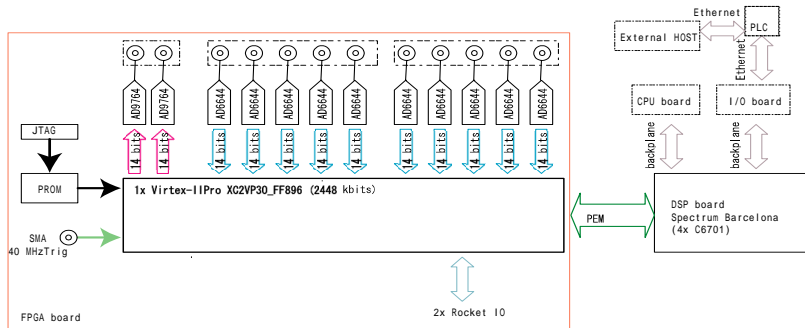


• **Digital Control System in the cPCI crate**
 DSP Board (Barcelona, 4xTMS320C6701)
 FPGA Board (10x14bit ADCs, 2x14bit DACs)
 Control I/O (communication between PLC and cPCI)
 CPU (Windows2000 based)

• **Analog System**
 RF&CLK (generate RF and clock signals)
 Mixer Unit (down-convert cavity signals)
 I/Q Modulator (I/Q modulation)

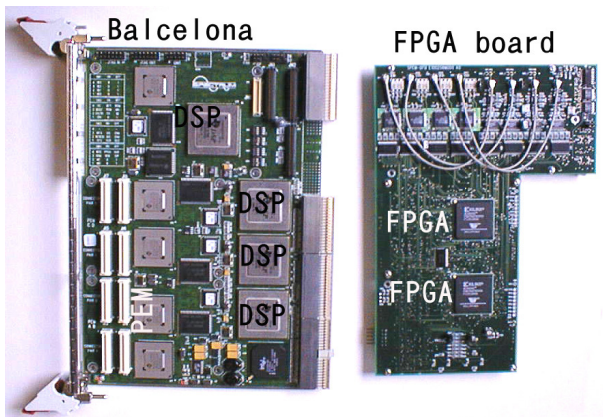
Water-cooling system will be adopted to stabilize the outputs of analog system (RF&CLK, Mixer, I/Q modulator).

The phase noise of RF&CLK unit is calculated by the noise in the base frequency oscillator. The effect of mixer and PLL to phase noise is not included.

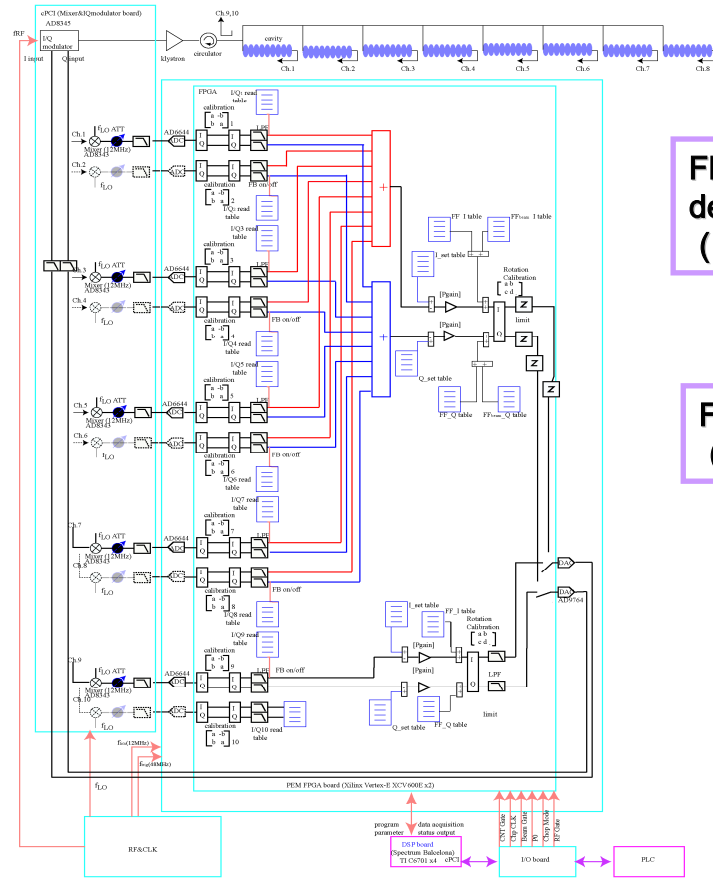


DSP Board
 Barcelona DSP board (Spectrum Signal Processing Inc., 4 x TMS320C6701). Each of the DSPs has I/O port called "PEM" on the board which provides a high-speed dataflow (400 MB/s) from/to a mezzanine (FPGA) board inserted into the PEM connectors. DSP board can stop rf during the pulse with intelligence.

- FPGA Board**
 FPGA chip : Xilinx Virtex-II Pro30
 14-bit ADC(AD6644) : 10ch
 14-bit DAC(AD9764) : 2ch



DSP and FPGA Board for JPARC LLRF System



FB program development (2006.1 ~ 8)

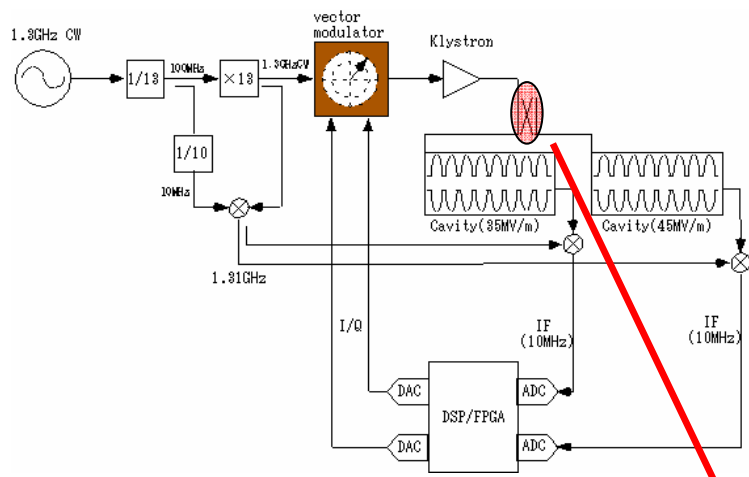
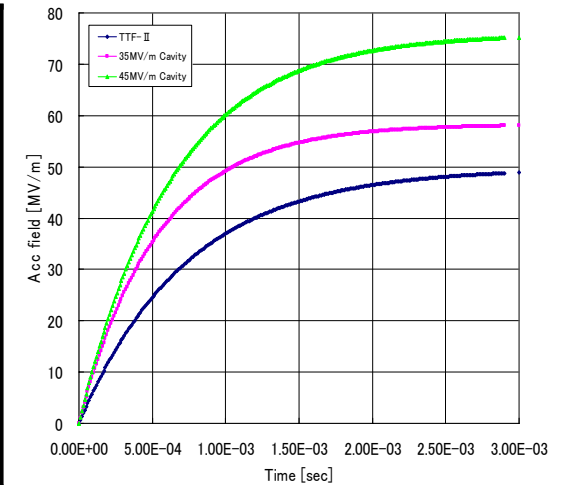
FB operation (2006 autumn)

Feedback (P control) + Feedforward

RF modeling and Simulation

At KEK-STF, two different types of cavities are operated with one klystron. The model of LLRF in STF was made by use of Simulink library for RF system developed for TTF. The performance of RF control system is estimated.

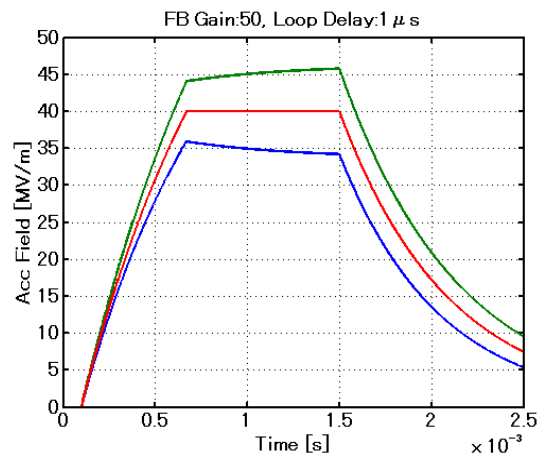
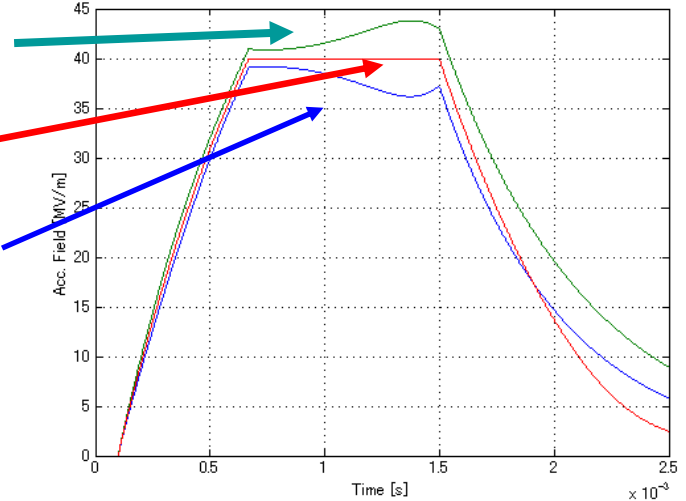
	TTF-II	35MV/m Cavity	45MV/m Cavity
Beam Current [mA]	8.0	10.4	10.4
r/Q [Ω]	1030	1016	1144
QL	3.00e6	2.20e6	2.60e6
Filling Time [μs]	735	539	637
Input Power [kW]	200	380	485



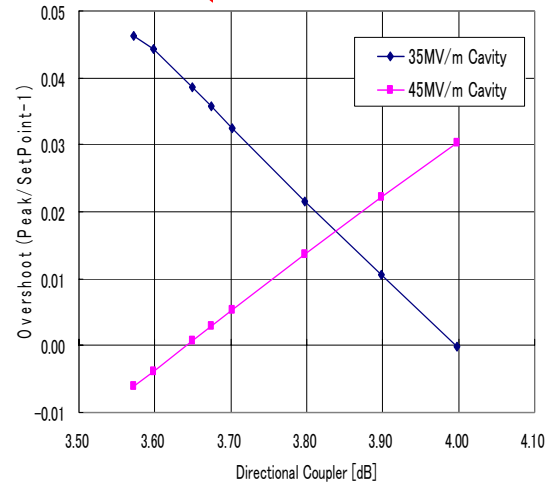
45MV/m Cavity

Average

35MV/m Cavity



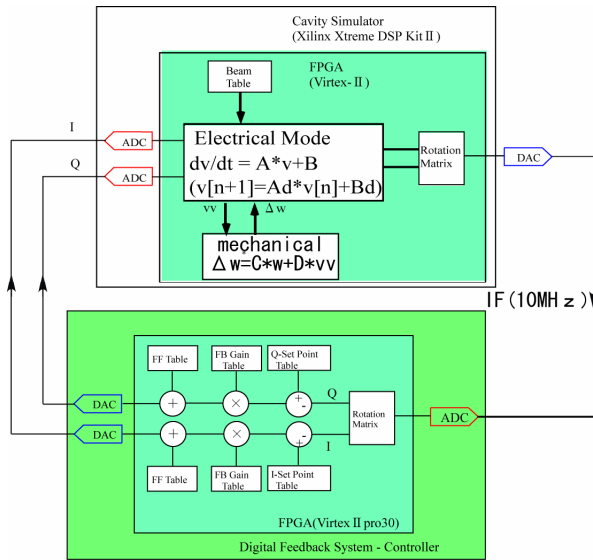
No Lorentz force detuning



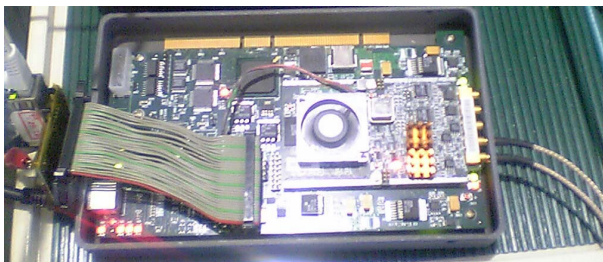
Including Lorentz force detuning (TTF- II parameter) with pre-detuning of 1250 Hz (45 MV/m cavity) and 1100 Hz (35 MV/m cavity). ⇒ Piezo tuner controller

Future improvement:
To include the parameters of mechanical mode for each cavities and (Piezo) tuner controller.

Cavity Simulator

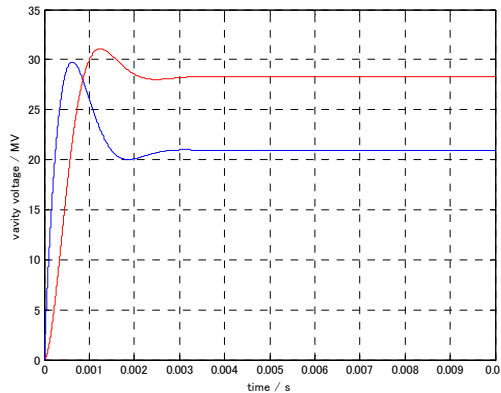
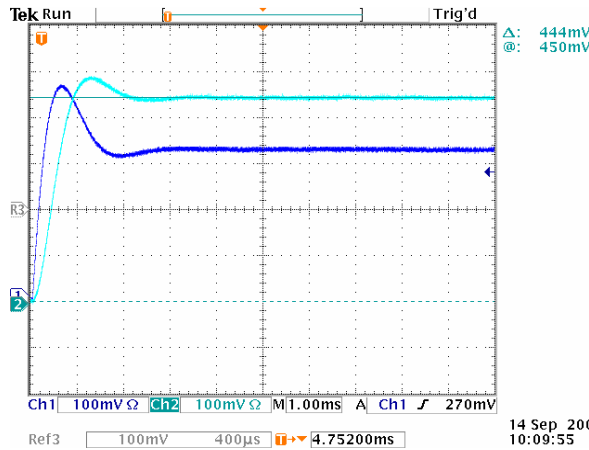


The performance test of LLRF system using cavity simulator

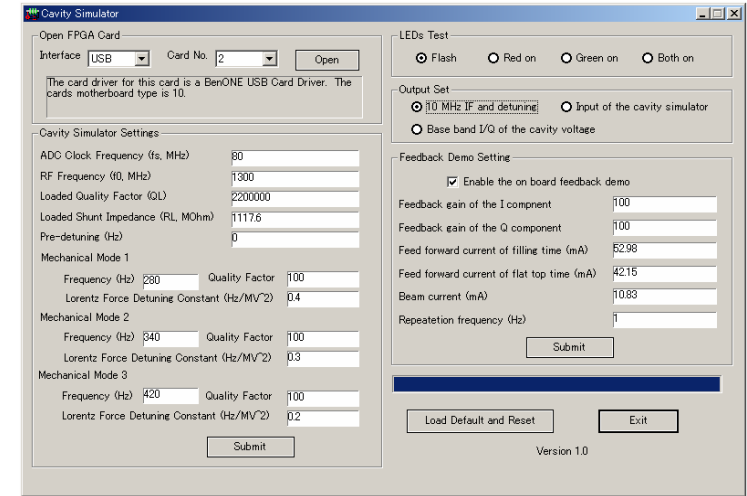


Cavity Simulator:
by commercial FPGA board

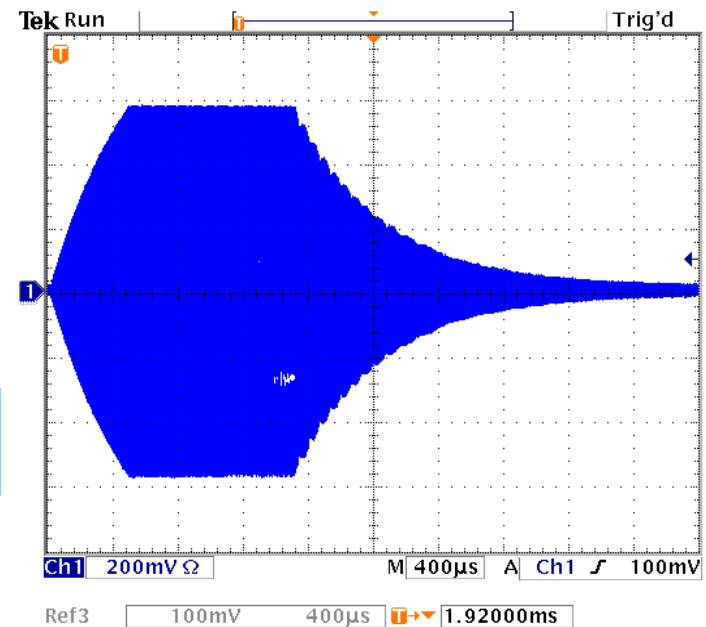
The VHDL code of cavity simulator and GUI program are build by Mr. Geng (IHEP).



Step response of cavity with pre-detuning of 400 Hz



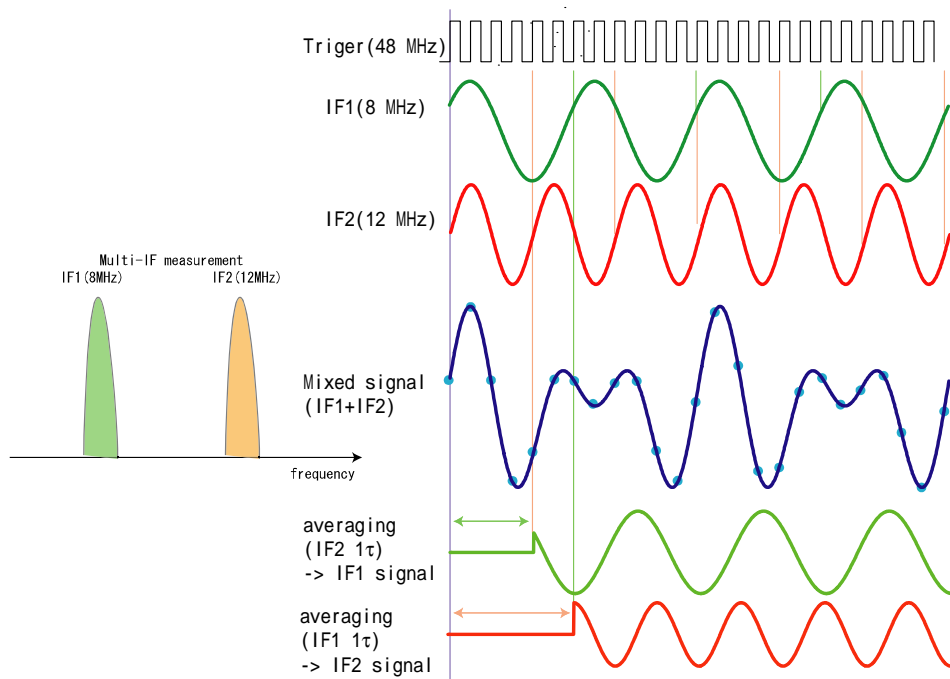
GUI on host PC to cavity simulator



Modulated IF signal (10MHz)
of the cavity simulator

Future work (IF-mixture)

Now, the number of ADCs in a FPGA board is limited due to the substrate. (maybe ~15 with 16 layers in substrate)
 The idea is based on the 'digital radio' and obtaining cavity signals with a ADC.



Mixture of two signals decrease the resolution of analog signals but averaging increases the resolution.

Cavity signals do not change during averaging (due to high Q values)
 → Enough IF separation

