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FPGA Phase Detector Implementation

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An optimized digital phase detector for a 106 MHz superconducting cavity was designed using state machine logic. Transitions of the feedback and reference inputs trigger corresponding changes in the state of the detector. The state machine has been implemented using a high speed Xilinx field programmable gate array. The resulting design incorporates two phase detectors (one for the phase loop and one for the tuning loop), two frequency counters, and a subtractor. The counters and subtractor are used to determine the frequency error for initial tuning of the cavity. The design and some initial test results are presented.

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