DEPFET Prototype System for the ILC Vertex detector: First test beam results

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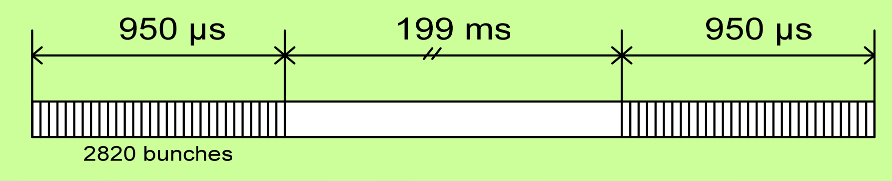
Overview

- Reminder
  - ILC requirements
  - DEPFET principle of operation
  - DEPFET ILC prototype system
- Material Budget ➔ Power dissipation
- First Test Beam Results

ILC requirements

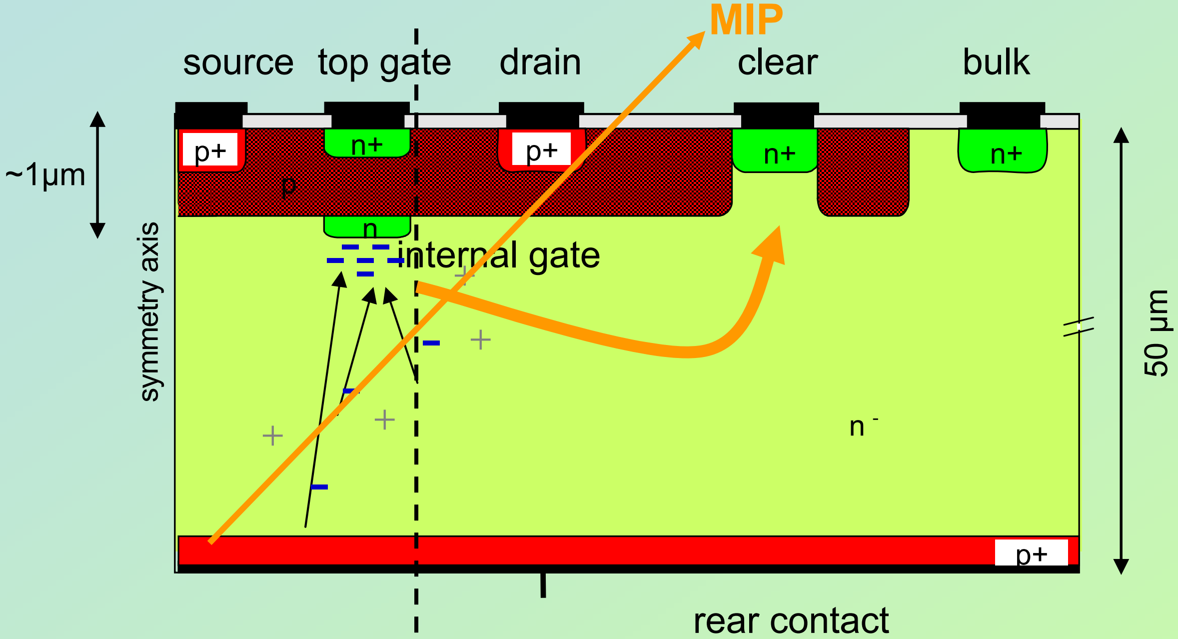
- Time structure: one train of **2820 crossings** in **~1 ms** every **~200ms**
  - ➔ Hit density: for **r = 15 mm**: **~ 100 tracks / mm^2 / train**
  - ➔ Row readout rate: **> 20 MHz**
  - ➔ **Occupancy < 0.5 %**



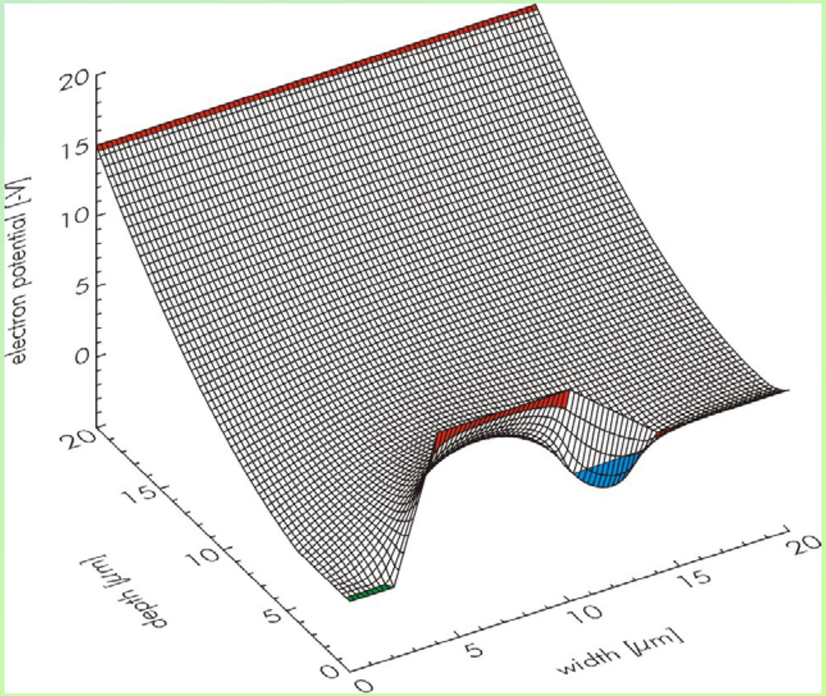
- Radiation length: **~0.1% X_0** per layer ⟶ **Talk by G. Lutz**
  - ➔ thinned sensors (50 µm)
  - ➔ **low power consumption**
- Radiation tolerance: **≥ 200 krad** (for 5 years operation) ⟶ **Poster by L. Andricek**
- Resolution: **few µm** (⇒ pixel size ≤ 25 x 25 µm^2)

DEPFET principle of operation

- A **p-FET** transistor is integrated in every pixel
- Electrons are collected at an „internal gate“ and **modulate the transistor current**
- Signal charge is removed via a clear contact



Potential distribution:

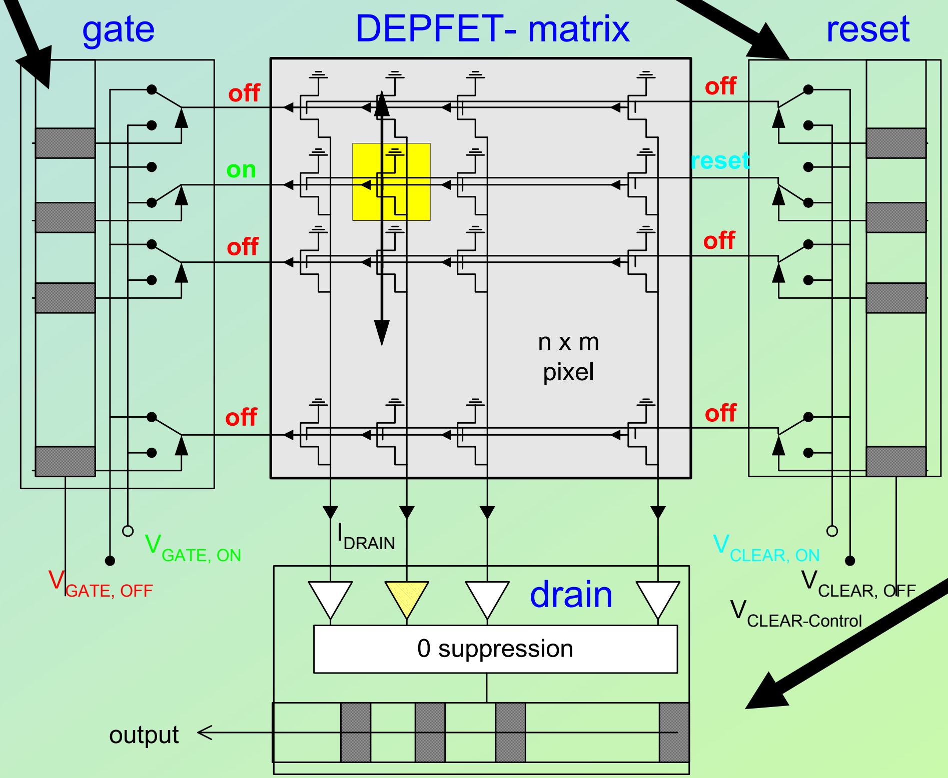


- **Fast** signal collection in **fully depleted** bulk
- **Low noise** due to small capacitance and first amplification in pixel
- Transistor can be **switched off** by external gate – charge collection is then still active !

DEPFET matrix operation

Switcher:
- 64 x 2 outputs
- Max ΔV = 25V
- Clear and Select

pixel matrix with row wise read out



CURO:
- current based read out
- 128 channels
- pedestal subtraction
- real time hit finding
  & zero-suppression
- Noise per sampling:
  30 nA @ 24 MHz
- row rate up to 24 MHz

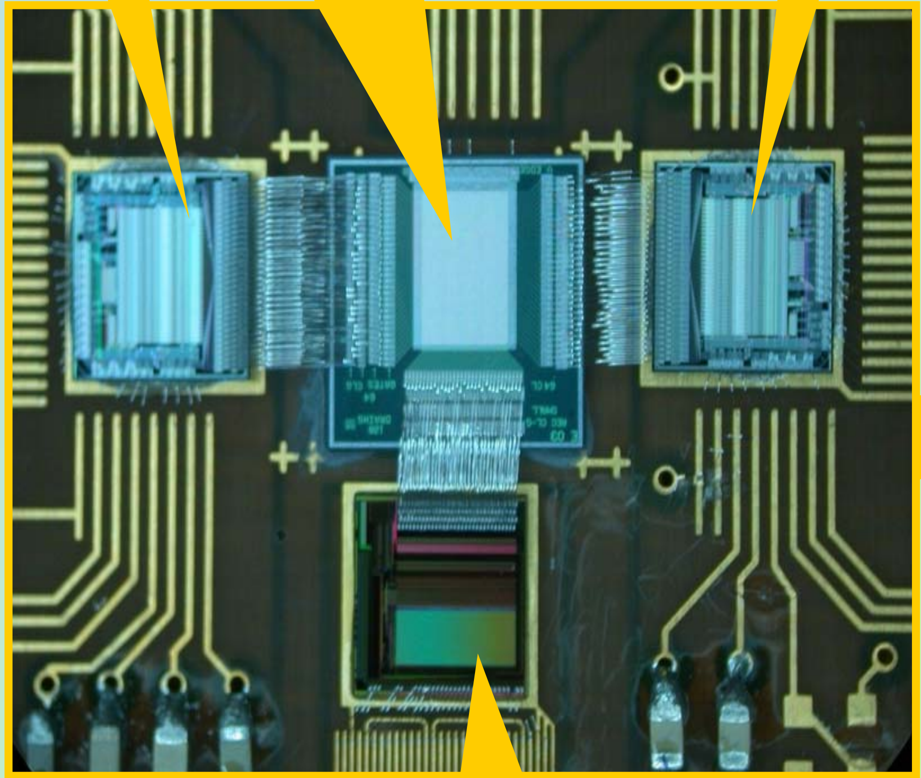
Matrix: MPI, Munich
Switcher: Mannheim Univ., Bonn University
CURO: Bonn University

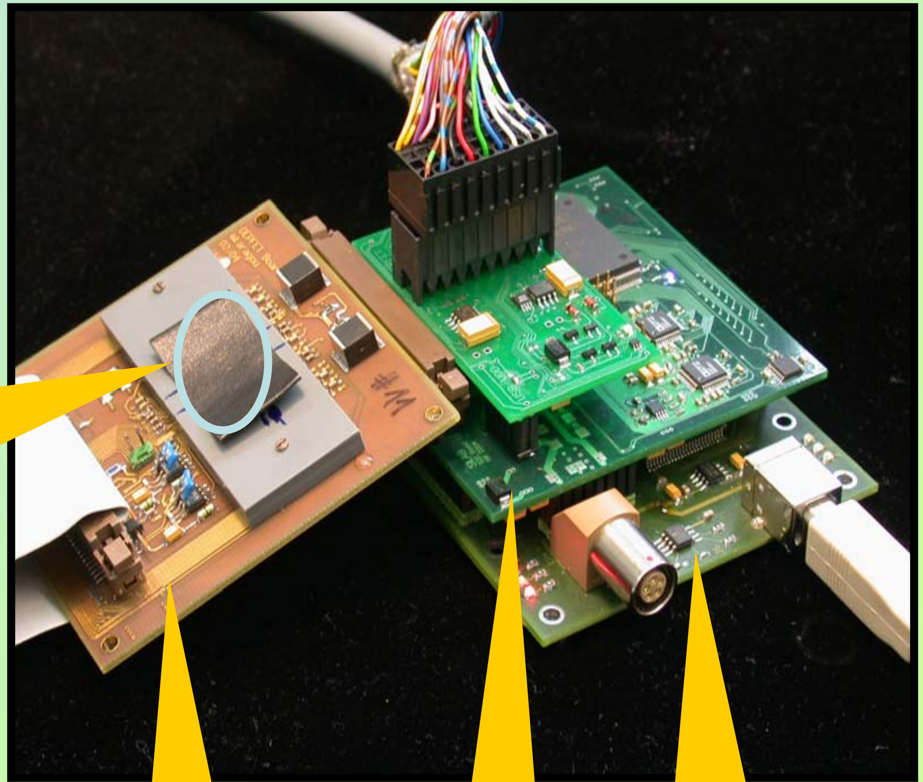
DEPFET prototype system

Gate Switcher

DEPFET Matrix
64x128 pixels, 36 x 28.5μm^2

Clear Switcher





Current Readout CUROII

PCB with DEPFET matrix

Analog board with ADCs etc.

USB based digital interface board

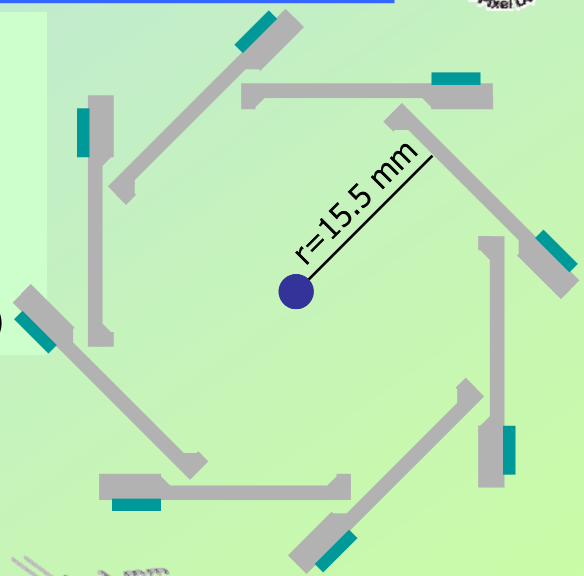
Expected Power Dissipation

Measured Power Dissipation:

- ➔ Switcher: 6.3 mW per active channel at 50MHz
- ➔ CURO: 2.8 mW / channel

Assumed Power Dissipation of DEPFET Sensor:

- ➔ P_{DEPFET}: 0.5 mW per *active* pixel (V_{Drain}= 5 V, I_{Drain}= 100 μA)



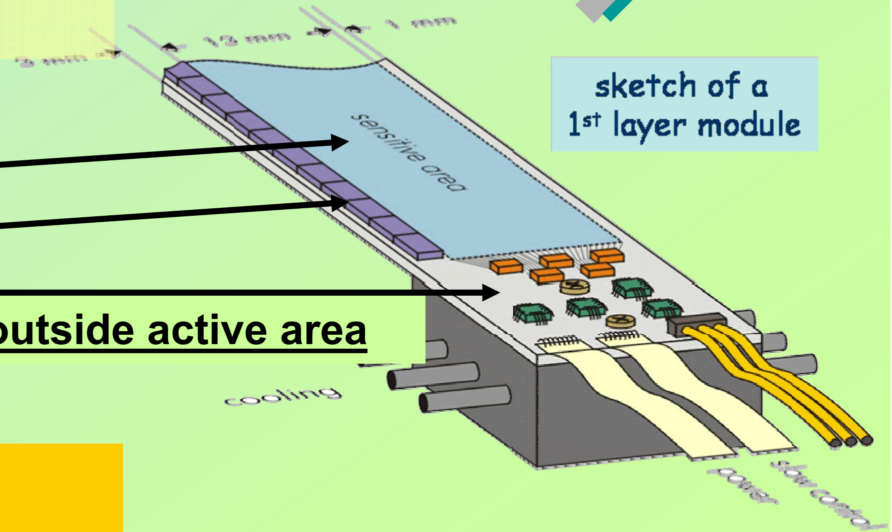
duty cycle:
1/200

Only active pixel dissipate power
1024 active pixels per module
8 modules **in Layer 1**
➔ **8192 active pixels**

Expected Power Dissipation in Layer 1:

- ➔ Sensor: 8192 x 0.5 mW / 200 = 20 mW
- ➔ Switcher: 16 x 6.3 mW / 200 = 0.5 mW
- ➔ Curo: 8192 x 2.8 mW / 200 = 114 mW

➔**for Layer 1** **Sum: 135 mW**

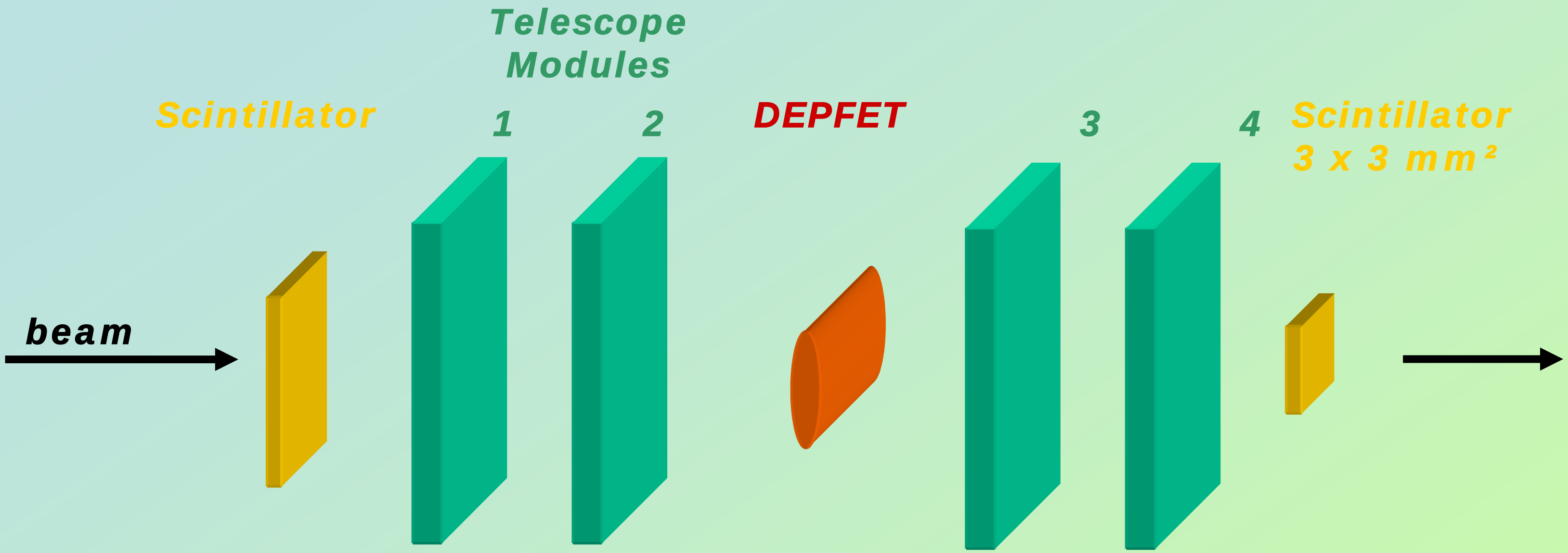


sketch of a 1st layer module

outside active area

For 5 Layer DEPFET Vertex Detector:
Total ~ 3.6 W ➔ no active cooling

Test beam Setup



Measurements at DESY test beam in Aug. 2005 with 6 GeV e- beam

Bonn ATLAS telescope system:

- double sided strip detectors
- pitch 50 µm (no intermediate strips)
- readout rate 4.5 kHz (telescope only)

Alignment & Multiple Scattering

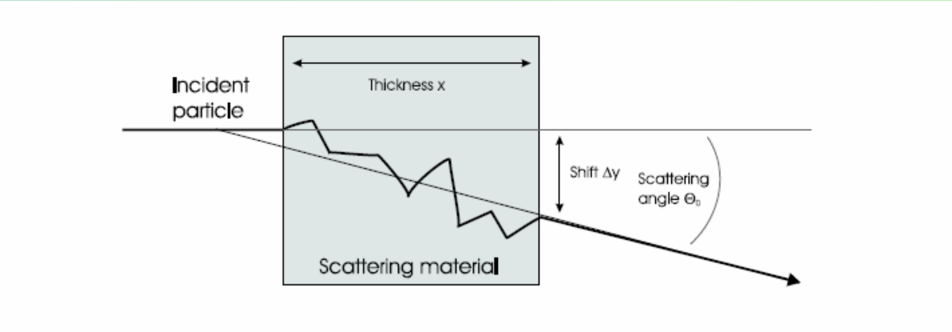
Aligning the telescope modules in the beam:

» Select events with tracks through all modules

» Make a linear fit through the track points of the telescope planes

» Aligning (incl. rotation) is done iteratively by minimizing the residuals between predicted and real hit position.

Multiple scattering makes *precise* track fitting difficult



$\sigma_\theta \sim 1 / \beta \cdot p$

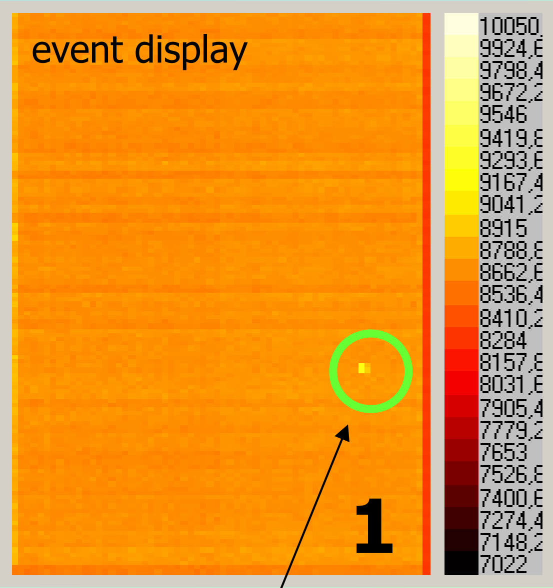
minimize scattering ➔ select straight tracks by applying a χ^2 cut on the track fit

Measured residuals of the telescope planes: $\sigma \approx 11\ \mu m$ *(DUT and resp. plane not included in fit)*

Data Processing & Clustering

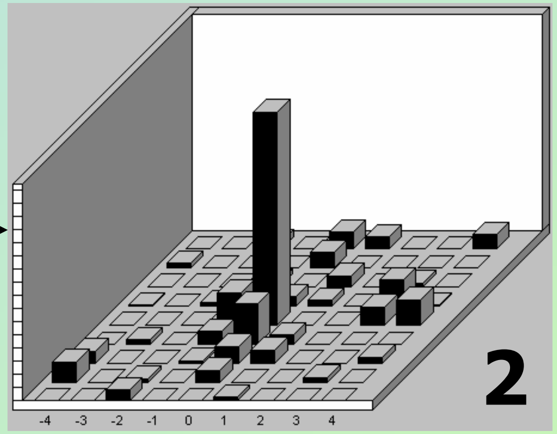
64 columns

128 Rows

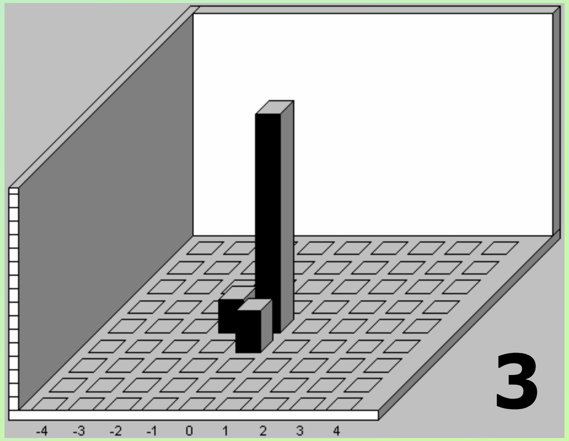


Hit in raw data!

a) Apply Seed Cut
b) Sort by Pulse Height
c) Check for double counting



d) Apply neighbor cut, if pixel is inside ROI around seed



Corrections on raw data:
- Pedestal subtraction
- Common Mode subtraction

Position reconstruction
➔ center of gravity method

$$\sigma_{COG} = \frac{\sum_i x_i \cdot PH_i}{\sum_i PH_i}$$

4

Compare with track fit results

Selecting stiff tracks
➔ χ^2 - cut

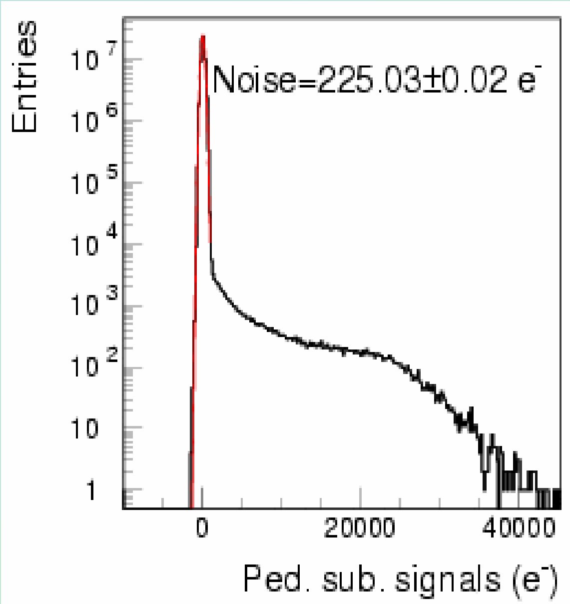
5

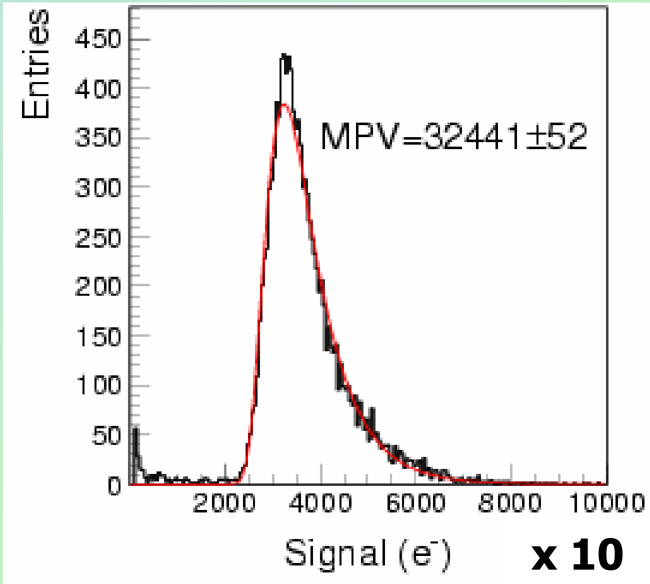
First Test beam results: S/N

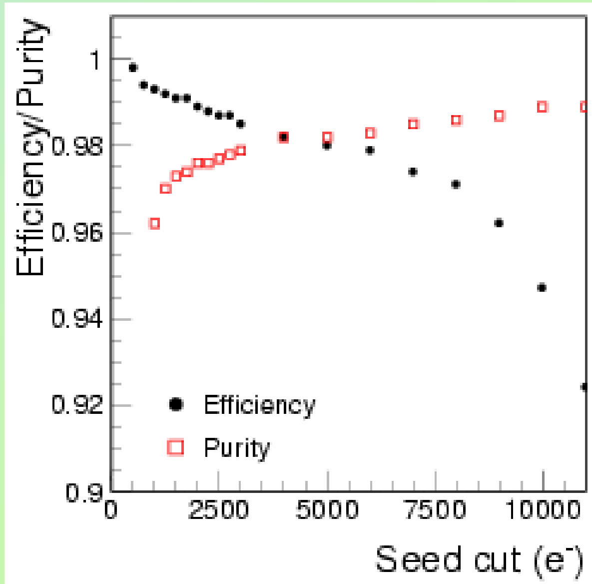
Noise: 225 e$^-$ **Signal$_{MPV}$ = 32500 e$^-$**

- Purity ≈ 0.97
- Efficiency ≈ 0.99

(6 σ Seed cut)







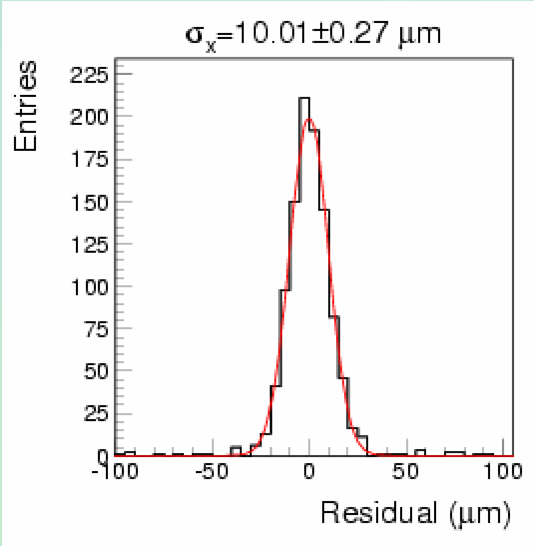
Typical cluster sizes:
4-6 pixels

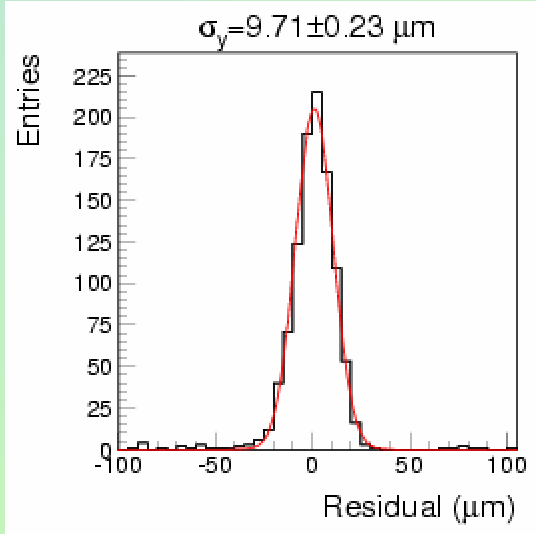
S/N = 144 for 450 µm ➔ S/N ~ 15 for 50 µm

First Test beam results: spatial residuals

Center of Gravity method

stiff tracks (χ^2 – cut)





Preliminary

For 6 GeV e- spatial residuals are **dominated by multiple scattering**

Pixel Size **36 x 28.5 µm**

→ Spatial residuals σ_{res} **~ 10 µm**

→ Binary position reconstruction ($\frac{pitch}{\sqrt{12}}$) σ_{sp} **~ 10.4 x 8.3 µm**

→ Center of Gravity (S/N ~ 144!) expected σ_{sp} **~ 2 - 4 µm**

For spatial resolution studies a high energy beam is needed.

Summary

A ILC prototype system has been build with
- two fast steering chips
- a 64 x 128 DEPFET pixel matrix
- Current based readout chip with on-chip CDS and zero-suppression

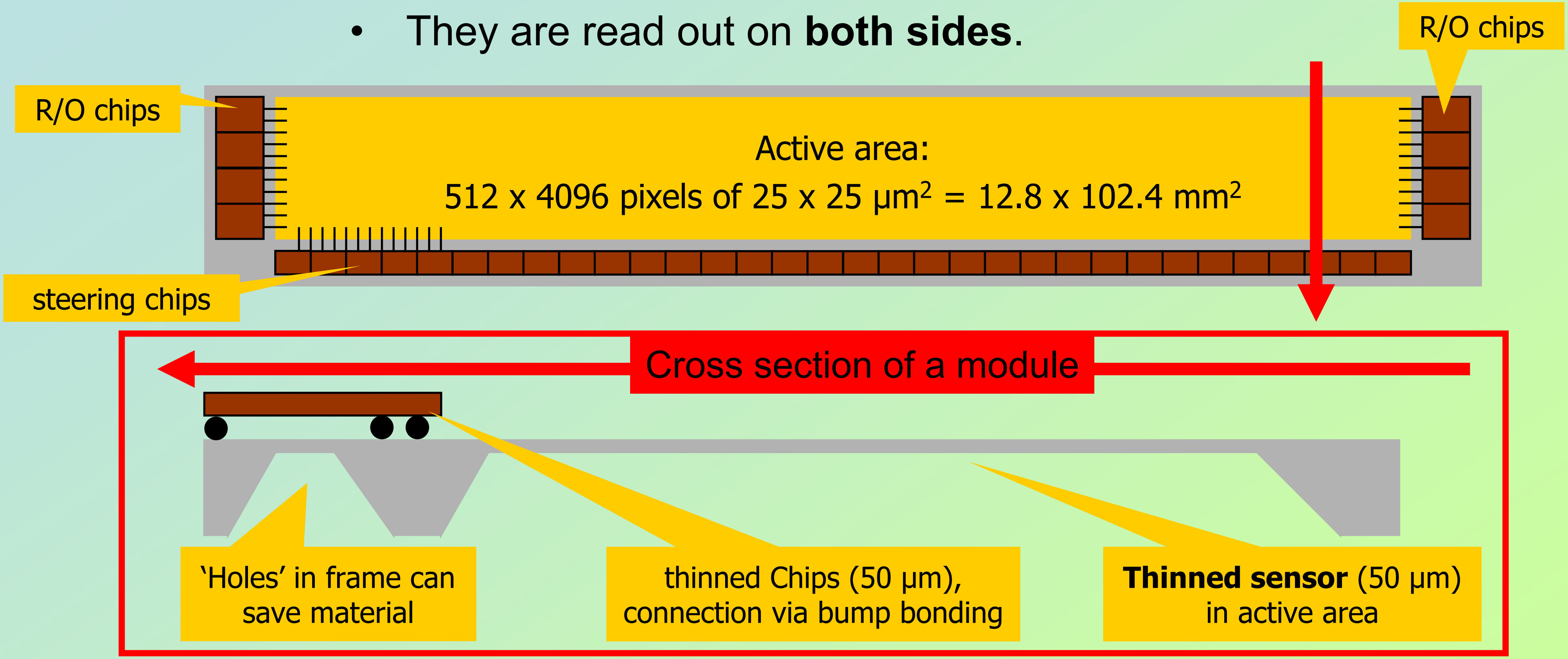
Test beam with 6 GeV e- @ DESY
- Successful operation of the system
- Signal over Noise better than 140 (450 µm) ➔ S/N ~ 15 for 50 µm thick sensors
- efficiency of 99%, spatial residuals dominated by multiple scattering

ILC milestones
- Excellent radiation tolerance of DEPFET pixels up to 1 Mrad (SiO_2) (^{60}Co, 17 keV X-rays)
- Radiation length of 0.11% X_0 can be achieved
- Low power consumption: > 5 W for the entire vertex detector
- Read out chips close to ILC specifications

Next Steps: ➔
- High energy test beam
- Close to full scale prototype module (512 x 512 pixels)

ILC DEPFET Module (Layer 1)

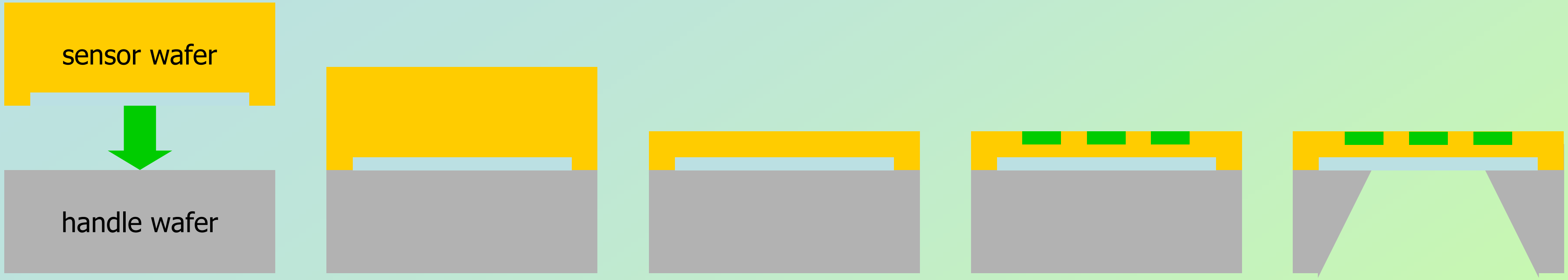
- Modules have active area **~13 x 100 mm²**
- They are read out on **both sides**.



4x100 mm², 50% of 300 µm: 0.05 % X_0 — 2x100 mm², 50 µm: 0.01% X_0 — 13x100 mm², 50 µm: 0.05% X_0

Total radiation length: 0.11% X_0

Thinning DEPFET sensors



1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

first 'dummy' samples:
50µm silicon with 350µm frame

thinned diode structures:
leakage current: <1nA /cm^2

Thinning technology for active area established

Backup I:

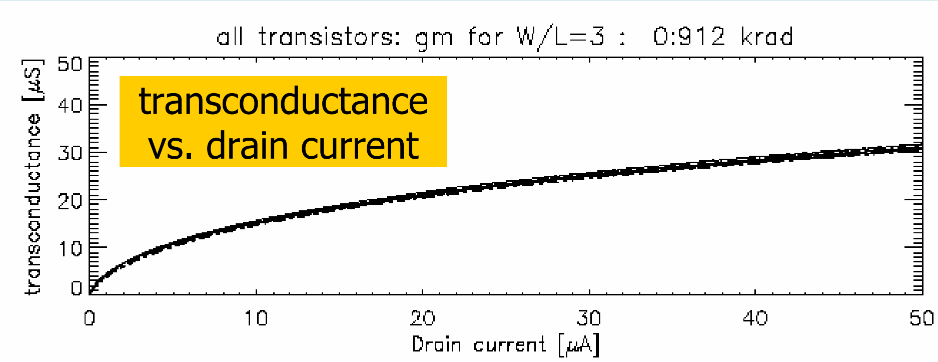
Backup II:

Radiation Tolerance

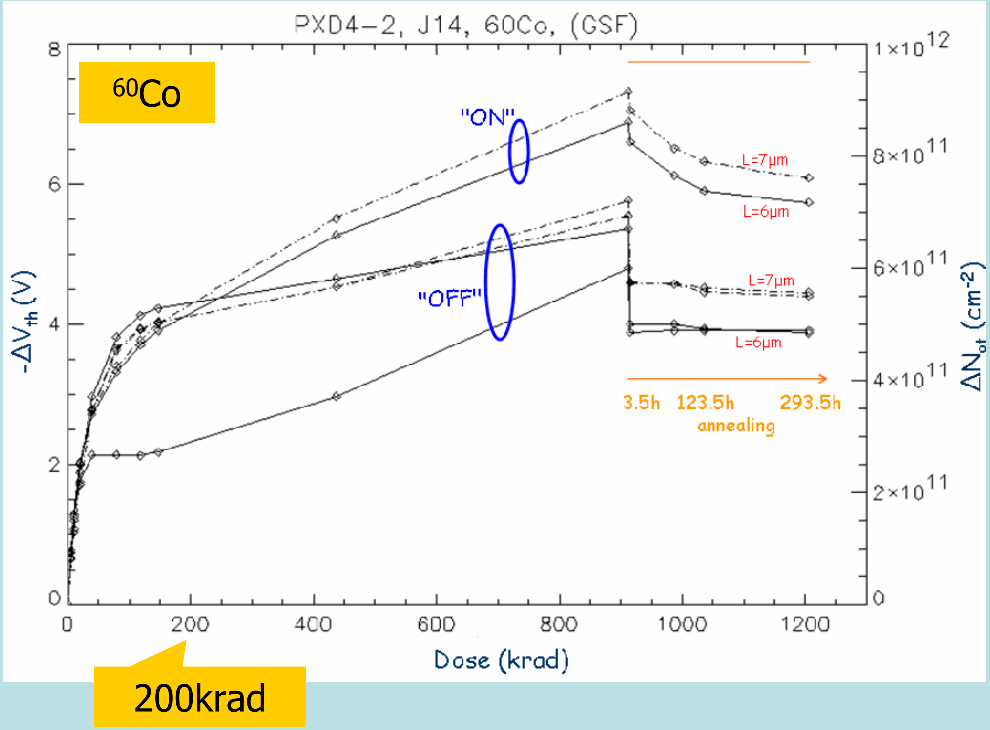
Threshold shift of the (external) MOSFET (oxide thickness ~200nm)

➔ Irradiations with ^{60}Co and X-rays (~17keV) up to ~1Mrad (SiO_2)

➔ Poster by L. Andricek



Transconductance remains unchanged



Threshold shift saturates at -5 V (OFF)

➔ Compensation by variation of bias voltage

excellent tolerance against ionizing radiation