Fabrication of 3D detectors with columnar electrodes of the same doping type

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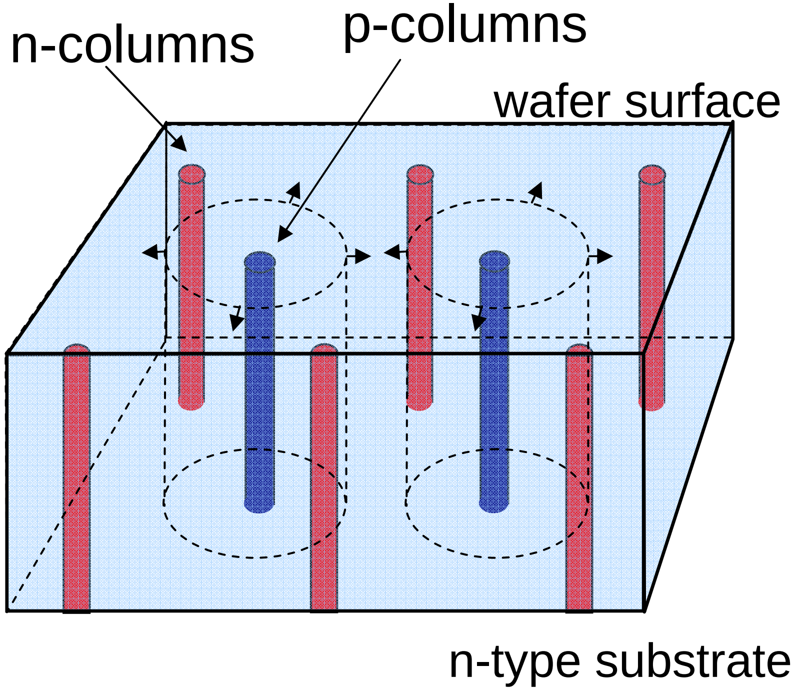
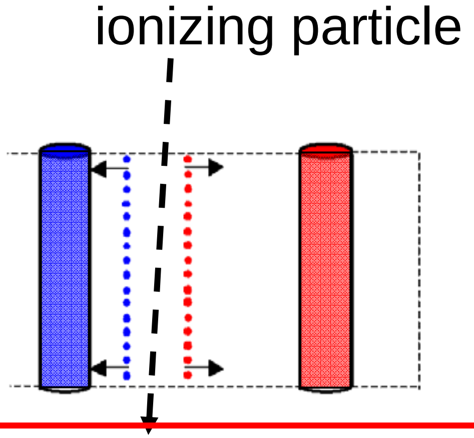
Outline

- Introduction
- Concept of a Single-Type Column 3D detector
- Fabrication of 3D detectors at ITC-irst
- Layout of the first batch
- Preliminary electrical results
- Conclusion

“Standard” 3D detectors - concept

First 3D architecture, proposed by S.I. Parker et al. [1] in 1997:
columnar electrodes of **both doping types**





Short distance between electrodes:
- **low full depletion voltage**
- **short collection distance**

➡ more radiation tolerant than planar detectors!!

DRAWBACK: Fabrication process rather long and not standard => mass production of 3D devices very critical and very expensive.

[1] S.I. Parker, C.J. Kenney, J. Segal, Nucl. Instr. Meth. Phys. Res. A 395 (1997) 328

3D-stc detectors proposed at ITC-irst [2]

ITC irst
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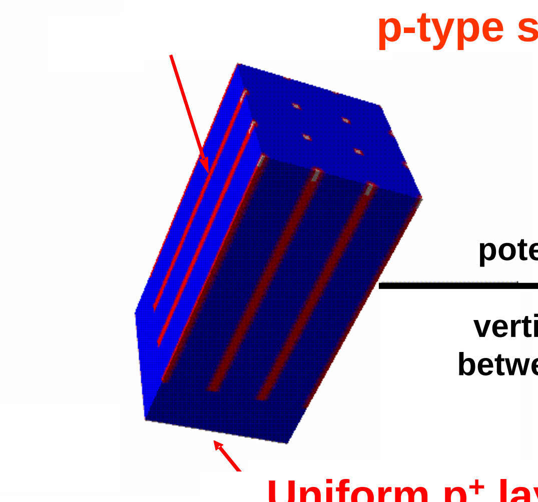
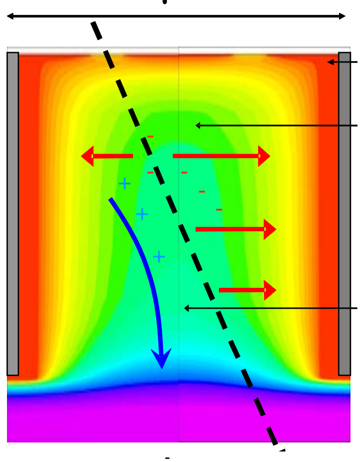




n^+ electrodes

p-type substrate

Uniform p^+ layer

potential distribution

vertical cross-section between two electrodes

50 μm

0 V

-5 V

-8 V

-20 V

ionizing particle

electrons are swept away by the transversal field

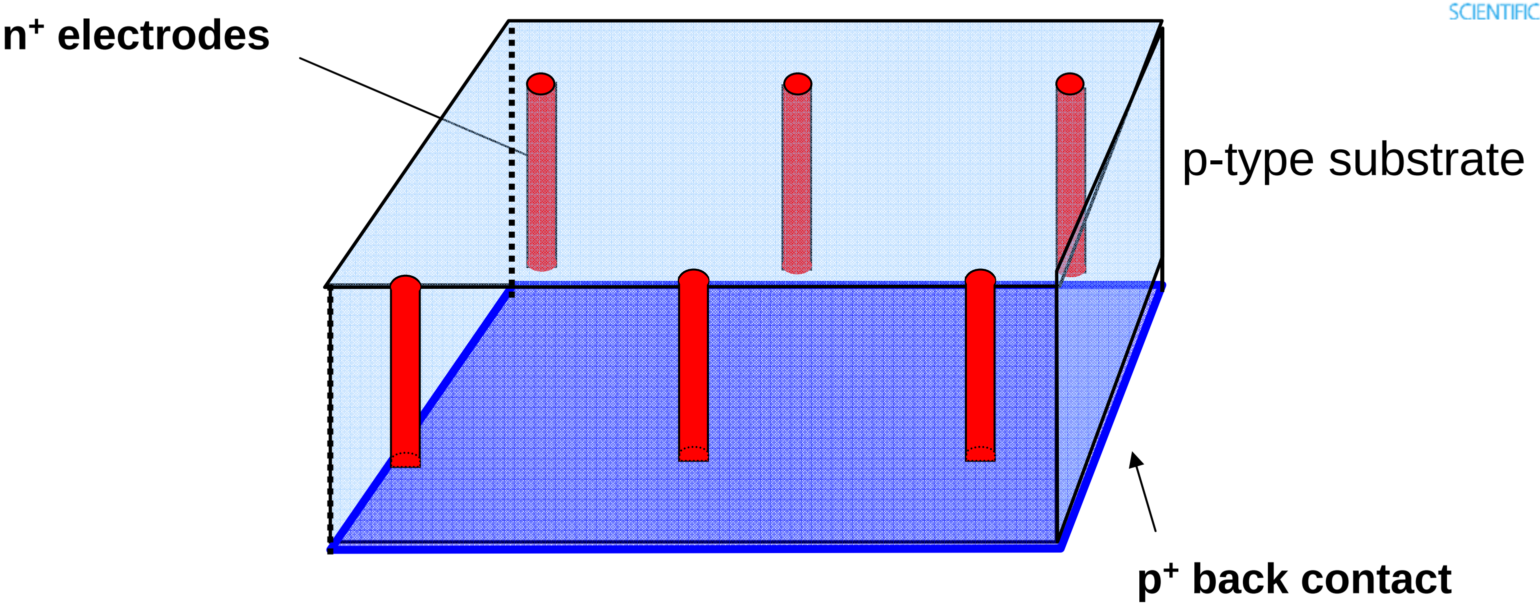
holes drift in the entral region and diffuse towards p^+ contact

<u>Recently</u>, Semi-3D radiation detectors with p+ columns in n-type substrates were proposed by Eränen et al. [3]

[2] C. Piemonte, M. Boscardin, G.-F. Dalla Betta, S. Ronchin, N. Zorzi, Nucl. Instr. Meth. Phys. Res. A 541 (2005) 441

[3] S. Eränen, T. Virolainen, I. Luusua, J. Kalliopuska, K.Kurvinen, M. Eräluoto, J. Härkönen, K. Leinonen, M. Palviainen and M. Koski, 2004 IEEE Nuclear Science Symposium, Conference Record, paper N28-3, Rome (Italy), October 16-22, 2004

Simplification of fabrication process



- **Single-Type-Column**

  Etching and column doping performed only once

- **No hole filling**

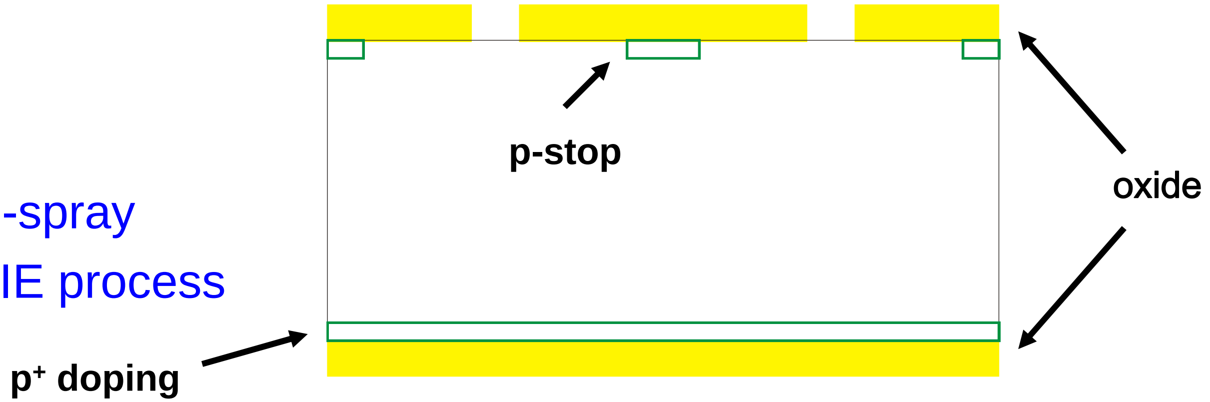
- **Holes not etched all through the wafer**

  No need of support wafer.

  Bulk contact is provided by a backside uniform p^+ implant (single side process)

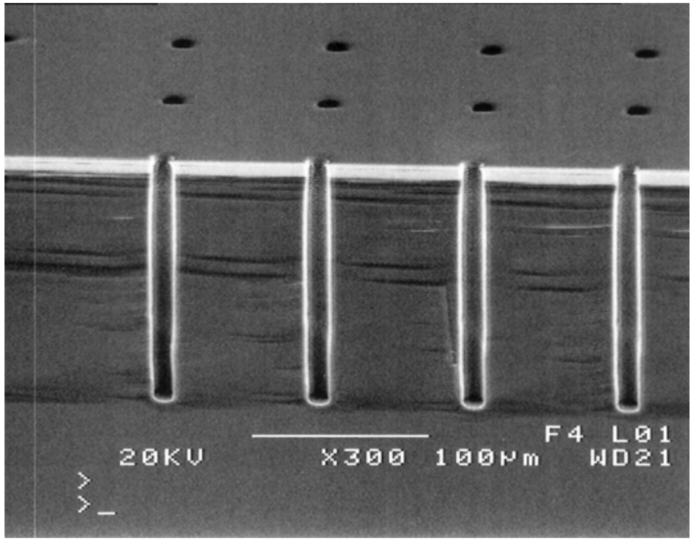
Fabrication process (1)

- initial oxide
- p^+-doping of back
- Isolation: p-stop or p-spray
- masking for deep- RIE process



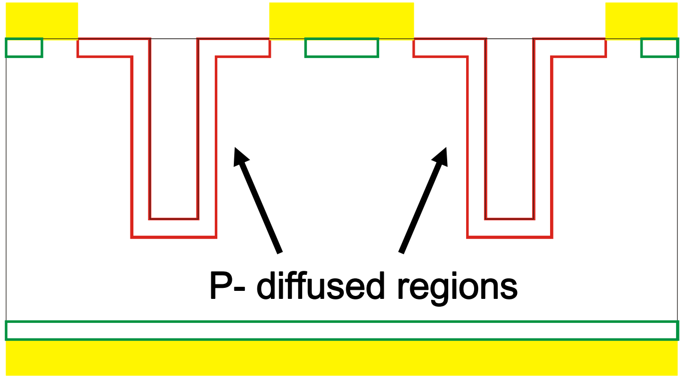
- deep-RIE

(CNM, Barcelona-Spain)

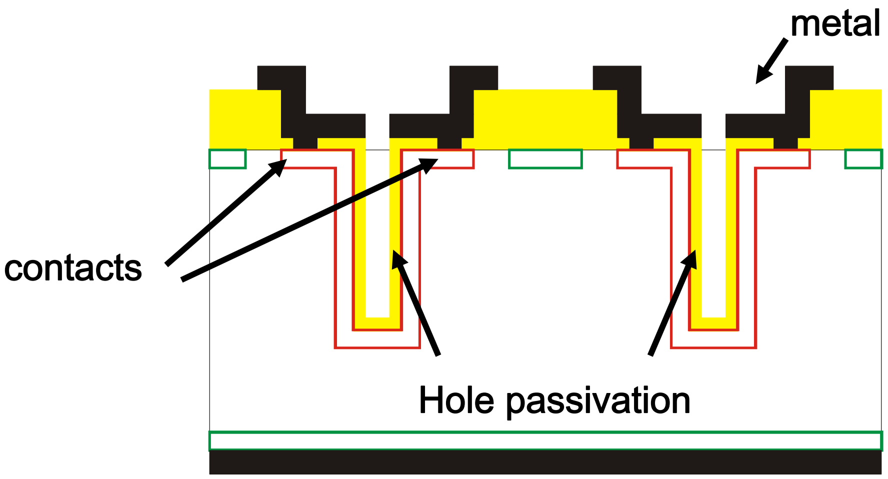


Fabrication process (2)

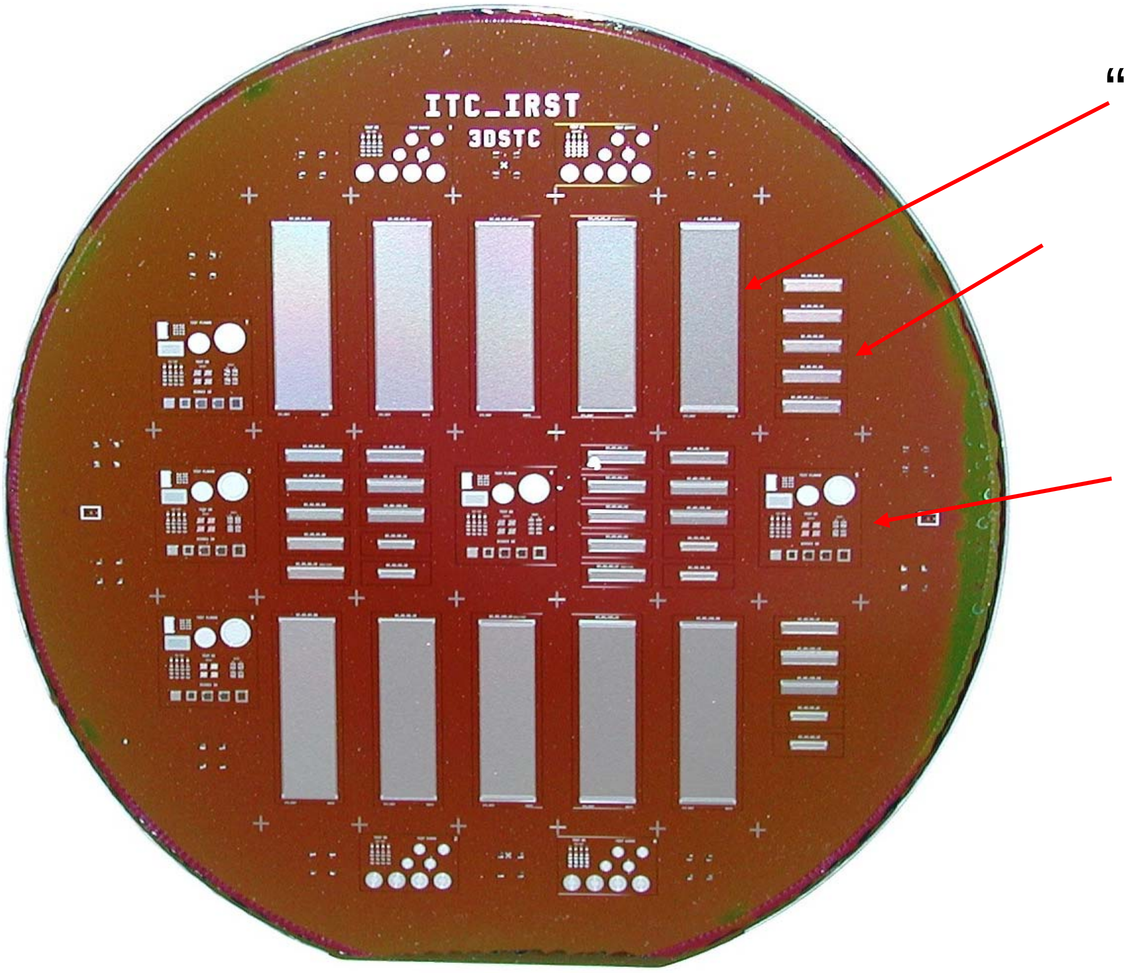
- P-diffusion



- Oxidation (hole passivation)
- Opening contacts
- Metal and sintering



Mask layout



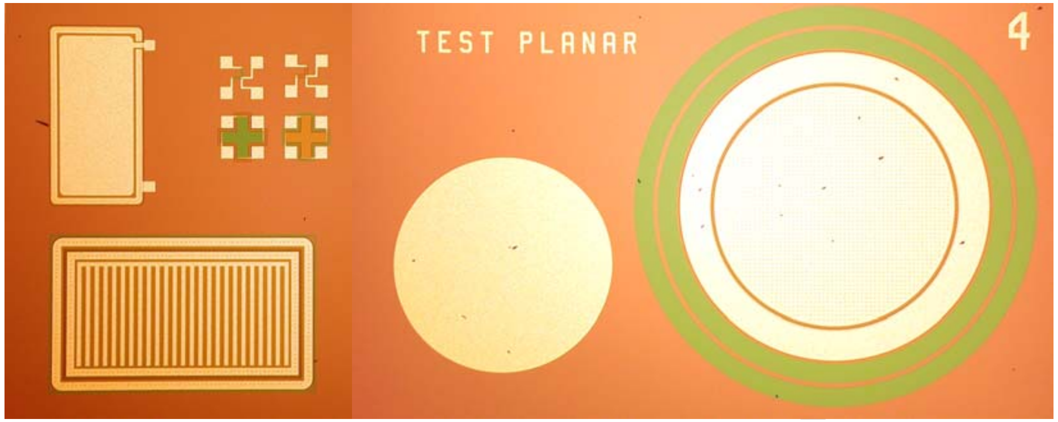
"Large" strip-like detectors

Small version of strip detectors

Planar and 3D test structures

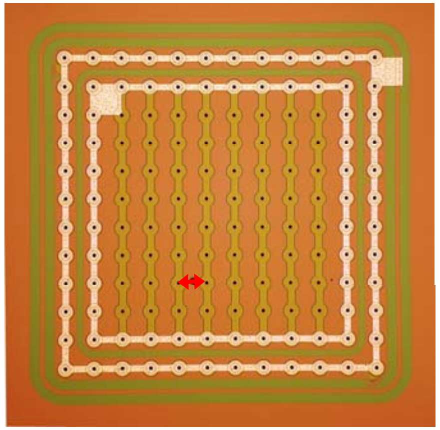
"Low density layout"
to increase mechanical
robustness of the wafer

Mask Layout-Test structures



Standard (planar) test structures

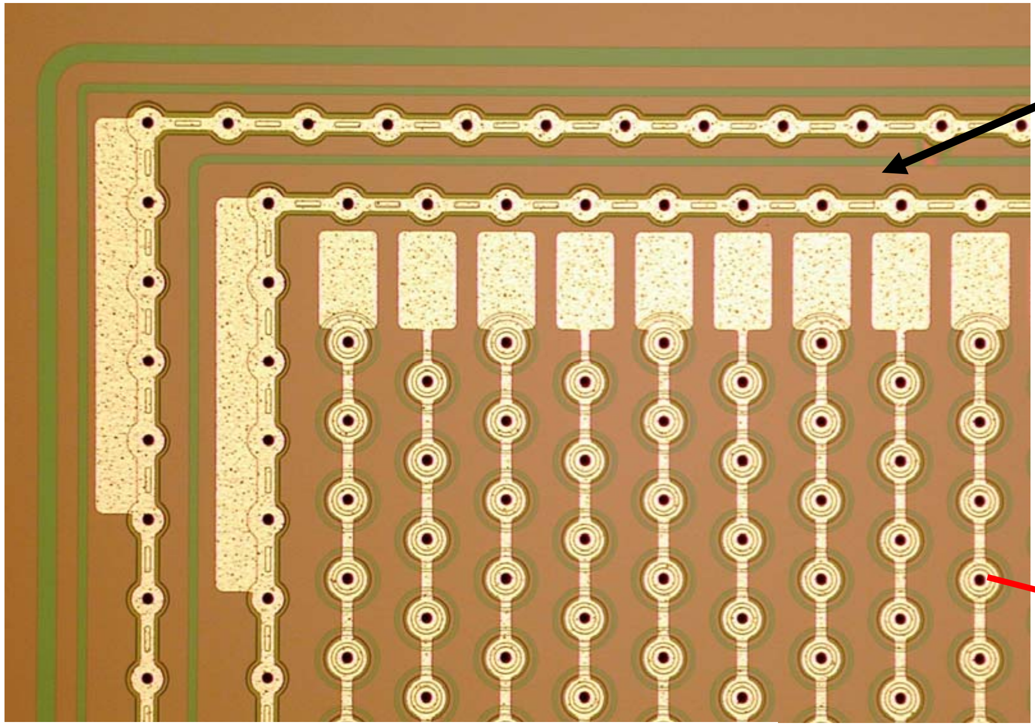
3D-Diode



Pitch 80 µm

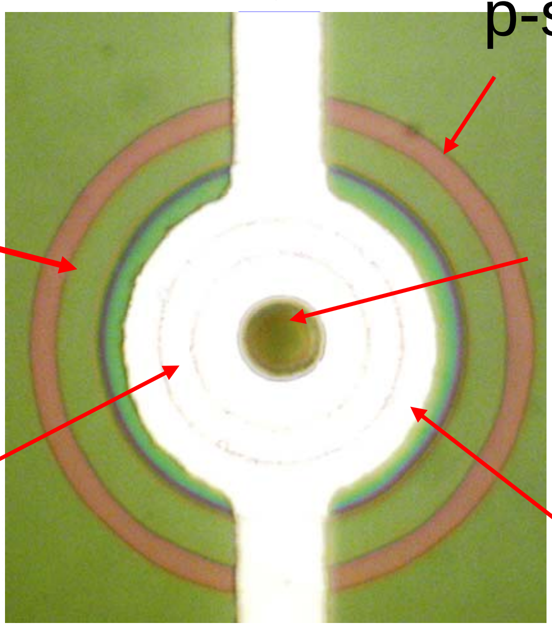
10x10 matrix
Ø hole 10 µm
44 holes GR
p-stop 20 µm
Ø implant 44 µm

Mask layout - strip detectors



Inner guard ring (bias line)

- AC and DC coupling
- Inter-columns pitch 80-100 μm
- Two different p-stop layouts
- Holes Ø 6 or 10 μm



metal

p-stop

hole

Contact opening

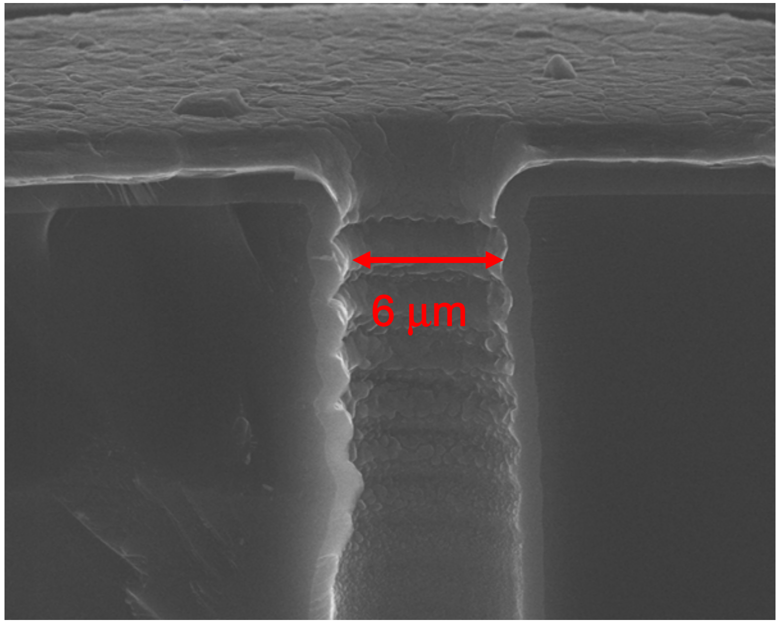
n^+

Fabrication run: main characteristics

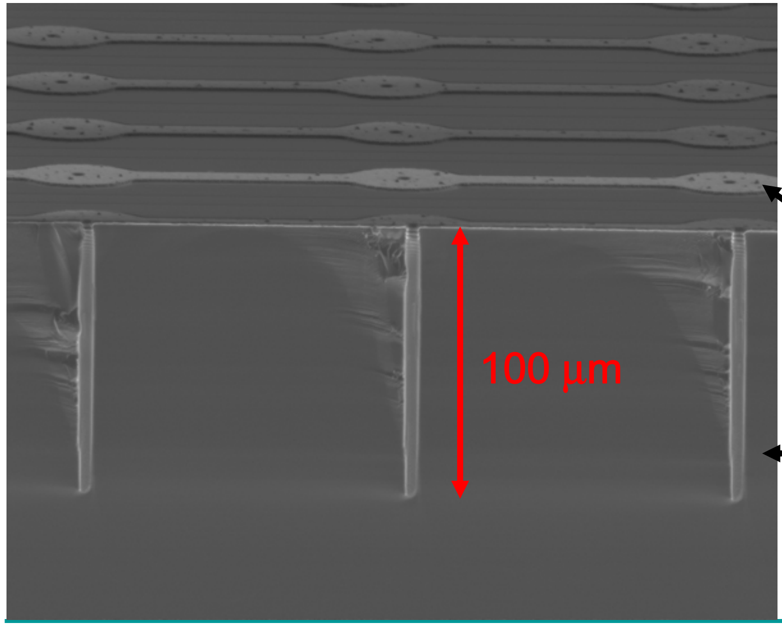
- **Substrate: Si High Resistivity, p-type, <100>**
  - **FZ (500 μm) ρ>5.0 kΩ**
  - **Cz (300μm) ρ>1.8 kΩ**
- **Surface isolation:**
  - **p-stop**
  - **p-spray**

SEM micrographs

Top-side of a column



Portion of a strip detector



Electrical Characterization (1)

Standard (planar) test structures

Parameter	Unit	typical range	
		p-spray	p-stop
Nd	[1E12 cm-3]	1 - 3.5	
Vdep	[V]	200 - 500	
Ileak	[nA/cm2]	1 - 20	
Vbreak	[V]	60 - 140	155 - 175
Tox	[nm]	570 - 585	860 - 875
Qox	[1E10cm-2]	9.5 - 11	6 - 9.6
So	[cm/s]	1.3 - 1.7	7 - 7.5

Different sub-types and thicknesses 2% to 13% variation on single wafer

Ileak measured Below full depletion due to Vbreak

electrical parameters compatible with standard planar processes

➡ DRIE does not endanger device performances

Electrical Characterization (2)

IV measurements

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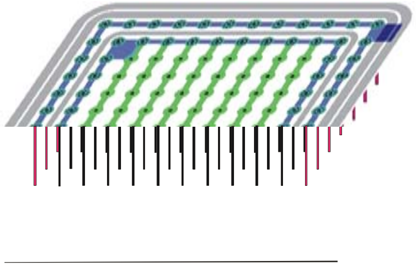
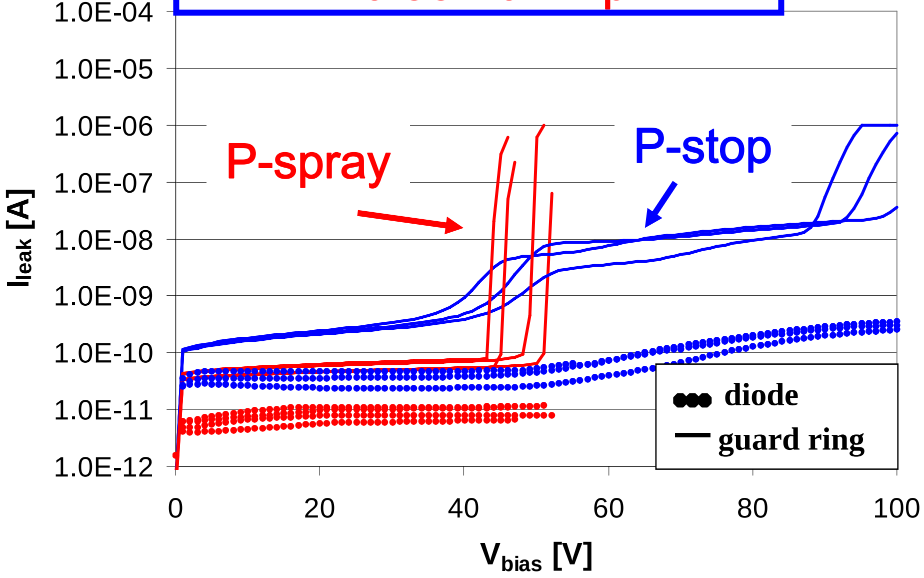
3D-Diode

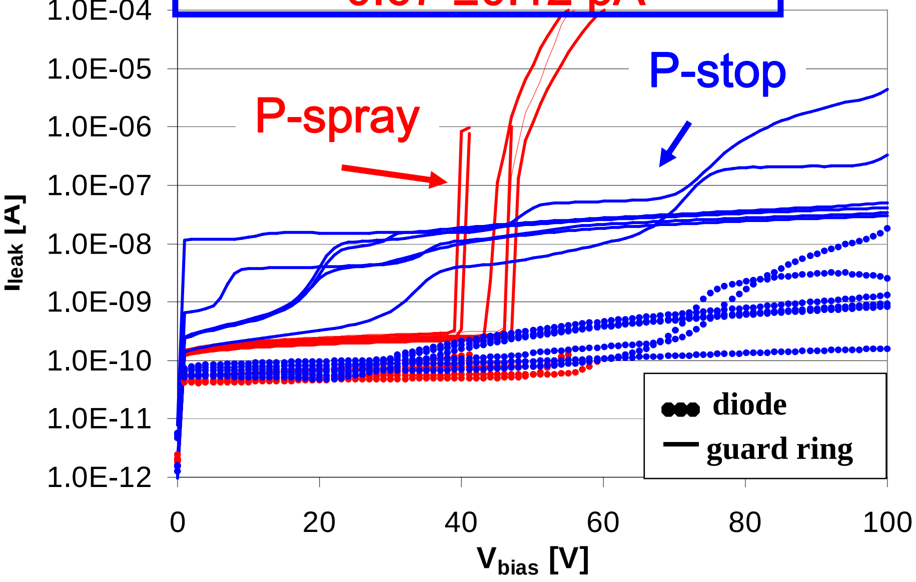


10x10 matrix
Ø hole 10 µm
Pitch 80 µm
Active area ~0.64 mm^2

CZ I_{leak}/column @ 20V
0.33 ±0.24 pA



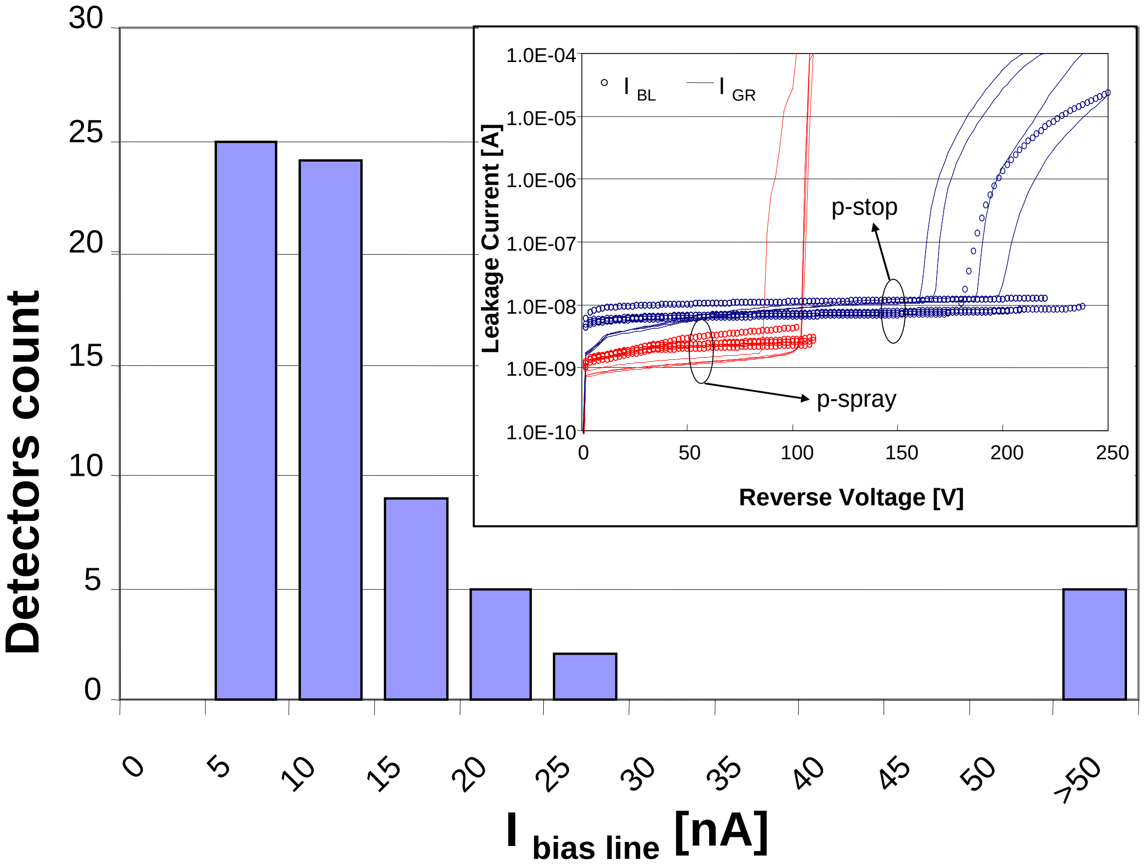
FZ I_{leak}/column @ 20V
0.67 ±0.12 pA



Electrical Characterization (3)

Strip detectors

Current distribution @ 40V of 70 different devices



1detector:
230 columns x 64 strips on 1 cm² ~ 15000 columns

↓

average current per column < 1pA

Good process yield

Conclusions

A **new type of 3D detector** has been conceived which leads to a **significant simplification of the process**:

- hole etching performed only once
- no hole filling
- no wafer bonding

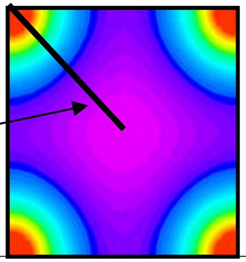
First production is completed:

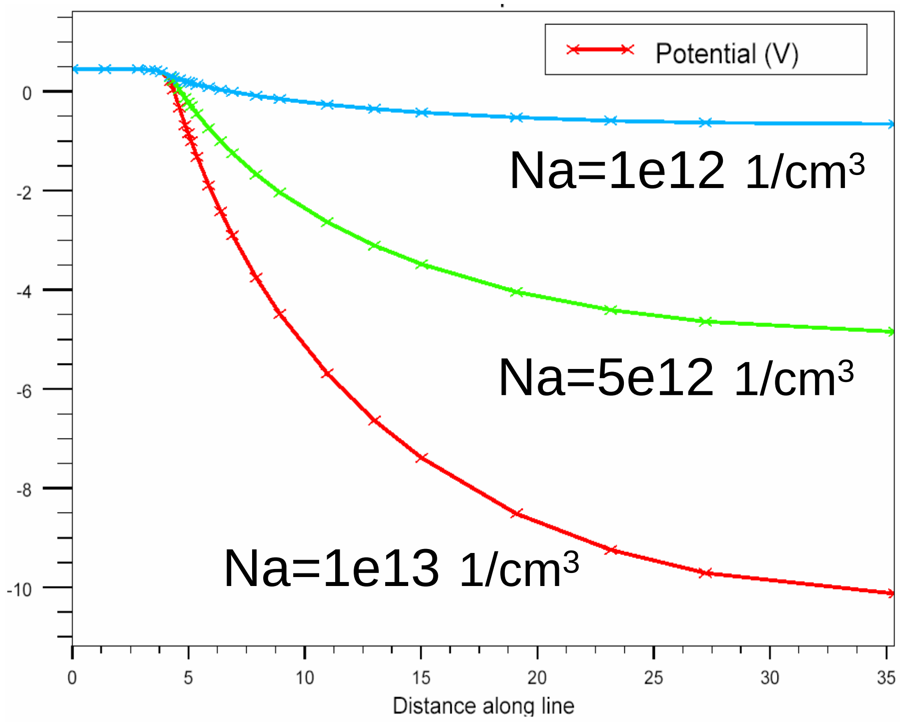
- Good electrical parameters (DRIE does not endanger device performances)
- Low leakage currents **< 1pA/column** and BD **~ 50V** for p-spray and **>100V** for p-stop in 3D diodes
- Good performances of strip detectors (Current/hole **< 1pA/column** for **93%** of detectors)

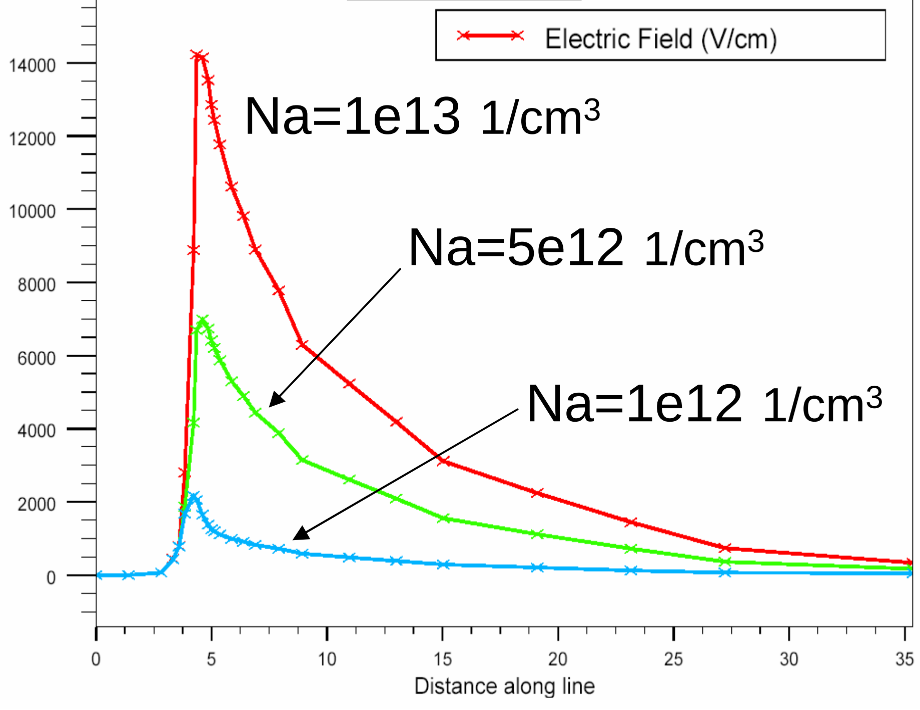
Accurate analysis of CV measurement results is in progress with the aid of TCAD simulations

TCAD Simulations - static

Potential and Electric field along a cut-line
from the electrode to the center of the cell



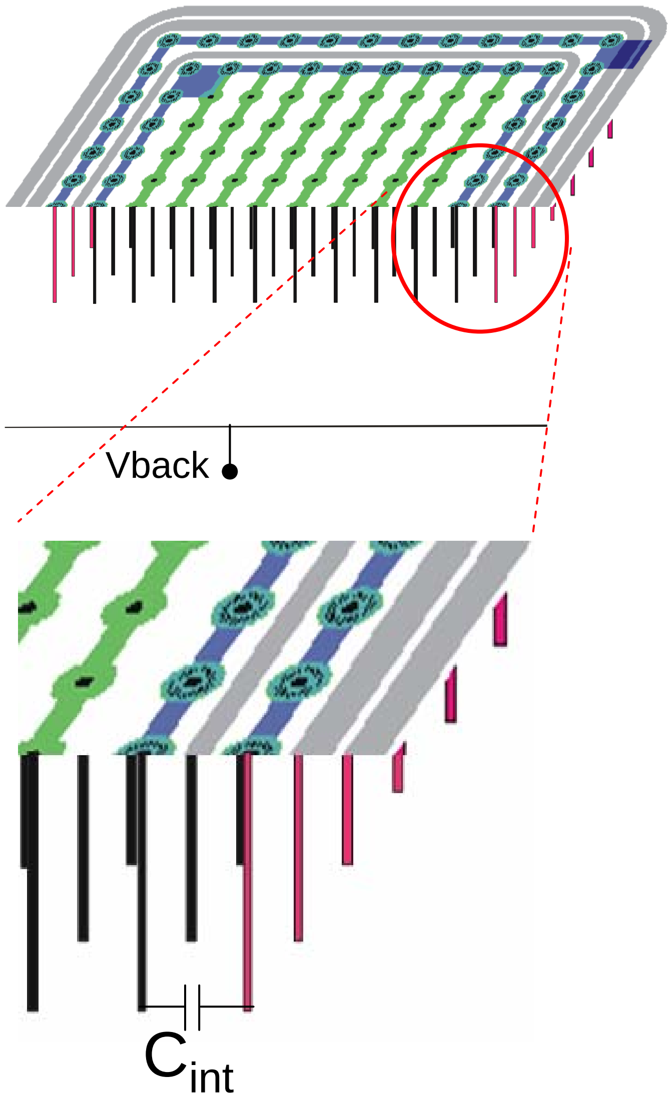




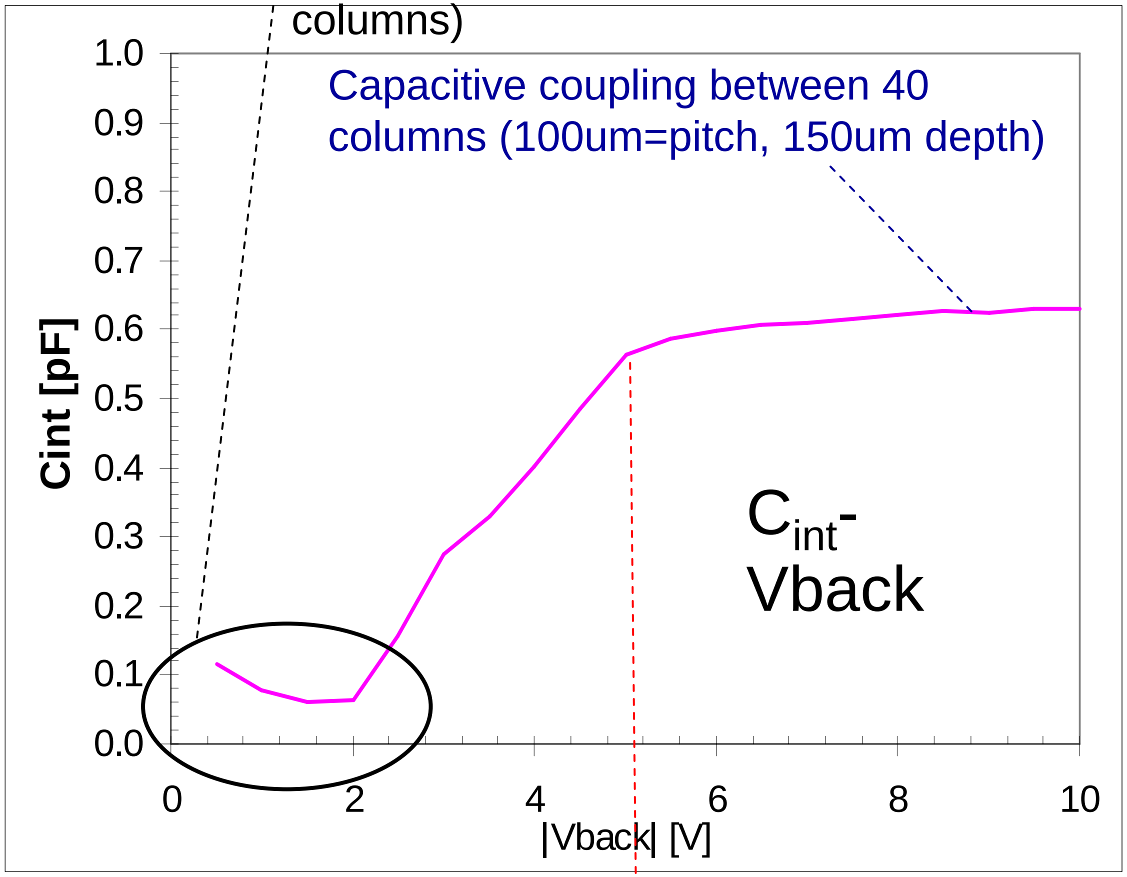
To increase the electric field strength one can act on the substrate doping concentration

Lateral depletion-voltage

Preliminary “3d-diode”/GR capacitance measurements



Weak capacitive coupling at very low voltages (conductive substrate layer between columns)



Capacitive coupling between 40 columns (100um=pitch, 150um depth)

~ 5V lateral full depletion voltage (100µm pitch)

Backplane full-depletion-voltage

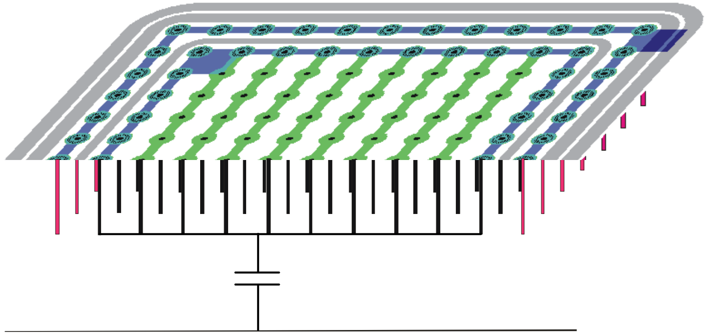
Preliminary “3d-diode”/back capacitance measurements

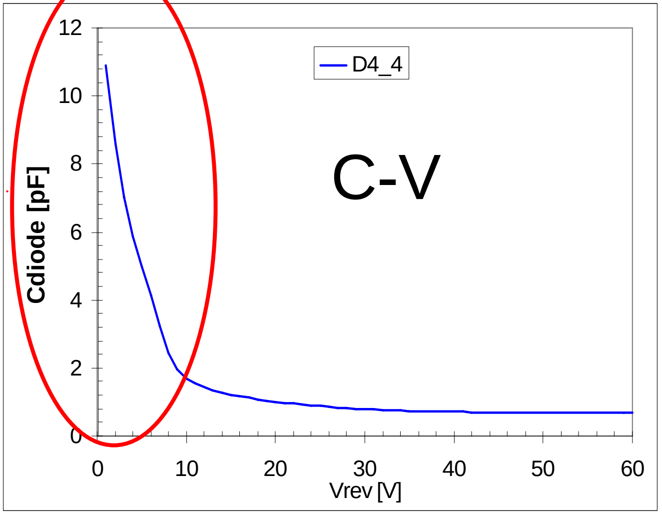
Lateral depletion contribution to measured capacitance at low voltages

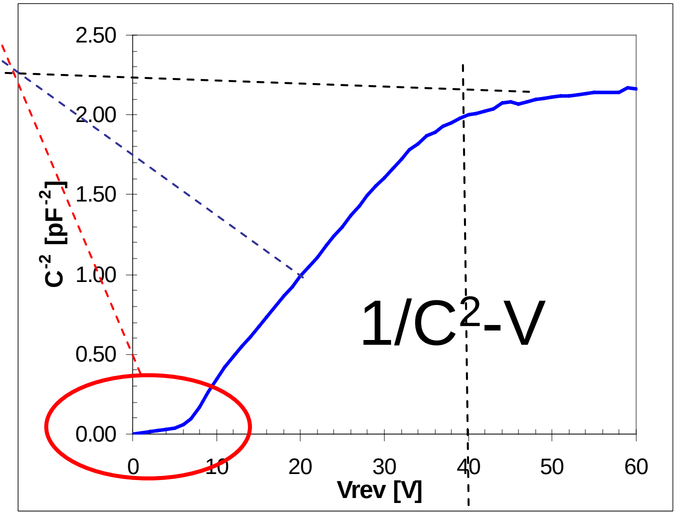
Linear $1/C^2$ vs V region corresponding to the same doping level of planar diodes

Saturation capacitance corresponding to a depleted width of ~ 150µm)

→ Column depth ~ 150µm







~ 40V full depletion voltage (300µm wafer)