A multichannel detector array with 768 pixels

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UWA
- Array Concept – Keith Birkinshaw
- Science Driver & XPS – Andy Evans, Steve Evans, Alex Vearey-Roberts

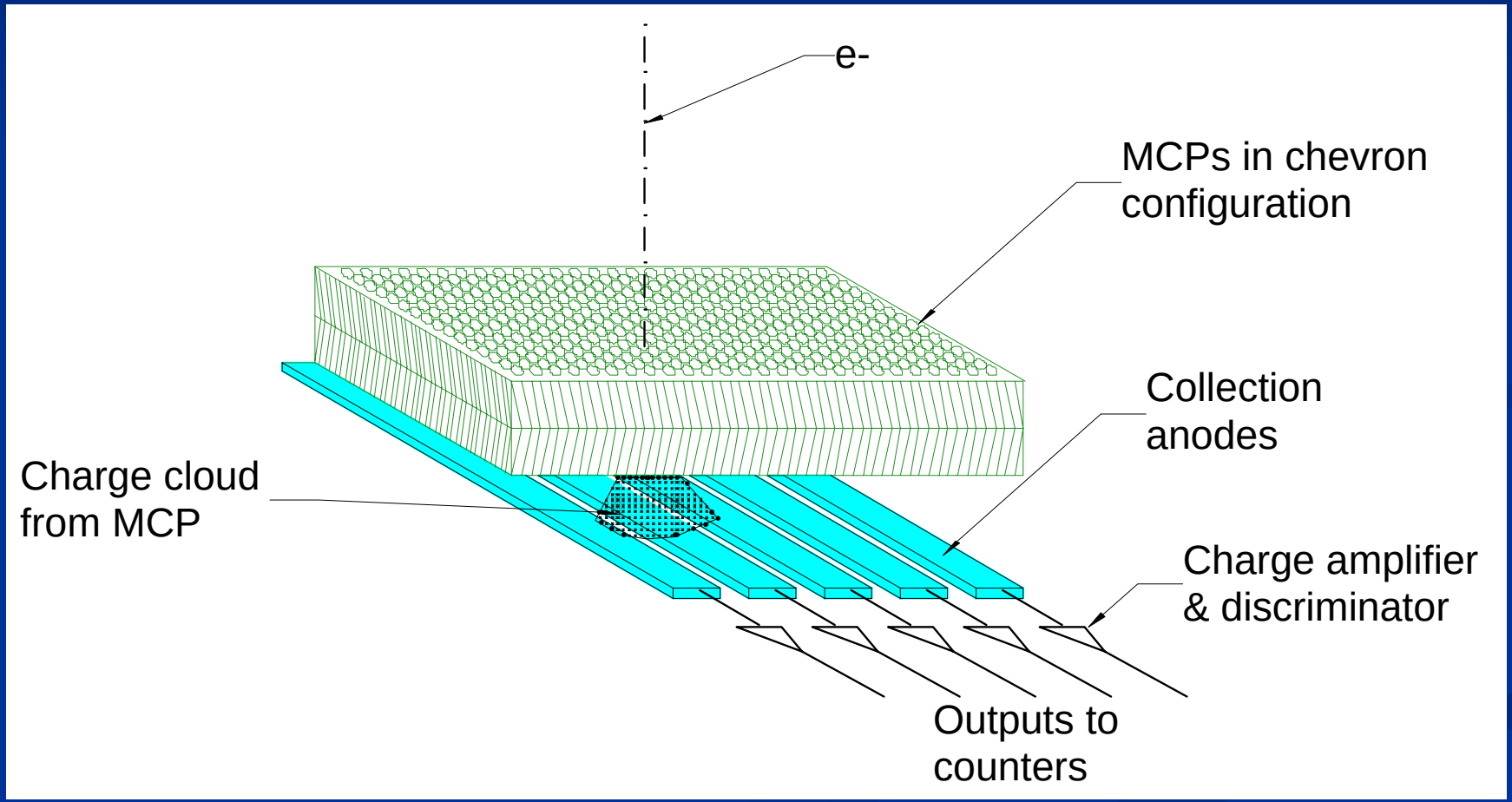
RAL/CCLRC/SRS
- Control Electronics – Richard Farrow, Jon Headspith, Richard Stephenson, Steve Burges
- CLAM4 mounting – Dave Teehan
- SRS 4.1 – Vin Dhanak, George Miller

EPSRC WDA/KEF

Technology Overview

- Multianode readout for Microchannel Plate
- Custom ASIC
  - Linear Array of Collection Anodes
  - Charge Sensitive Amp + Discriminator + 16-bit Counter
  - Readout Circuitry
- Ceramic Substrate & MCP Holder
- Floating Control Electronics (ex vacuum)
  - Interface with TCP/IP
  - MCP power supply

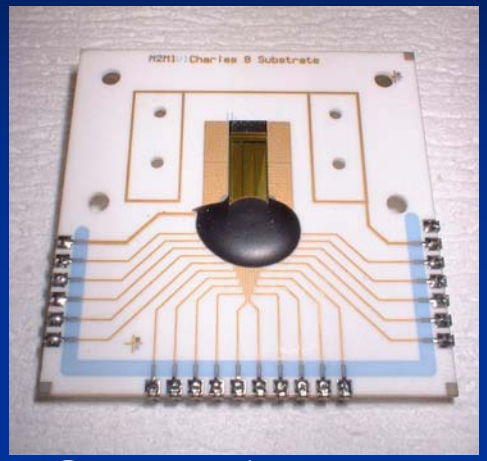
Principle of Operation



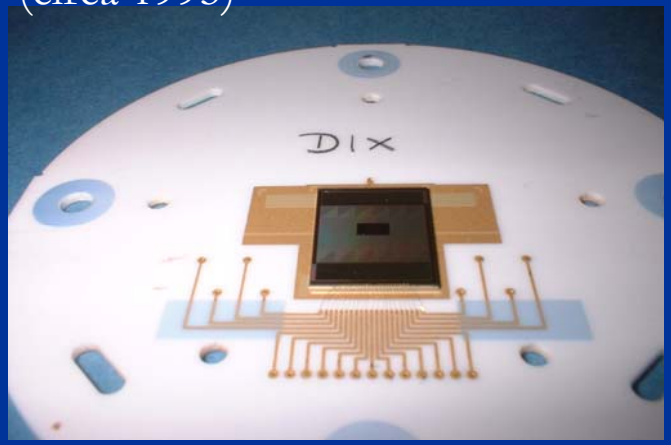
Advantages of in-vacuum electronics

- Made possible by ASIC integration
- Reduce stray & cross couple capacitances.
  - >10pF → <1pF
- Low impedance I/O through vacuum envelope
- Reduced I/O wire count
- Mass produced electronics
  - Make Moore's law work for you!
- Pulse Counting → Highly Linear

Detector Chips Past and Present



MCD192 – 5mm x 2mm
(circa 1995)



MCD384 – 9.6mm x 2mm (May 2003)

MCD768 – 19.2mm x 3mm (Aug 2004)

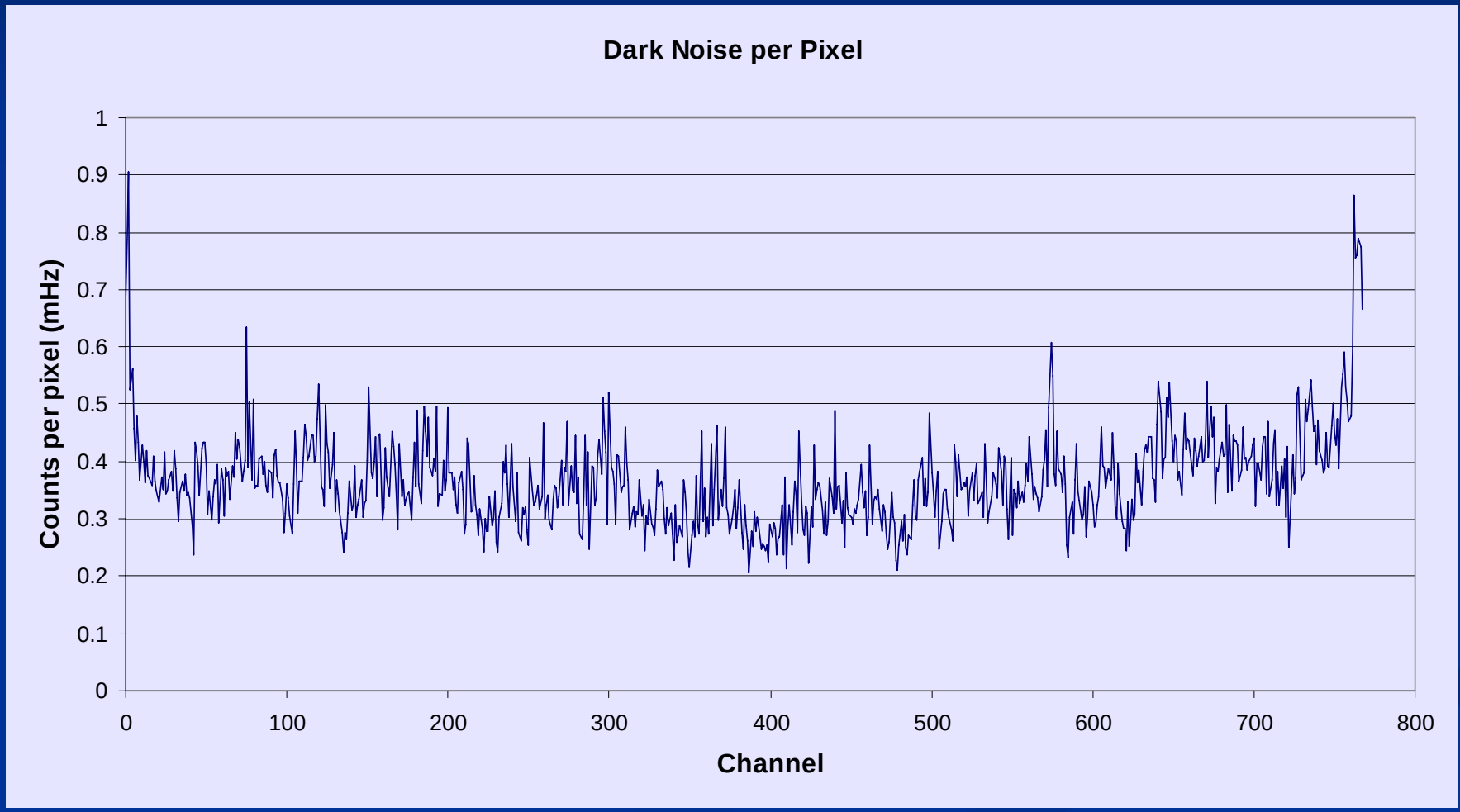
MCD768 ASIC Specification

- 768 collection anodes
- Anode size: 25µm × 3mm
- Total Active Area: 19.2mm × 3mm
- 16-bit counter per anode
- ≈330,000 transistors
- Fabricated on Alcatel 0.5µm process via Europractice

Detector Noise Floor

- Due to β decay from potassium in MCP glass
- Simply measured - X-rays OFF
- Accumulate of long period (121 hr)
- Average of 160 counts pixel^{-1}
- 3.7×10^{-4} Hz pixel^{-1}

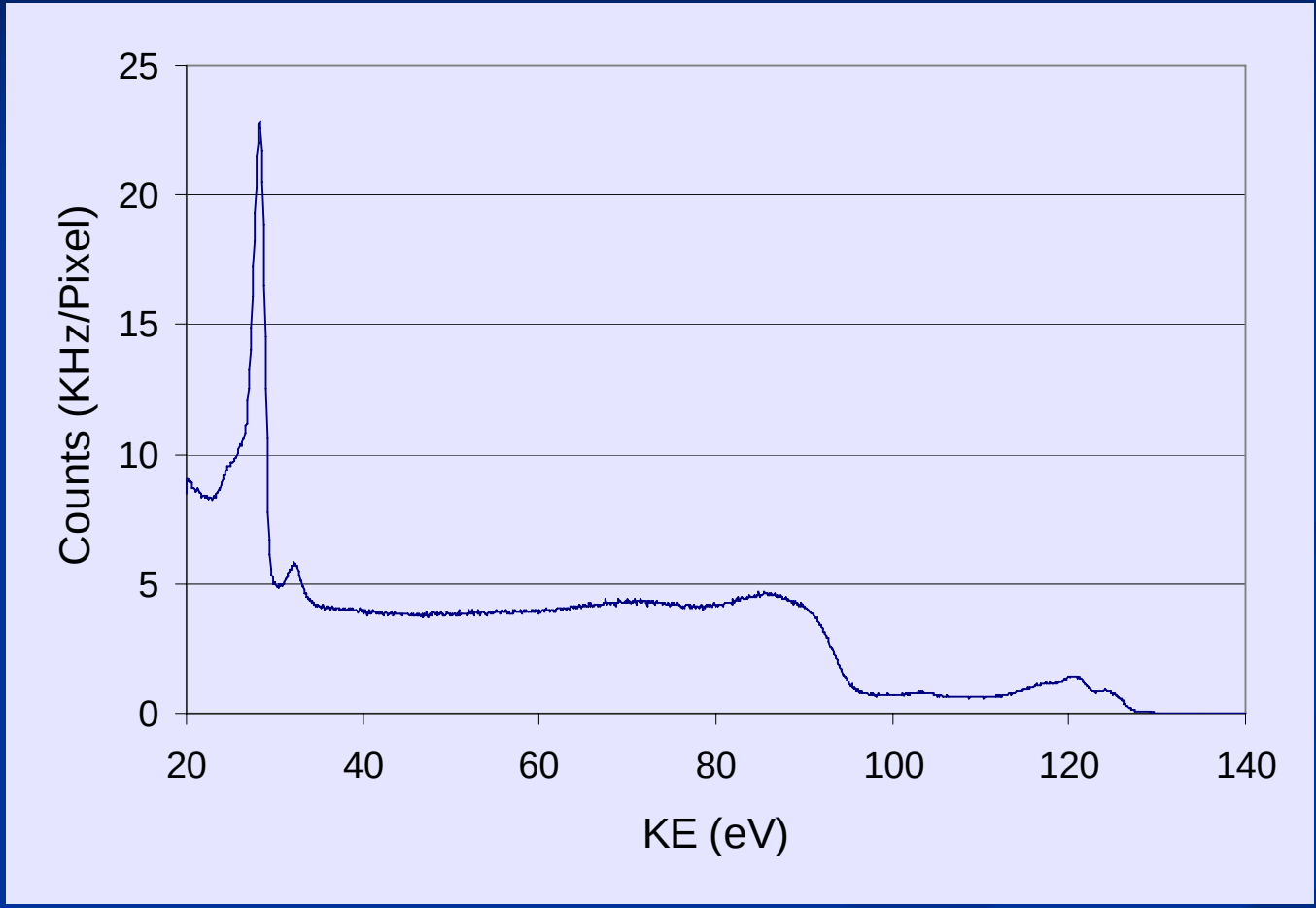
Detector Noise Floor



Maximum Count Rate

- Particularly important for high brightness sources
- Measured core level spectrum
- Extract single pixel from data
- Equivalent to 25μm analyser exit slit
- Measured in excess of 2×10^4 Hz Pixel^{-1}
- Due to recharging limitation of MCP

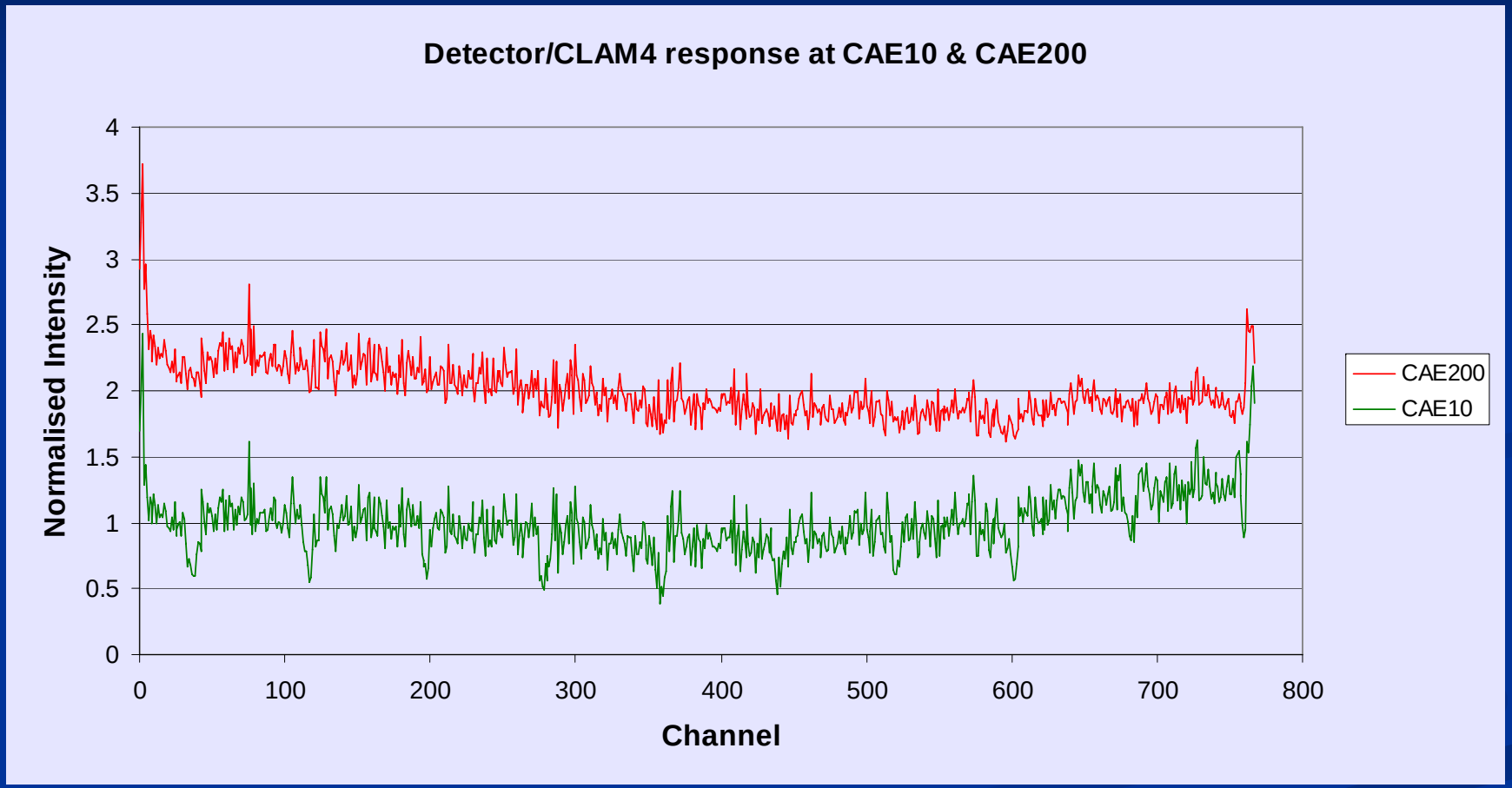
Maximum Count Rate



Uniformity across array

- ASIC tolerances + MCP variations
  ➔ Non-uniformity at detector
- Also focal plane distortion in analyser
- Illuminate array as uniformly as possible
- Result depends on analyser pass energy
- Curves shown for CAE10 & CAE200
  - curve for CAE200 offset for clarity

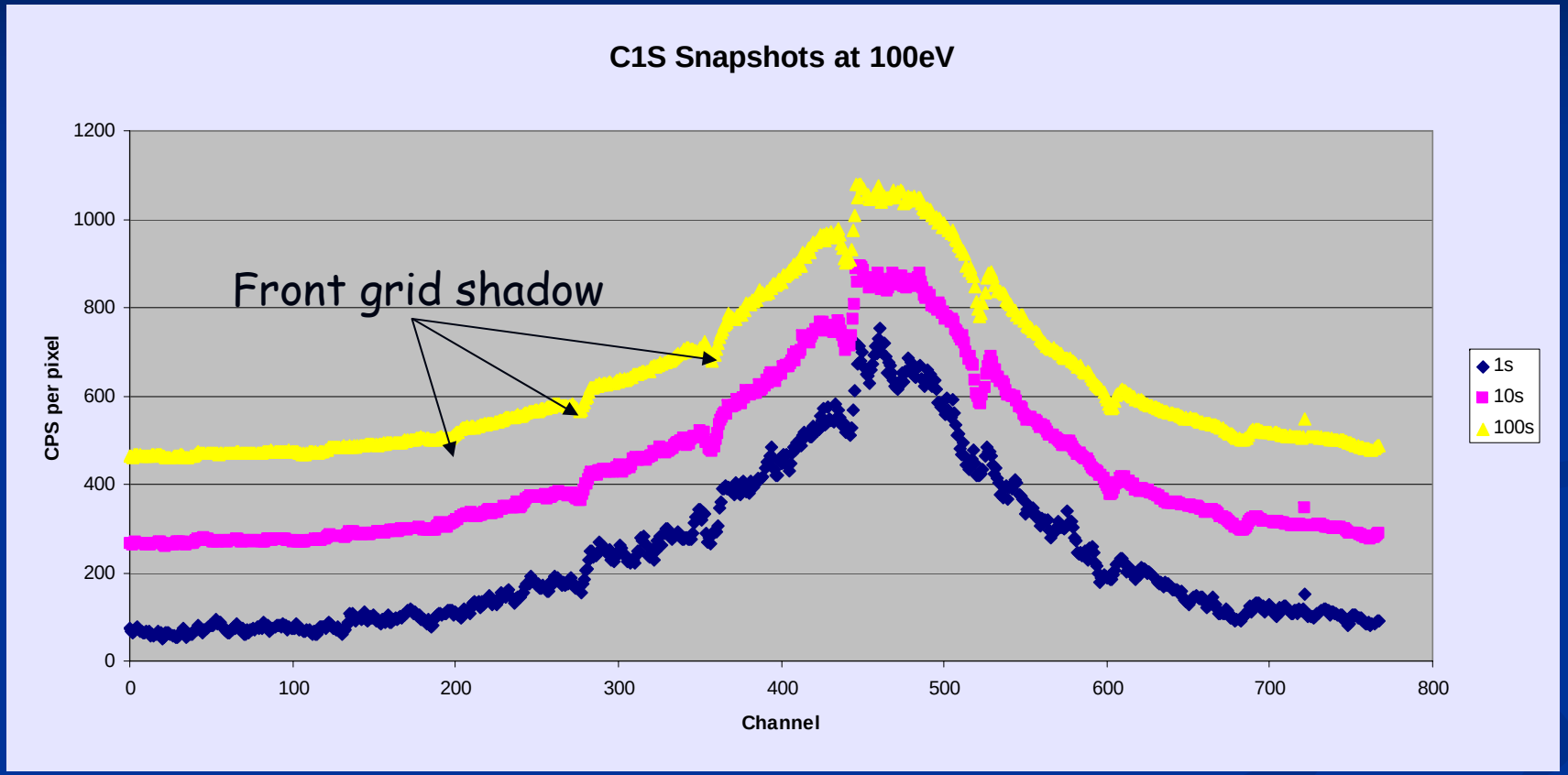
Uniformity across array



Applications

- 'Virtual channeltron' – select pixels & sum in software. Acts as channeltron with variable entrance slit.
- 'Weaving mode' – Combine data from all pixels during sweep
- 'Snapshot' – Image feature on array, monitor peak amplitude and position

Snapshot Readout from MCD768

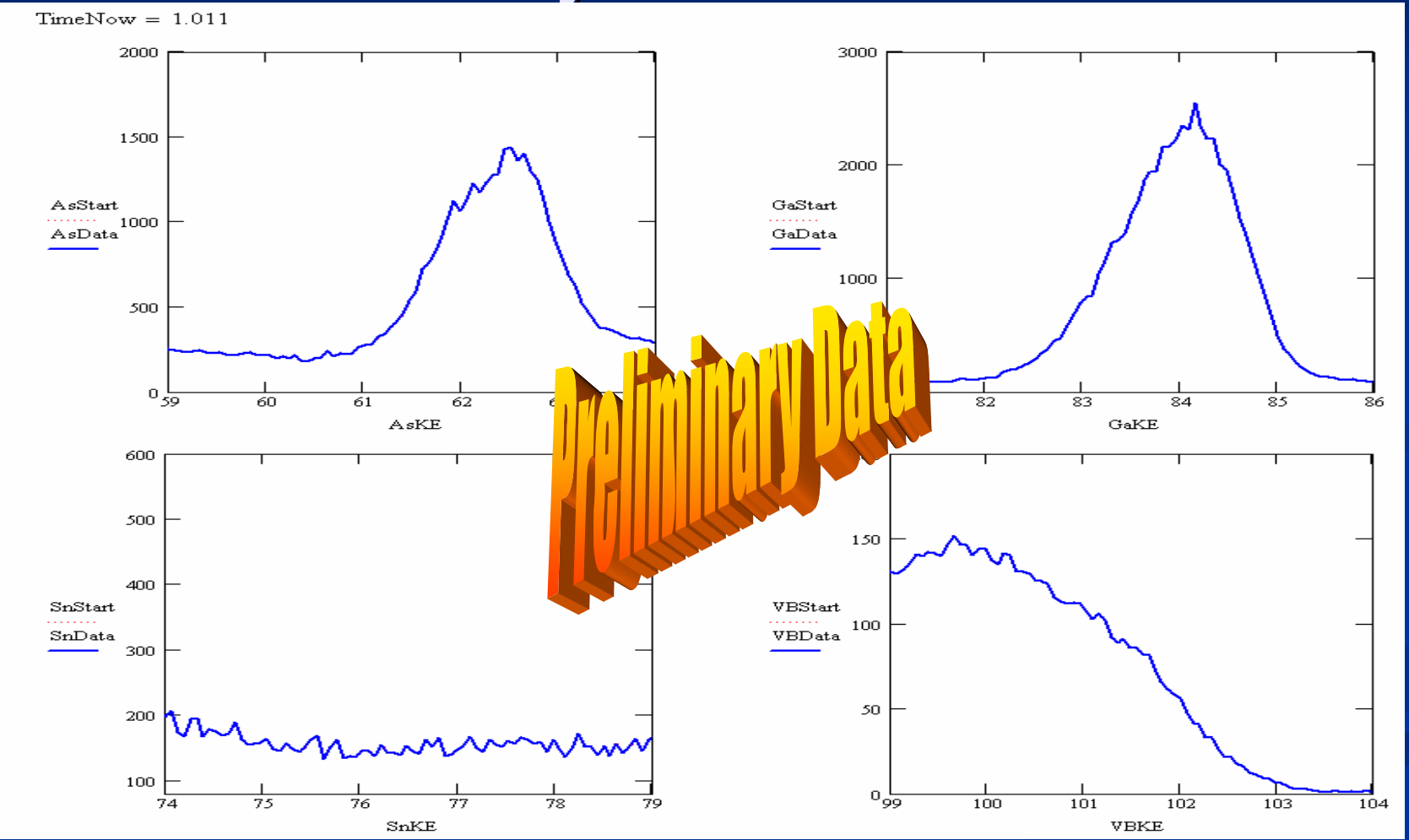


XPS of Diamond <111>, MgKα source, UWA

Monitoring deposition of SnPc on GaAs by real-time XPS

- A.Evans, A.Vearey-Roberts, A.McGlynn [In Preparation]
- Monitor Ga3d, As3d, Sn4d & Valence band edge during SnPc deposition
- Reading cycle
  - Ga3d – 1s/As3d – 1s/Sn4d – 1s/Valence – 10 s
- With settling time + overheads ➔ ~20s/cycle
- 764 cycles over 4 hour experiment

Monitoring deposition of SnPc on GaAs by real-time XPS



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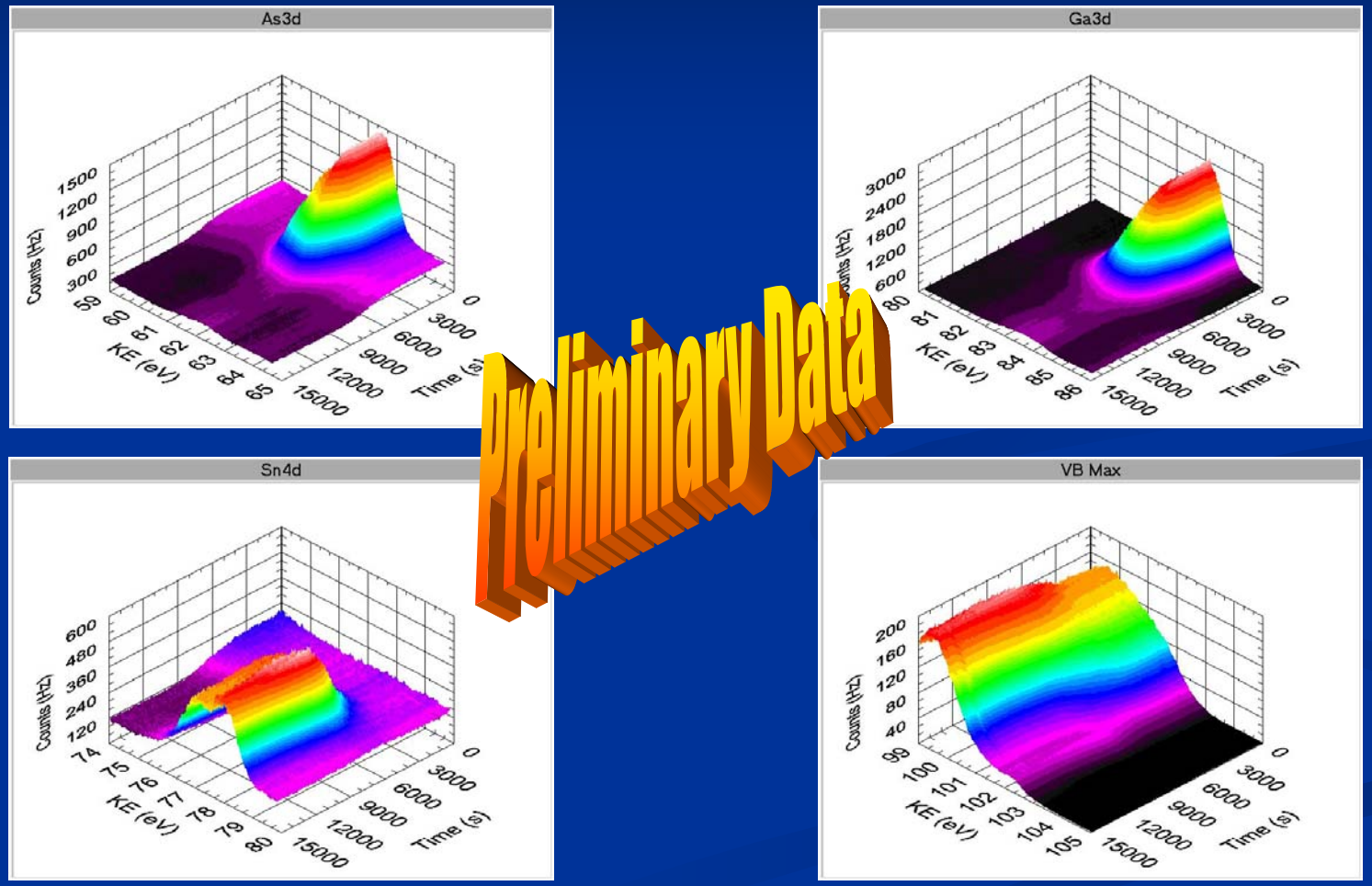

Conclusions

- 768 channel MCP based detector
- 25um channel pitch
- 19.2mm in dispersive direction
- Noise: ~ 4×10^{-4} Hz Pixel^{-1}
- Max Count Rate: >$2x10^{4}$ Hz Pixel^{-1}

Further Work

- Analyser focal plane
  - Comparative study
- Longer array – reticle stitching
  - SRIF
- 2D Detector