Development of a thinned back-illuminated CMOS Active Pixel Sensor for Extreme Ultra-Violet Spectroscopy and Imaging in Space Science

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CMOS Active Pixel Sensor Development for Solar Orbiter

- Background
- 4k x 3k CMOS Sensor
- Back-thinning
- New Developments
- Future programme
- Summary

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CMOS Active Pixel Sensor Development Programme

1999

- Design / modelling of pixel test structures (0.5 and 0.7 µm CMOS).

2000

- Fabrication / testing of pixel test structures.
- Established collaboration with e2v (Formerly Marconi and EEV).
  - Exchange of designs / ideas, Packaging, Testing.
  - Back-thinning → Unique capability.
- Design of 512 x 512 pixel sensor (0.5 µm CMOS).

2001

- Fabrication of 512 x 512 pixel prototype sensors.
- e2v thinning test structures and 512 x 512 prototypes.
- Planning for Solar Orbiter (move to 0.25 µm CMOS).

2002

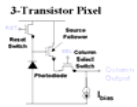
- Design and fabrication of 4k x 3k pixel sensor.
- Testing of thinned 512 x 512 pixel sensors.

2003

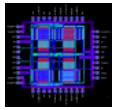
- Initial characterisation of 4k x 3k sensors.

2004/2005

- Thinning and Front-etch EUV enhancement of 4k x 3k sensors.
- Optimisation / design of high dynamic range pixels.
- Design / fabrication of new Test Structures.

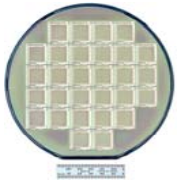


Pixel design

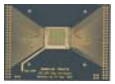


CAD layout

Packaged chip

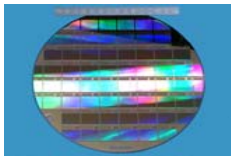


6-inch wafer

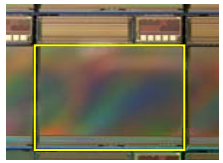


Test PCB

10Hz test image

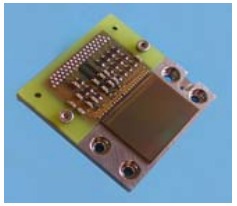


8-inch wafer



4kx3k pixel sensor die

First test image



Sensor module

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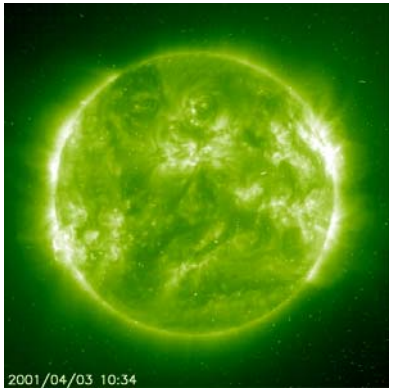
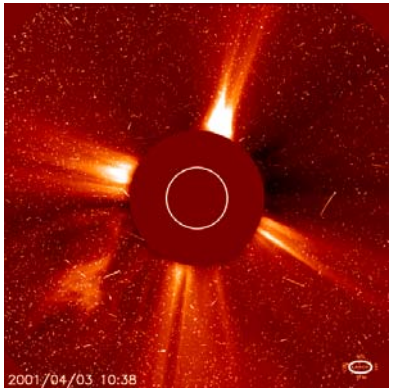
EUS - Spectrometer for ESA's Solar Orbiter Mission (2015?)

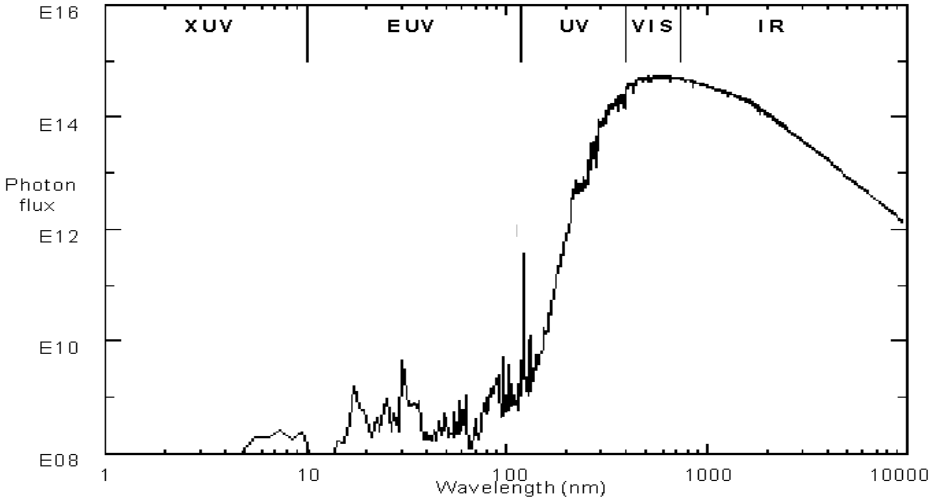
- **To study the atmosphere and heliosphere of the Sun from close up.**

Original Requirements

- **Large format sensors: 4k x 4k pixels.**
- **Small pixel size: 5 μm.**
- **Science-grade dynamic range, noise, linearity, etc.**
- **EUV sensitivity (17nm to 120nm).**
- **Radiation hard.**
- **Low power.**







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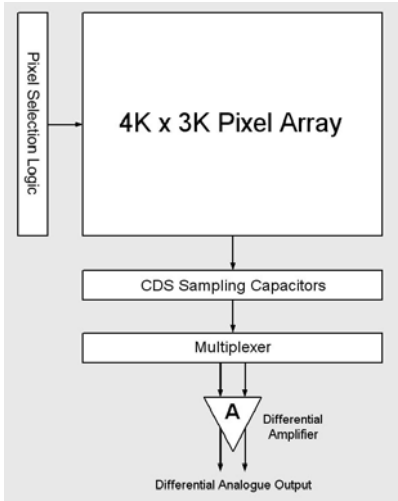
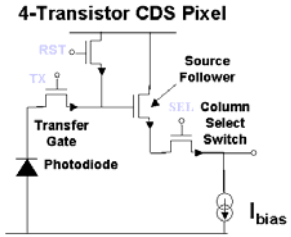
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter

- 5 µm pixel size.
- 12 bit dynamic range.
- 4-transistor CDS pixel for low noise.
- 0.25 µm CMOS process.
- EUV sensitivity by back-thinning or front-etch.

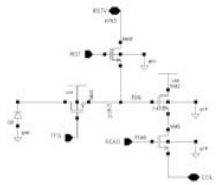


Architecture

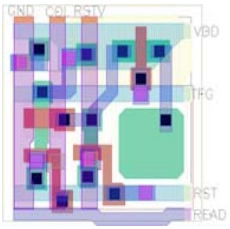
Pixel Circuit

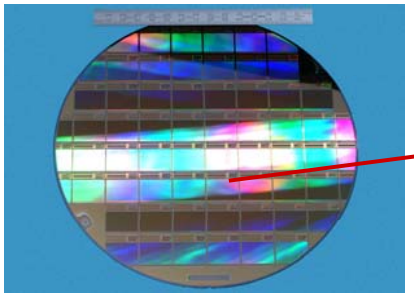


CAD Simulation

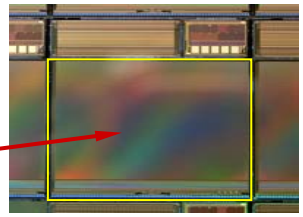


CAD Layout

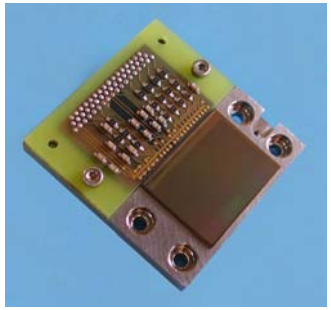




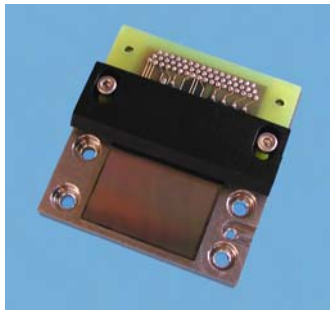
8-inch Wafer 0.25 µm CMOS



4kx3k pixel sensor die



Sensor mounted on an invar block and wire-bonded to a PCB



Bond-wire protection-cover fitted

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4k x 3k Pixel Sensor Development for ESA's Solar Orbiter

Progress to date . . .

Early test image 4kx3k pixels with JPEG compression for display purposes

Modified Batch 1 wafers

- Early test image from modified Batch 1 wafers.
- Sufficient progress to proceed with the new Batch 2 wafers.

Next Steps . . .

- Characterisation of Batch 1 samples for:
  - Readout noise
  - Dynamic range
  - Linearity
  - Leakage current
  - Pixel uniformity
  - Radiation tolerance, etc.

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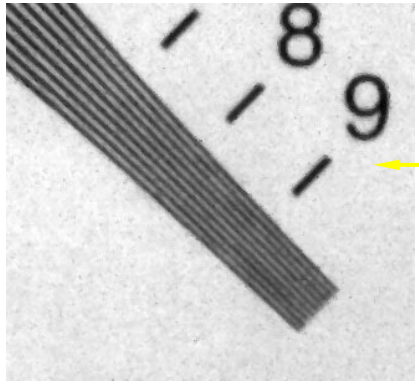
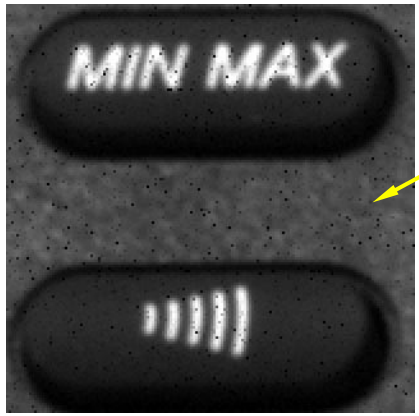
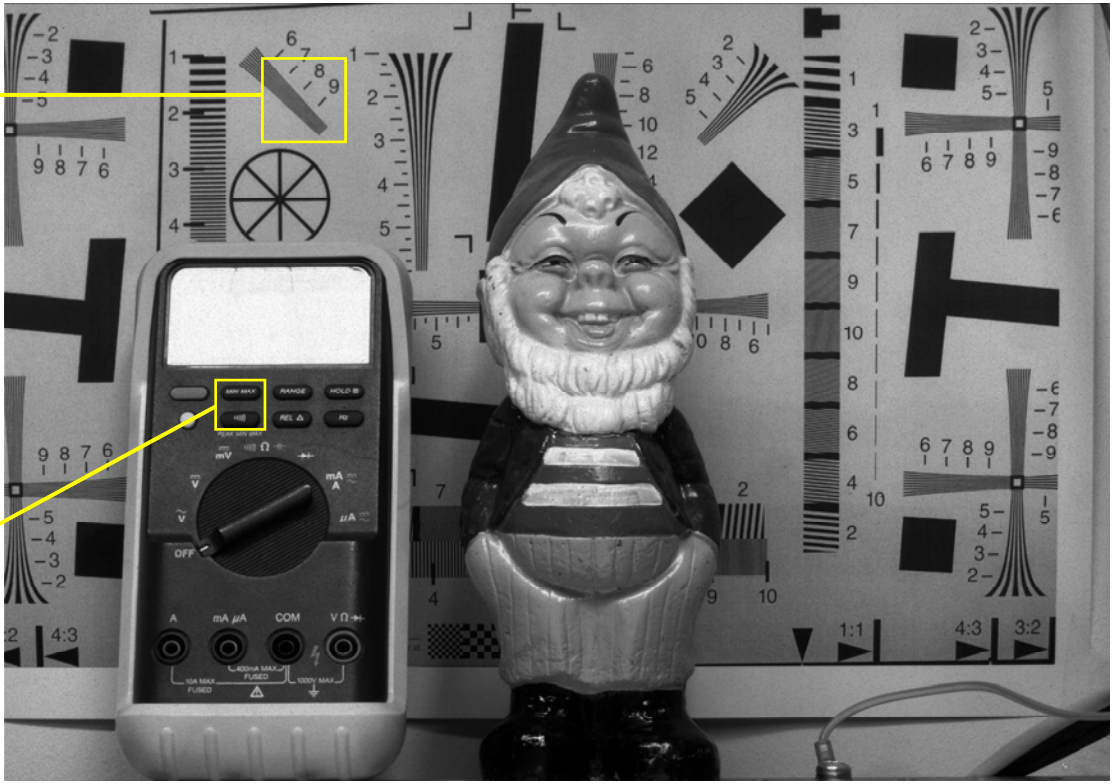
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter



Raw data



Raw data



Early test image 4kx3k pixels with JPEG compression for display purposes

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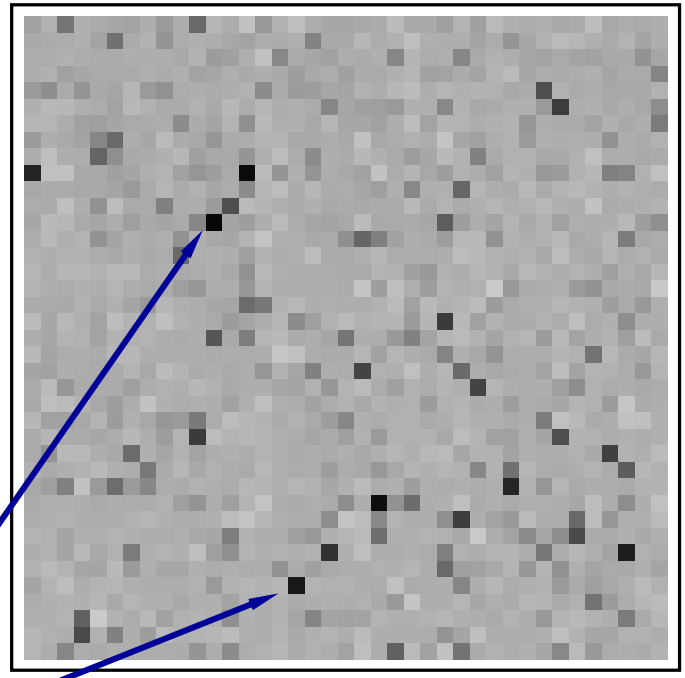
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter



Black "spots

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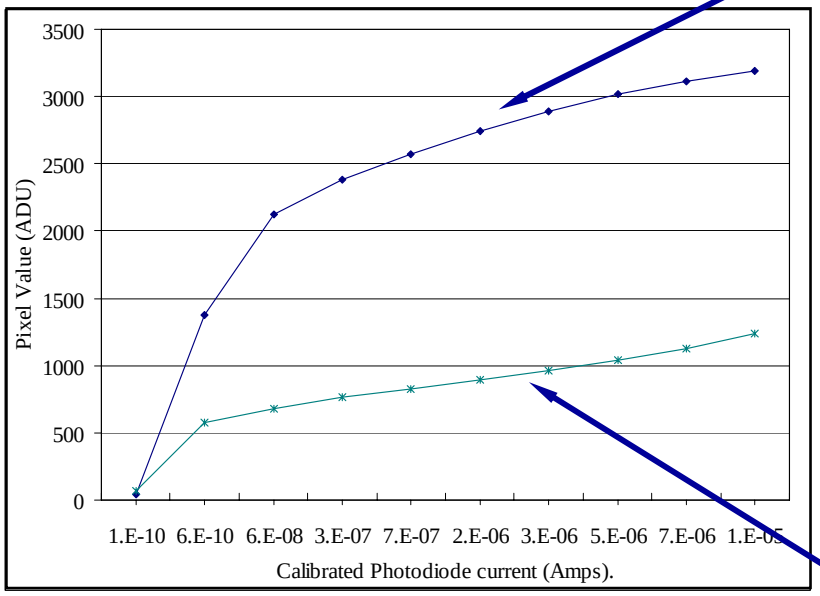
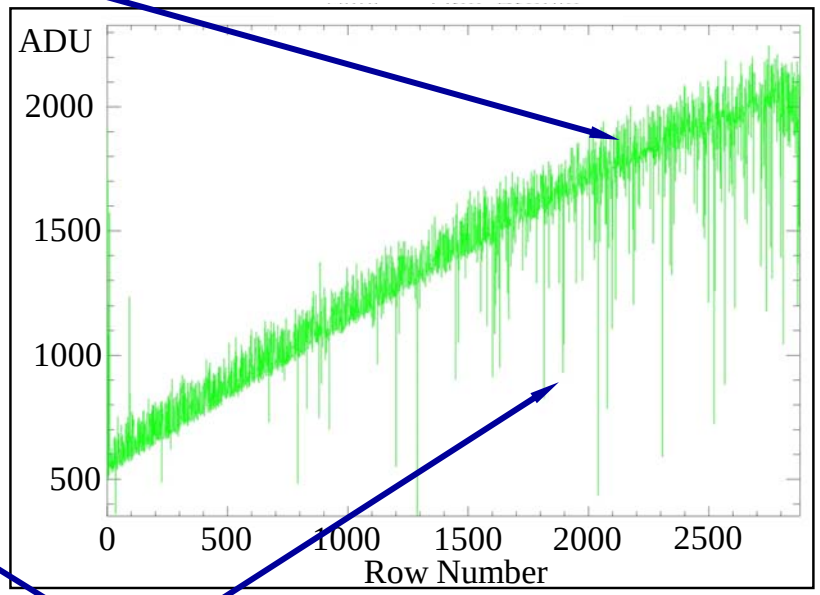
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter

Pixel Responsivity

Normal Pixels





Black "spot" Pixels

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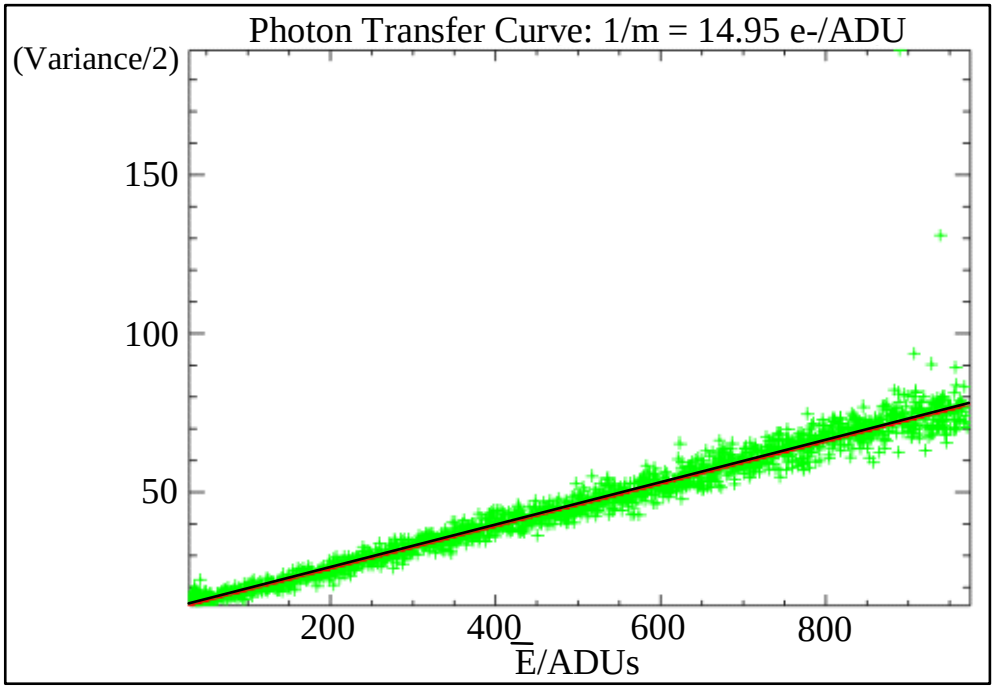
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter



Charge Conversion = 15 electrons/ADU

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4k x 3k Pixel Sensor Development for ESA's Solar Orbiter

Dynamic Range

Useful linear dynamic range	~ 22,500 electrons	**Less than expected because of need to operate the reset voltage at 2.5 V as opposed to 3.3 V.**

Noise

Expected to achieve a noise figure	~ 12 electrons rms,	- assuming CDS cancellation of KTC noise.
Measured Noise:	~ 41 electrons rms.	
	~ 17 electrons rms.	- transfer switch held off throughout.
Off-Chip ADC and Readout System	~ 13 electrons rms	
Just Output Amplifier operating	~ 15 electrons rms.	
With the multiplexer operating	~ 16 electrons rms.	

- It therefore appears that the excess noise arises within the actual pixel.

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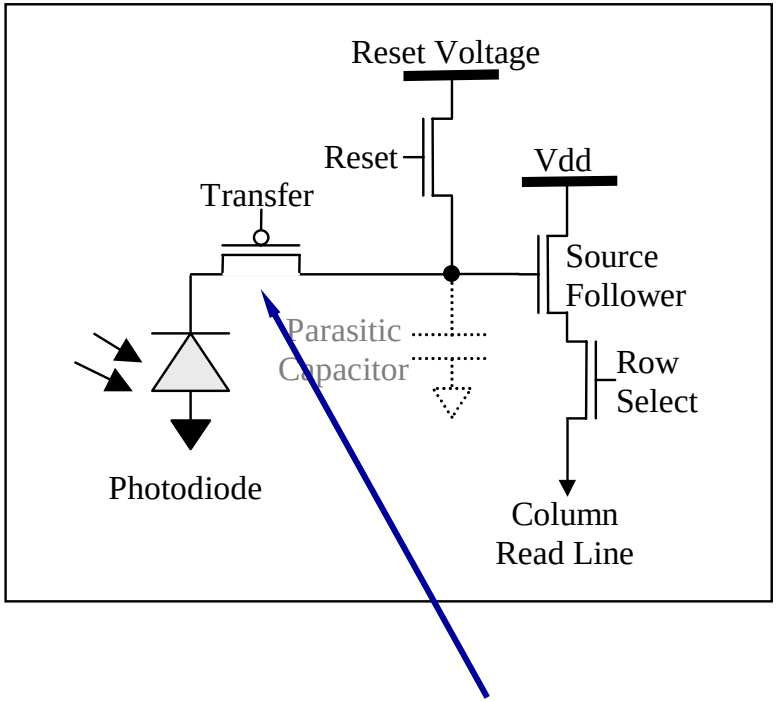
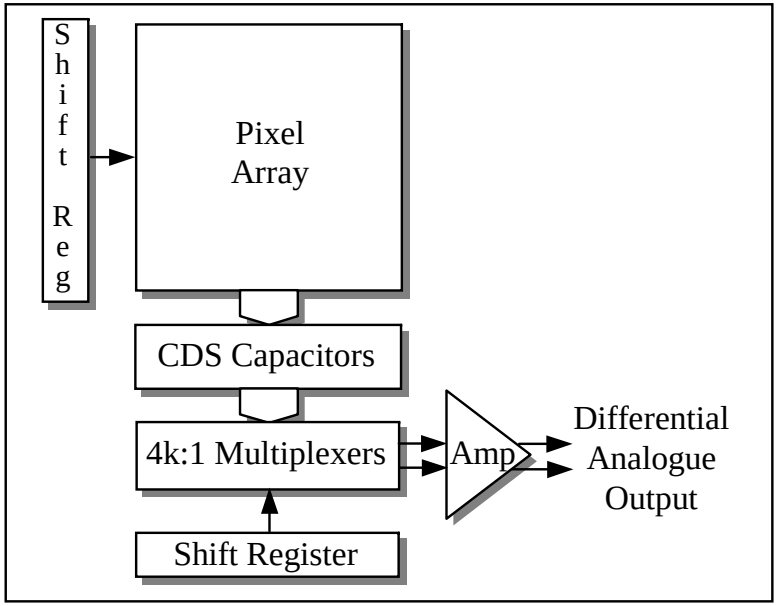
4k x 3k Pixel Sensor Development for ESA's Solar Orbiter





KTC noise "shared" across the total node capacitance

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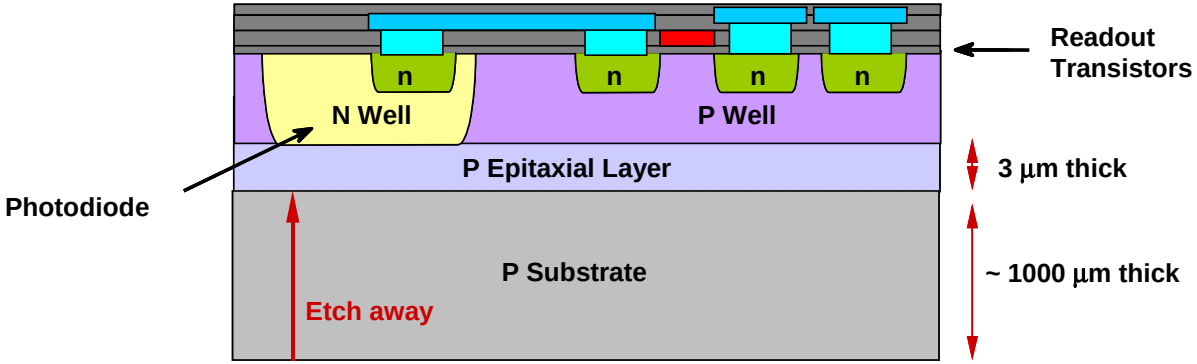
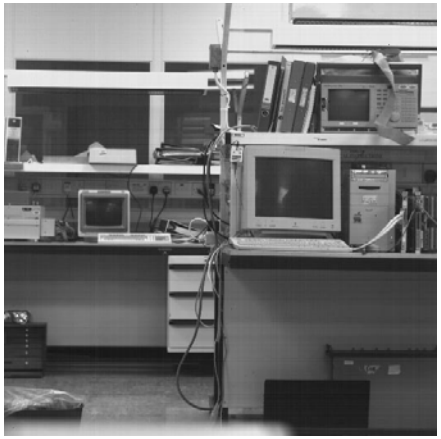
CMOS Thinning Developments with e2v technologies

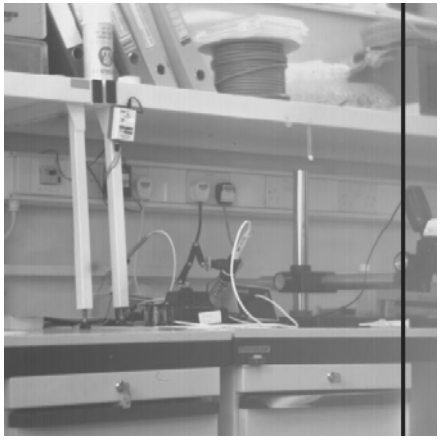
Thinning of 512 x 512 pixel star tracker sensors.

- **Thinned sensors work !**
- **Limited blue response due to difficulty in thinning to the 3 μm epitaxial layer.**





Front-illuminated



Back-illuminated

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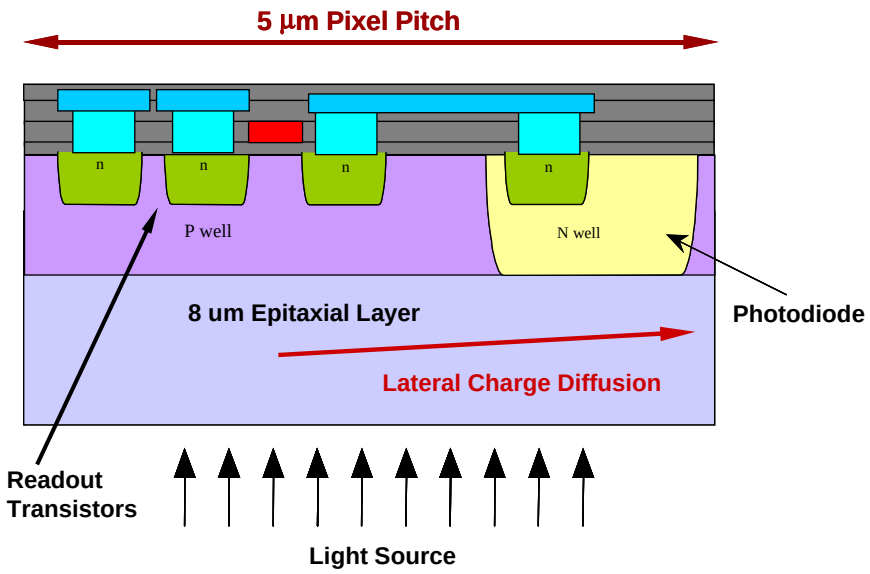
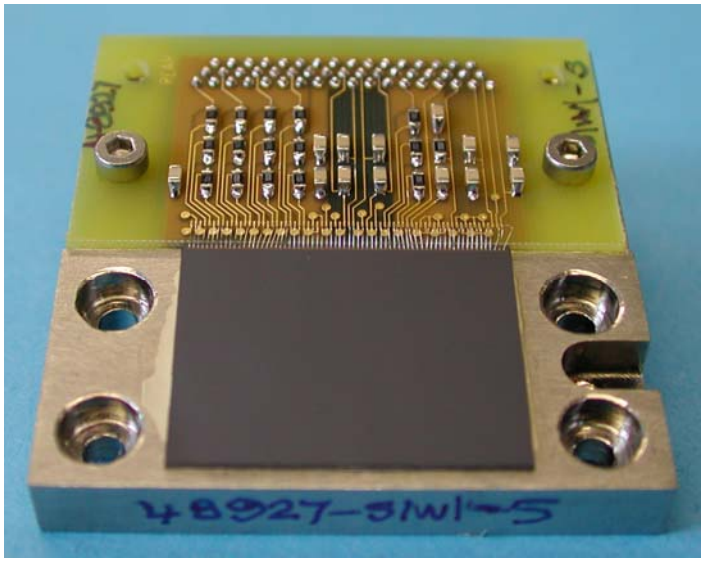
CMOS Thinning Developments with e2v technologies

Thinning of 4kx3k pixel Wafers

- Remove bulk of wafer by diamond turning – allows better etch uniformity later on.
- Etch down into the 8 μm epitaxial layer – actually thinned to ~ 6 μm .
- Characterise EUV responsivity and MTF performance.





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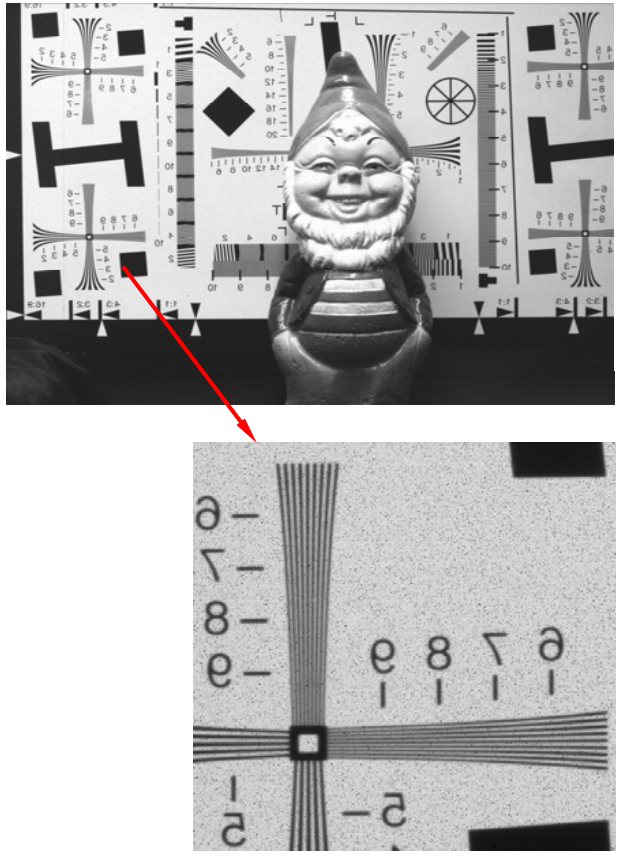
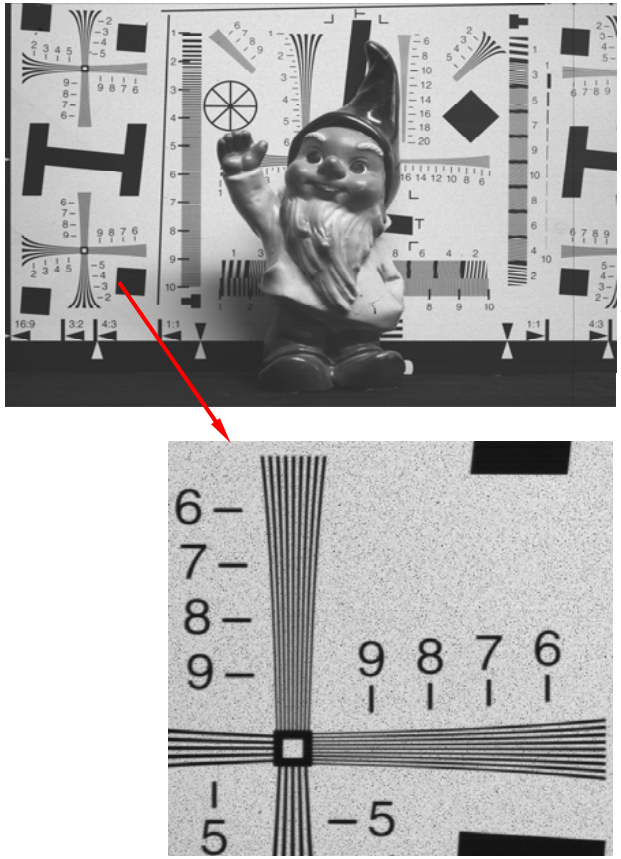
CMOS Thinning Developments with e2v technologies

Front-illuminated



Back-illuminated



Back-illuminated image was taken through a 50nm filter at 350nm with IR-blocking filter.

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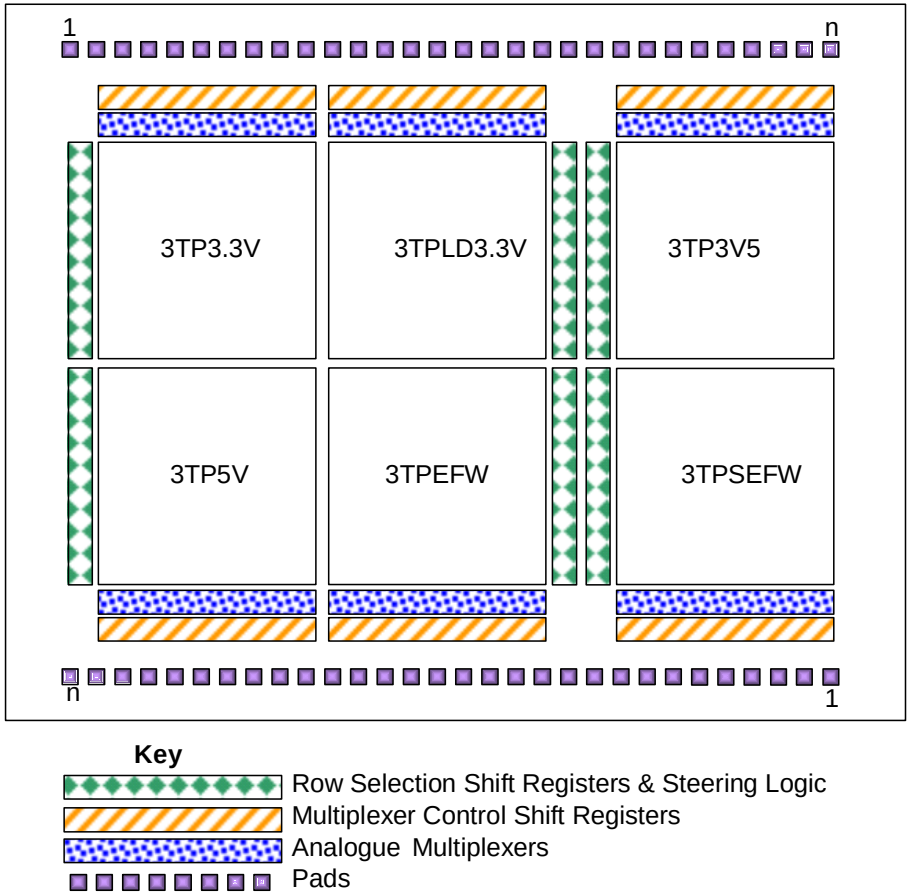
New Test Structures

- 6 arrays of 512 x 512 pixels.
- 10 µm pixel size.
- Varying 3T pixel designs.
- Optimised Signal to Noise.
- Soft-reset for lower kTC.
- Maximise dynamic range.
- Thinning for EUV sensitivity.



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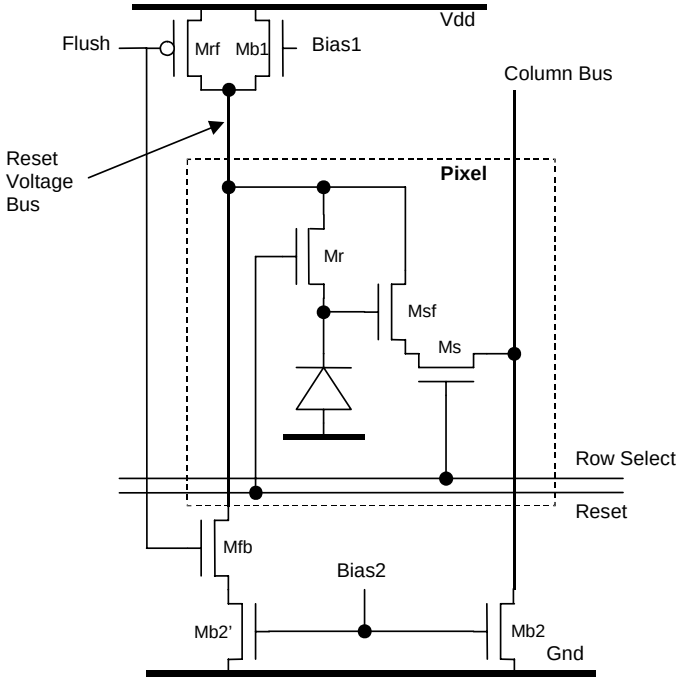
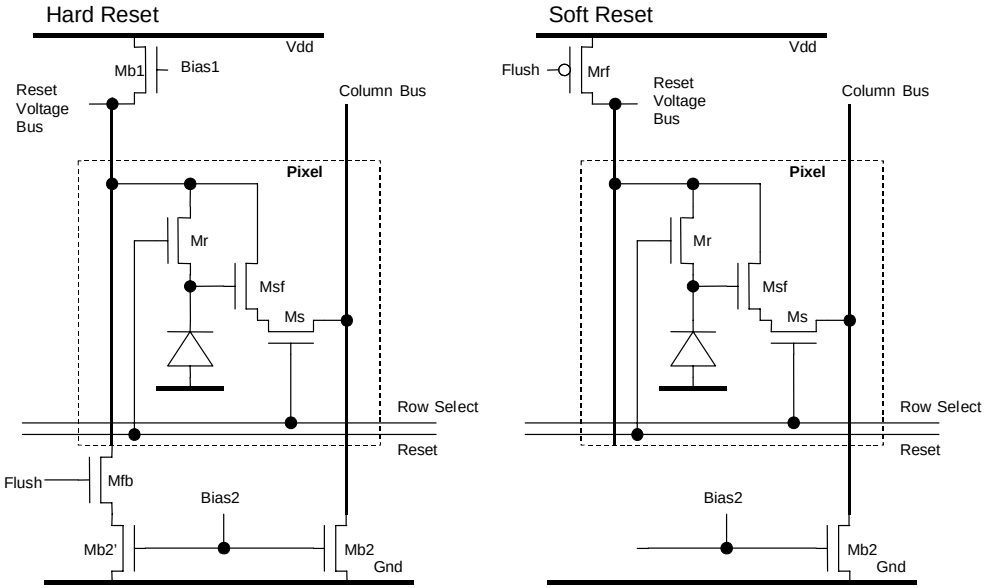
New Test Structures - Pixel Types

Pixel Name	Photodiode capacitance	Main Features
3TP3.3V	5 fF	Simple 3-transistor pixel designed for minimal capacitance and thus minimum kTC noise.
3TPLD3.3V	10 fF	Same as 3TP3.3V but optimized with larger capacitance for greater well capacity.
3TP3V5	5 fF	3.3 V and 5 V mixed voltage version of 3TP3.3V
3TP5V	5 fF	All 5 V version of 3TP3.3V.
3TPEFW	20 fF	Enhanced full-well version of 3TP3.3V with an added capacitor to maximize well capacity.
3TPSEFW	7 - 24 fF	Switchable version of 3TPEFW to allow selectable photodiode capacitance and hence well capacity.

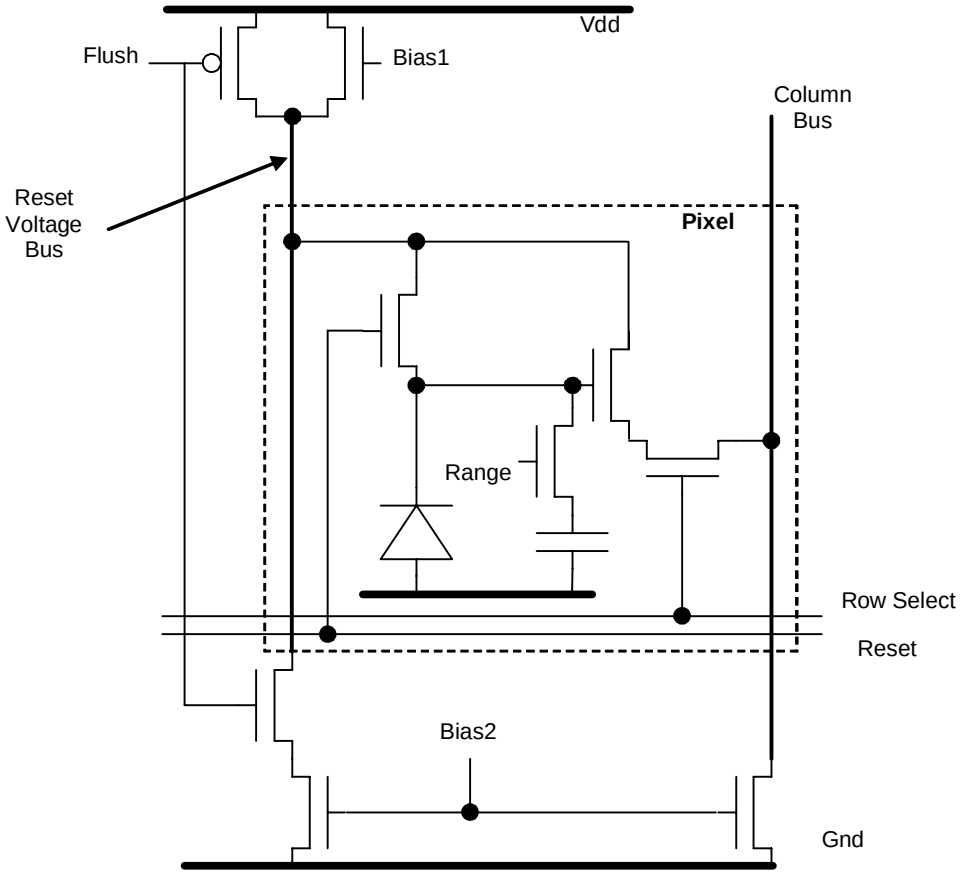
New Test Structures - Soft Reset Operation



From:
Pain, B., Yang, G. Cunningham, T.J., Wrigley, C. and Hancock, H.
An enhanced-performance CMOS imager with a flushed-reset photodiode pixel.
IEEE Transactions on Electron Devices, Vol. 50, No. 1, (2003), 48-56.



New Test Structures - Switched Capacitance Pixel



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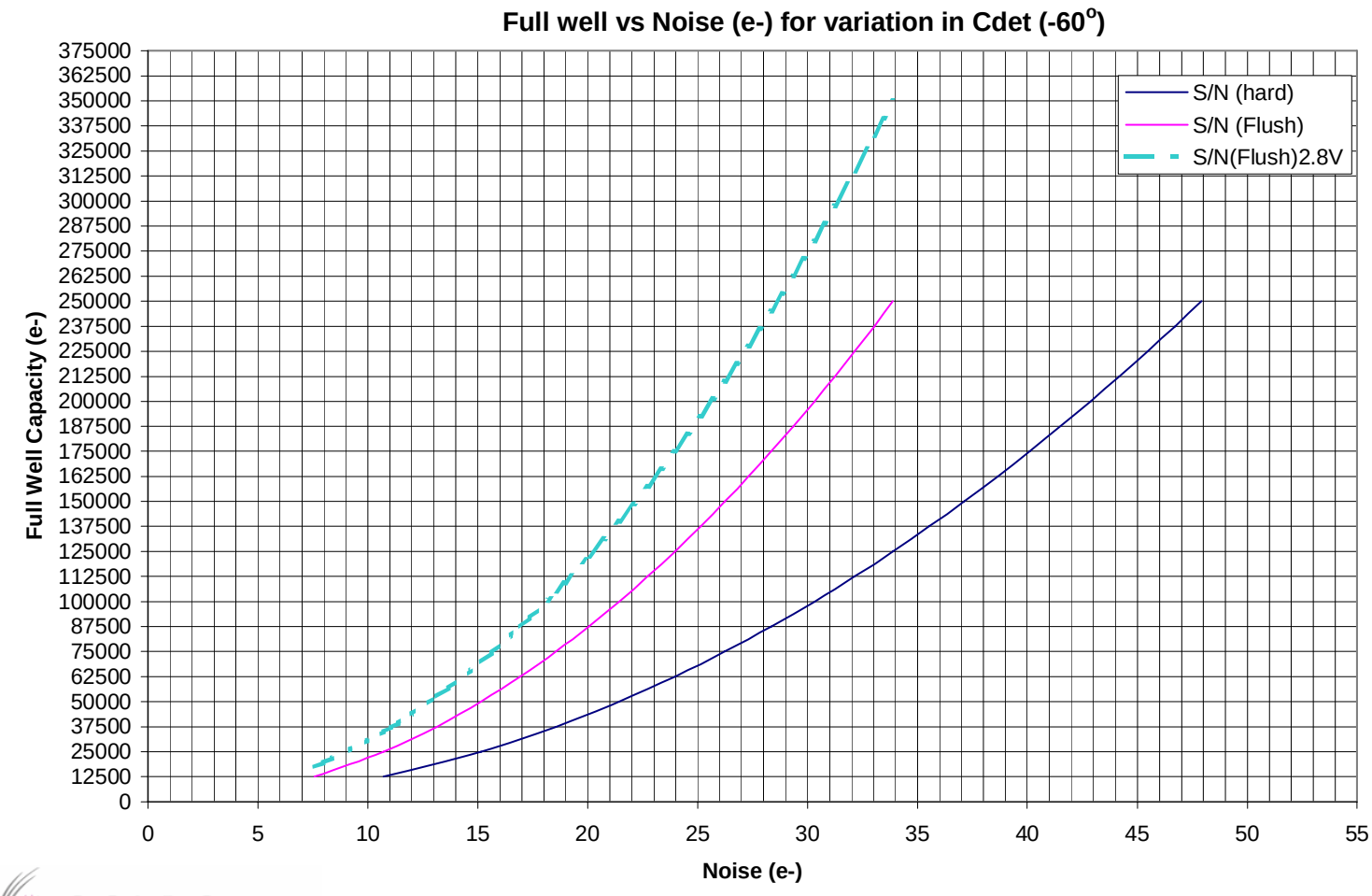
New Test Structures – Full Well vs Noise



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Future Programme

- Further evaluation of more back-thinned 3Kx4K for EUV sensitivity & MTF.
  - e2v technologies are optimising the thinning process.
- Evaluate test structures for Solar Orbiter pixels
  - Confirm improved noise & dynamic range.
  - Determine optimal pixel for the Solar Orbiter application.
  - Radiation testing - total dose and single-event latch-up.
- Design/build/test full-sized prototype of a Solar Orbiter detector.

Summary

- Demonstrated a working large format 4k x 3k pixel CMOS sensor.
- Further work needed to obtain necessary performance.
- Demonstrated the feasibility of back-thinning CMOS image sensors.
- Demonstrated a working back-thinned large format CMOS sensor.

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