MSSL

High-stability multi-CCD Focal Plane for ESA imaging missions

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Overview

- Extra-solar planet detection

- Eddington mission

- Demonstration focal plane for Eddington:-
    CCDs
    Electronics, analogue and digital

- Test system

- Results: Noise, linearity, crosstalk etc.

- RAL ASIC ADC tests:-
    - Characterisation: INL, DNL etc.
    - Radiation testing, TID, SEE

- Gaia mission, radial velocity spectrometer

- Conclusions – no time left

Extra-solar planet detection

- Spectral: Doppler

- Astrometric

- Gravitational lensing

- Transit: e.g. Eddington (ESA),
    Kepler (NASA)
    HD 209458
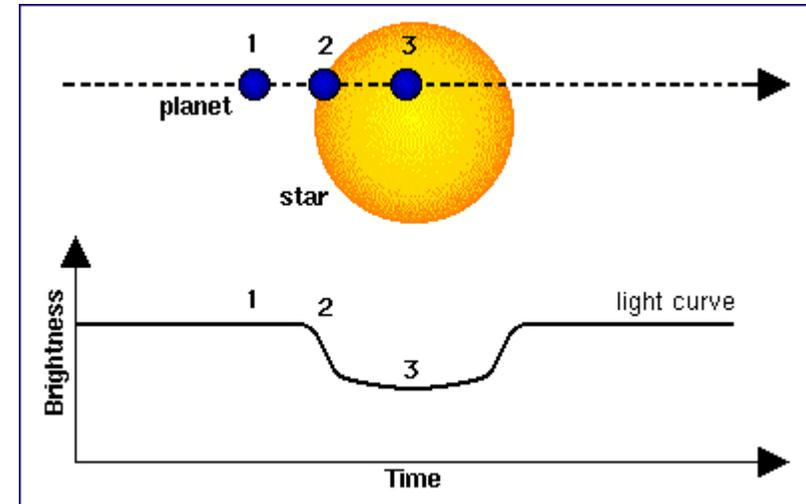
- Direct imaging

- Doppler isolation (planet light)

- Polarisation (planet light)

- Nulling interferometry

Habitable planet transits

- ~0.5% systems aligned

- Duration: few hours

- Period: ~1 year

- Dimming ~1 in 10^4

Eddington mission, R.I.P.

- Aims:

    Planet-finding, ~500K stars

    Asteroseismology, ~50K stars

- L2 Lagrangian point

- 3 or 4 telescopes, each with a 38Mpixel
    focal plane

- FOV ~3°

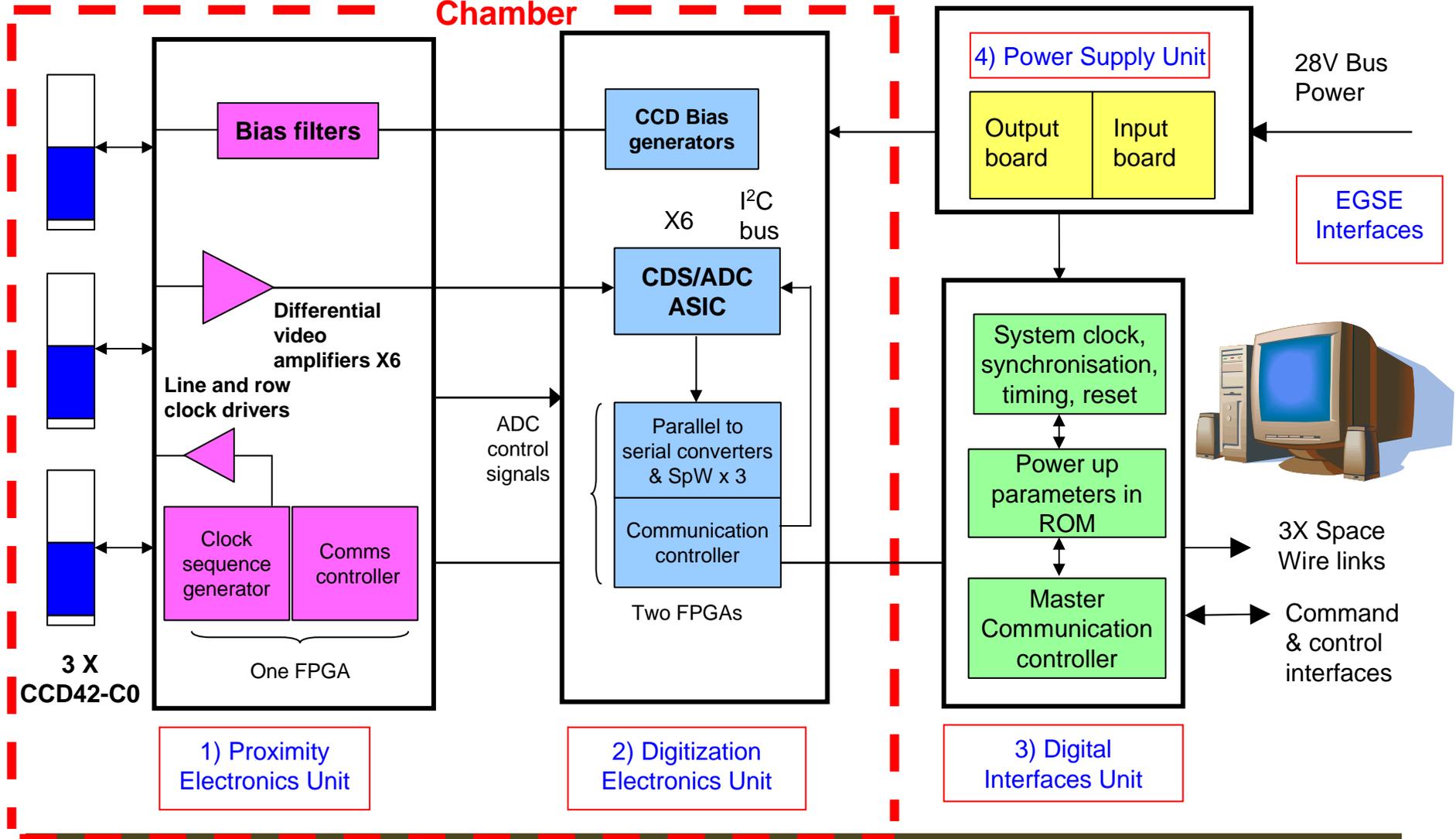- Expected to find a few habitable planets,

    thousands of larger planets

Eddington Demo FPA: Aims

- Flight-representative system for a half Eddington focal plane
  (each half independent for redundancy). 1.2Mpix/s per port, 6 ports

- Also usable for Gaia-RVS focal plane tests.

- EGSE to read and store all data in realtime.
  Chose Spacewire for ESA compatibility:
  Transmitter - VHDL core in Actel Pro-ASIC in-system-programmable FPGA,
  this limited the readout rate to 1.2Mpix/s per port with 6 ports.
  Receiver – Star Dundee PCI-2 card, capable of running at
  ~2.4Mpix/s per port (~240Mbit/s).

- Investigate readout noise, temperature stability around -120C, crosstalk etc.

- RAL ADC ASICs: Characterise (e.g. INL, DNL) and perform radiation tests.

Eddington Demo FPA)

Inside Chamber

**4) Power Supply Unit**

28V Bus Power

| Output board | Input board |

EGSE Interfaces

Bias filters

CCD Bias generators

I^2C bus

X6

CDS/ADC ASIC

System clock, synchronisation, timing, reset

Power up parameters in ROM

Master Communication controller

Differential video amplifiers X6

Line and row clock drivers

ADC control signals

Parallel to serial converters & SpW x 3

Communication controller

3X Space Wire links

Command & control interfaces

Clock sequence generator

Comms controller

Two FPGAs

One FPGA

3 X CCD42-C0

1) Proximity Electronics Unit

2) Digitization Electronics Unit

3) Digital Interfaces Unit

PSD7   Liverpool Sep/05   Dave Walton

Demo FPA physical layout

LN2 Dewar

Cold finger

Temperature control, monitoring & logging

Base plate

Chamber Window

Douglas vacuum feedthrus

Optical mask

Optical bench and light source

Thermal baffles

To FPA EGSE

CFPA (CCDs)

Proximity Electronics Unit

Digitising Electronics Unit

Power Conditioning Unit

Digital Interfaces Unit

⚜UCL

e2v CCD42-C0

- Provided by ESA
- Frame transfer
- Thinned, back-illuminated
- 3 side buttable package
- 2k X (3k + 3k) pixels
- 13.5µm square
- Image line shift ~96µs
- Storage line shift ~20µs
  - fastest whole image frame transfer = 295ms
- 2 port readout
- Image & store full well $\geq$ 150k e-
- Readout register full well $\geq$ 600k e-

Inside cryostat

DEU

Optical test mask

PEU

Thermal baffles

CCDs

Cold
finger
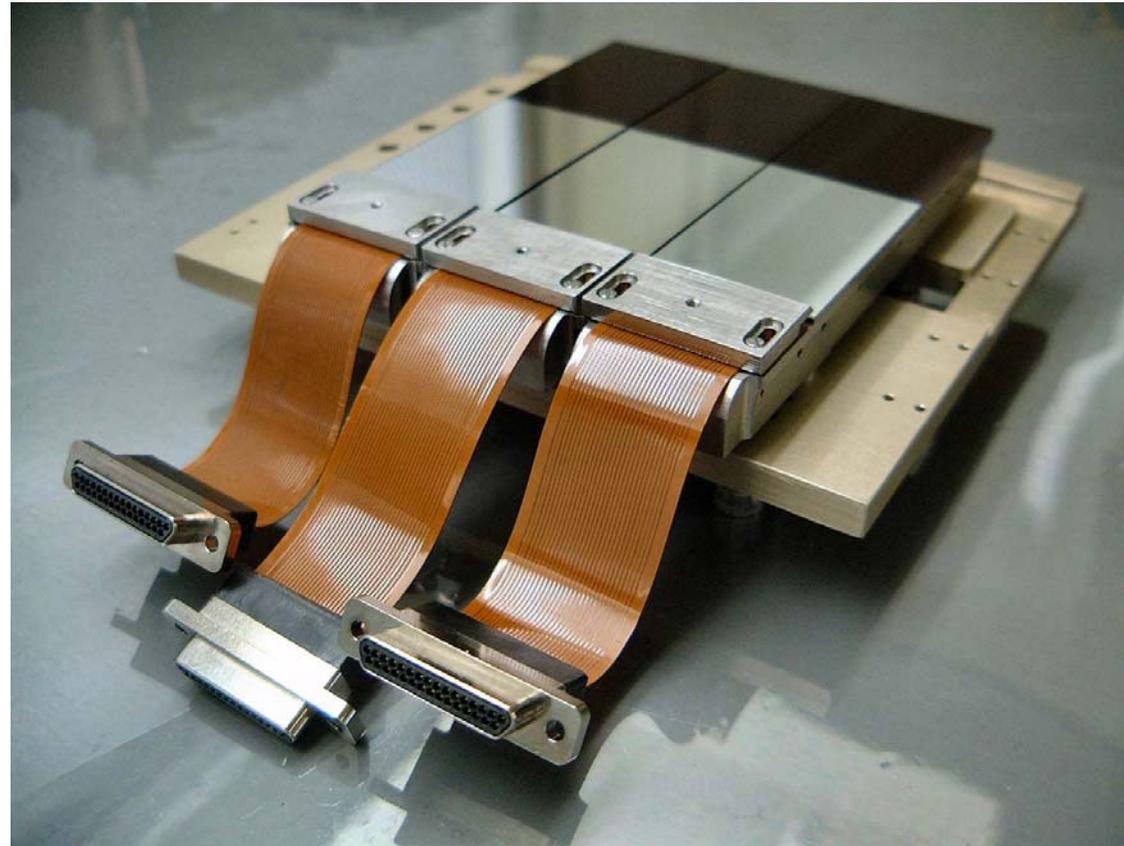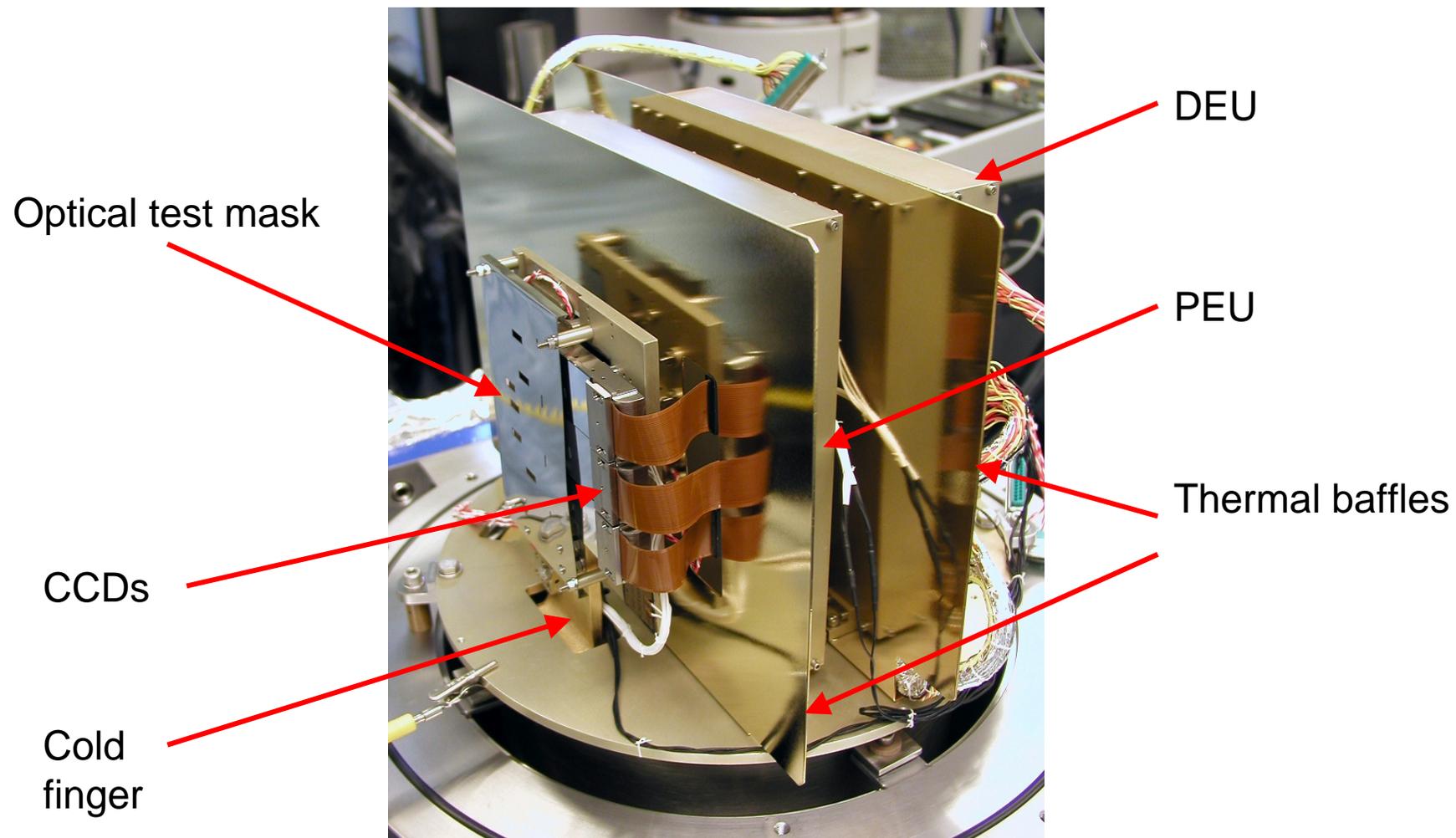
Cryostat with optical bench in MSSL cleanroom
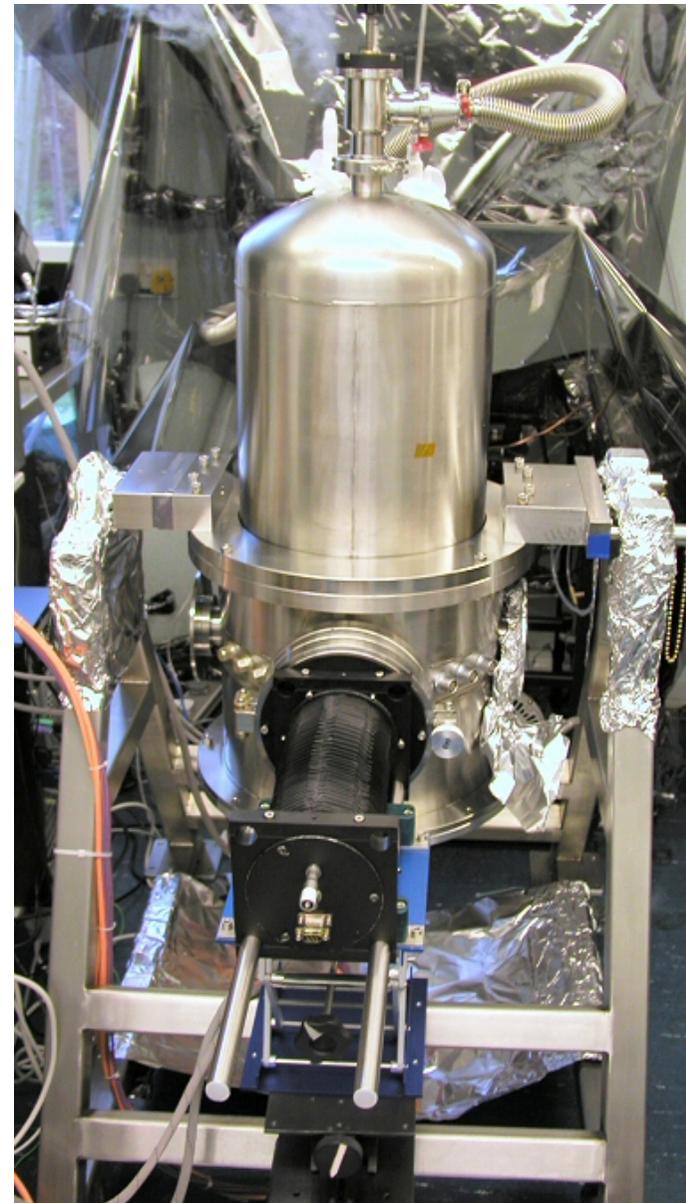
Results at 1.2Mpix/s per port

20k DN signal   10 DN crosstalk =0.05%

• Readout noise: ~60e-, dominated by chamber electrical environment, analogue harness etc. (~17e- seen on bench, ~10e- from CCD/analogue ~13e- from ADC ASIC). Further work needed on grounding etc.

• CCD integral non-linearity ~0.1% over ~80% full-well

PSD7   Liverpool Sep/05   Dave Walton
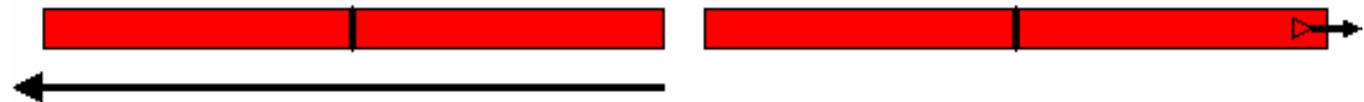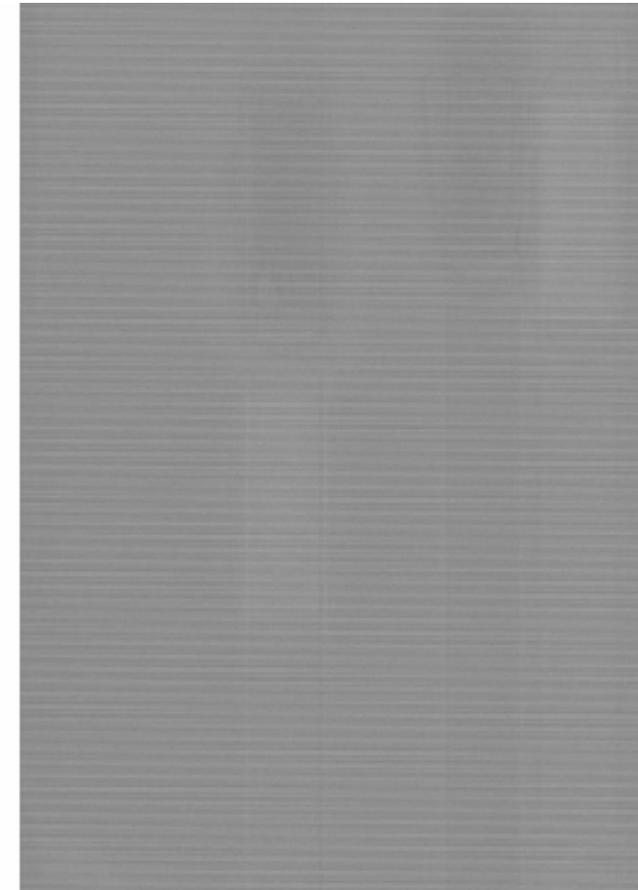
Results: Stability

- We see approx. +/- 6 parts in 10^4

- Likely to be limited by stability of optical bench

- Variations correlate with clean room temperature

37 hours, ~15000x8s integrations

- PEU -10ºC -> +10 ºC, +0.015%/ºC

- DEU -10ºC -> +10 ºC, +0.03%/ºC

- CCDs -120ºC -> -90 ºC +0.04%/ºC
  Two competing effects:
  Output FET gain expected to give -0.1%/ ºC
  CCD QE expected to give +0.05%/ ºC
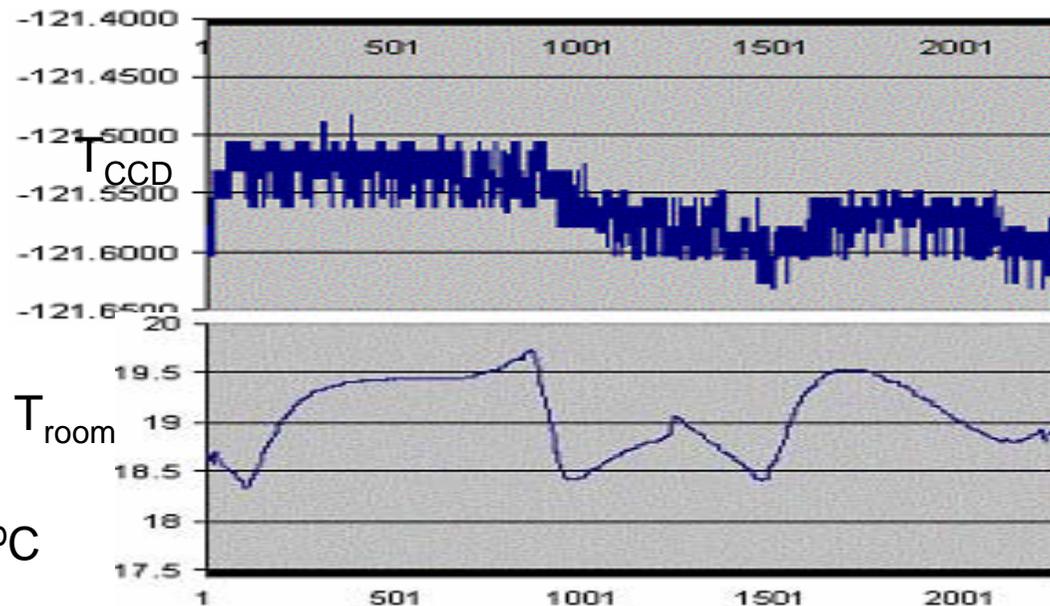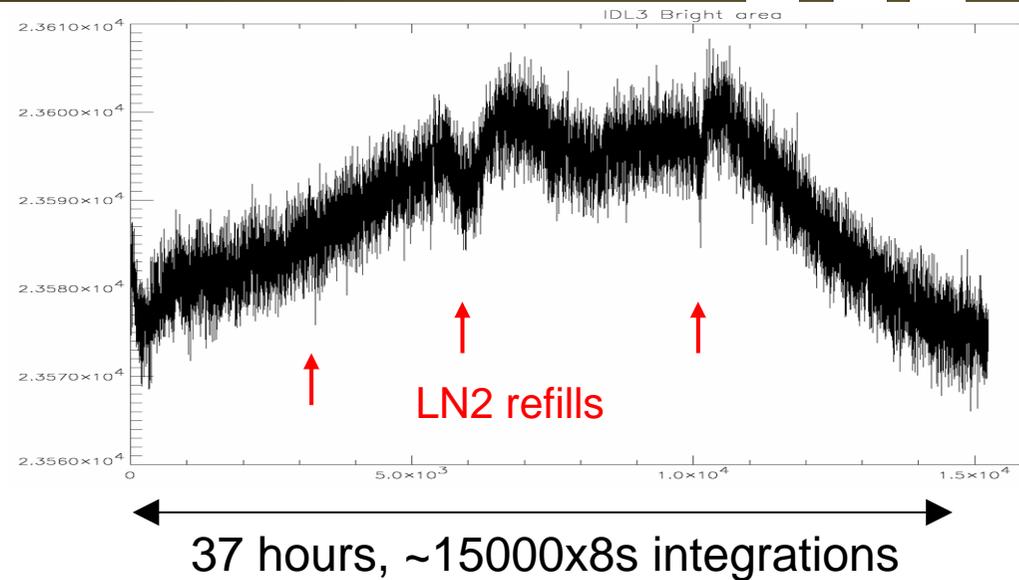
RAL ASIC ADC

CCLRC Space Science and Technology Department   CDS/ADC ASIC

Commercial In Confidence

CCLRC
Rutherford Appleton Laboratory
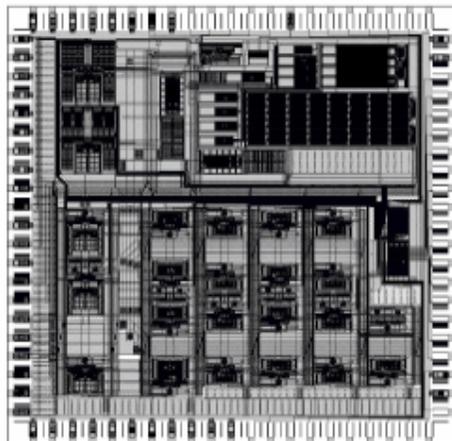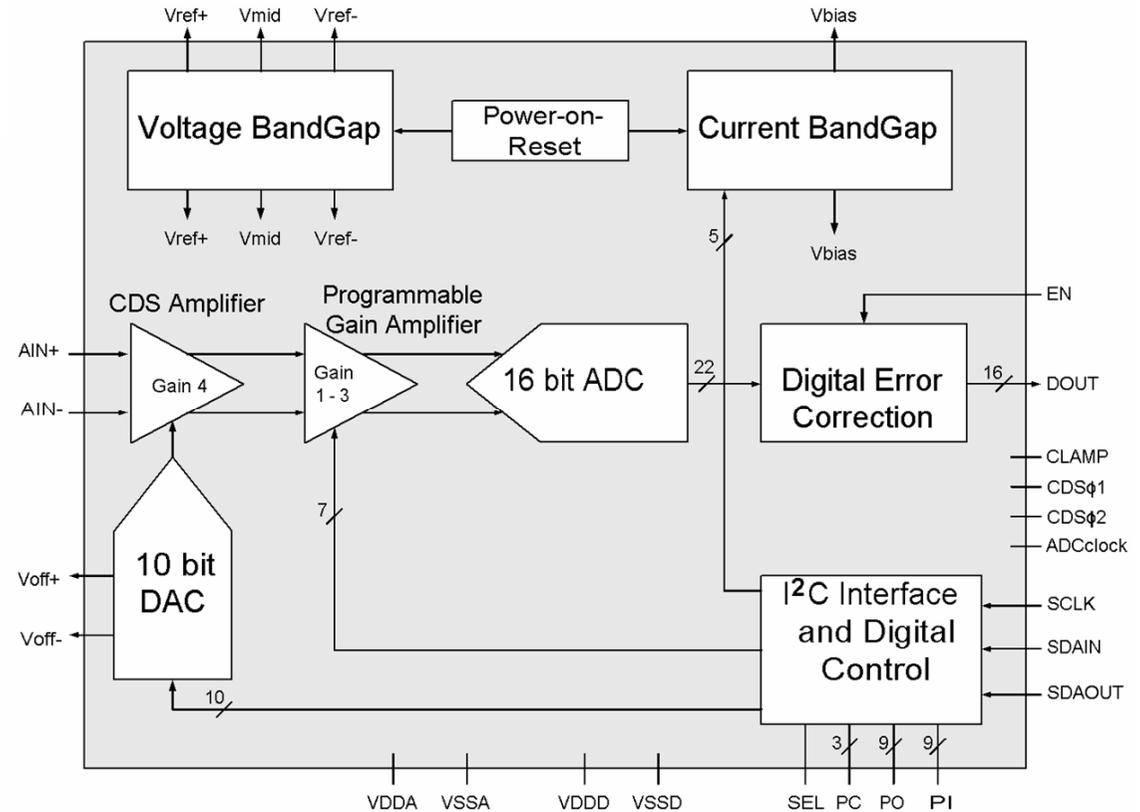
CDS/ADC CCD Video Processing ASIC

Design Description

Version: 3.4

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- Good for > 1MHz pixel rate
- 16 bit ADC architecture
- Mature design after several iterations
- European ASIC fab
- Process known to be good for total dose

Test results on RAL ADC ASIC

- INL, DNL, noise: ADC test system developed using 19bit DAC with in-house analysis software. Results as per RAL predictions, e.g. intrinsic noise ~3.5DN rms.

- TID (performed at ESTEC): The Mk6 RAL CDS/ADC ASIC is deemed to be tolerant to at least 50 krad(Si) TID in view of the strong correlation between pre- and post irradiation measurements.

- Electrical parameters and input-referred noise: little change after 50 krad(Si) TID.

- None of the devices exhibited Missing Codes before or after irradiation, at both 14 and 16-bit data levels.

- SEL (performed at Louvain Heavy Ion Facility): SELs seen above ~14MeV/(mg/cm^2), but suitable for spaceflight with latch-up protection circuitry.

Gaia

- Aim: to measure positions and velocities of ~2.5×10^8 stars in 3-D in order to trace Galactic kinematics and history.

- Radial Velocity Spectrometer has spectral dispersion, hence v. low signal levels per pixel. To compensate for this, intention is to use e2v L3CCDs.
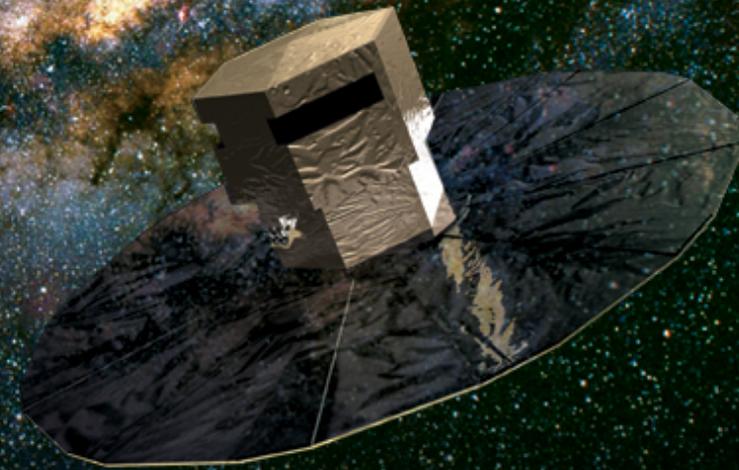
L3CCDs
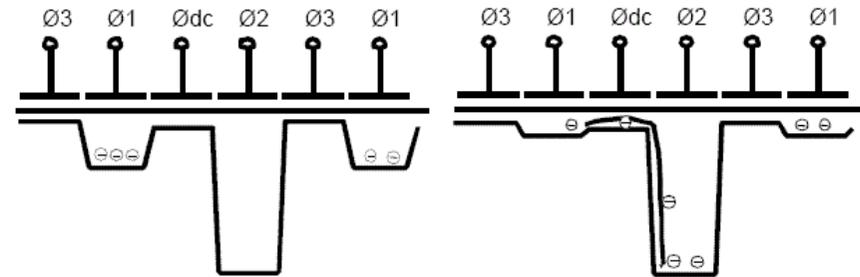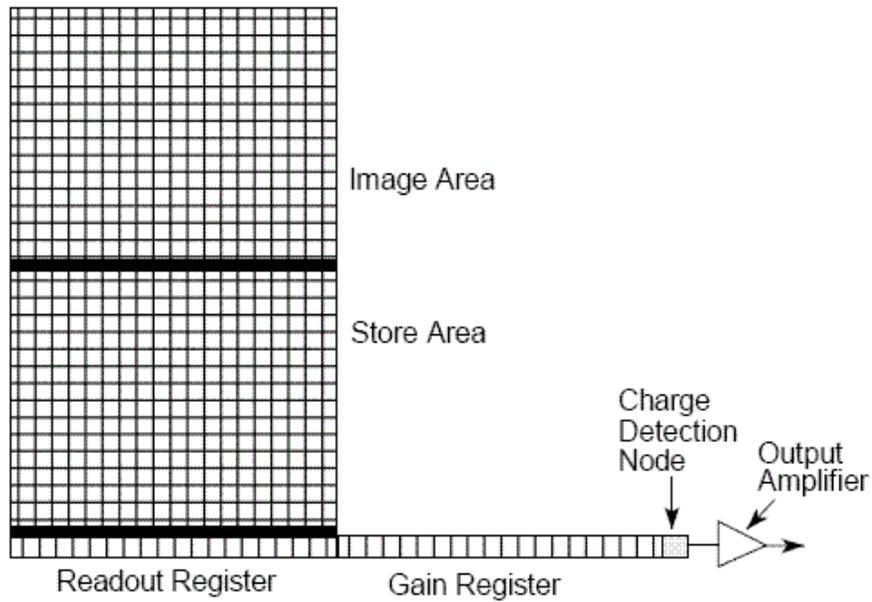
Acknowledgments

ESA for contract, CCDs

RAL for ADC ASIC assistance

U. Dundee / Star Dundee for spacewire assistance

Future work

Using the system for Gaia-RVS work

"Son of Eddington"

"Super-WASP in space"