Electronics Issues

for sLHC Tracking Detectors

- **Noise, Threshold**
- **Signal**
- **Signal/Threshold**
- **Electronics Tidbits**

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Quiz Question # 1: who wrote the following sentence

E debbasi considerare, come non e cosa piu difficile a trattare, ne piu dubia a riuscire, ne piu periculosa a maneggiare, che farsi capo a introdurre nuovi ordini.

It must be considered that there is nothing more difficult to carry out, nor more doubtful of success, nor more dangerous to handle, than to initiate a new order of things.

Answer:

Niccolo Machiavelli: IL PRINCIPE

Noise, Threshold setting

Signal-to-noise ratio S/N is essential for performance of the tracking system.

RMS noise σ [electrons]

depends on shaping time and size (i.e. C, i) of the detector channel

Threshold Thr

need to suppress false hits Thr = n* σ + threshold dispersion δThr

SCT: $\sigma \approx 600+C*40 \approx 1500e^-$, n = 4 —> Thr ≈ 6,000$e^-$

Pixels: $\sigma = 260e^-$, $\delta Thr = 40\ e^-$ n = 5 —> Thr ≈ 1,300e^-

BUT Pixel Threshold ≈ 2500 – 3000 e^- —> Mixed signal system issue, S/N!

Single-bucket timing is needed, use short shaping times (τ_R= 15ns for sLHC?).
yet there is still a problem with time walk: signal is in time
only if it exceeds the threshold by large amount ("overdrive")
Or: measure pulse height (ToT) and correct timing for pulse height.

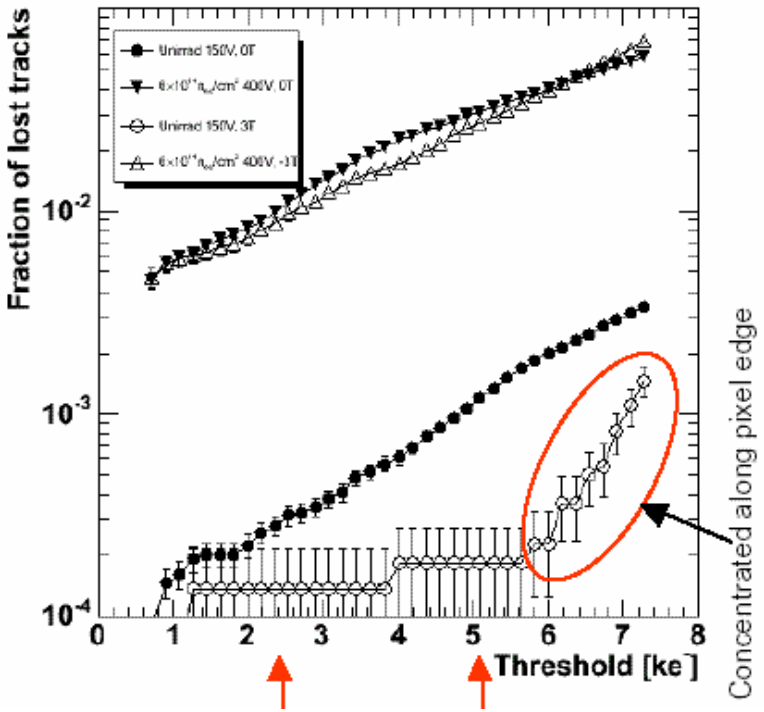
Signal / Threshold S/T : Expected Performance

Efficiency in CMS Pixels

(T. Rohe, RESMDD04)

After radiation damage from a fluence of $6*10^{14}$ n_{eq}/cm^{-2}, inefficiency vs. the signal-to-threshold ratio S/T:

S/T	Inefficiency [%]
6	1
4	2
3	3
2	9



Efficiency in Pixels

(depends on B-field, pixel size etc, but serves as a guide even for larger fluences):

Need S/T > 4 - 5

sATLAS Tracker Regions: Predicted Threshold

Integrated Luminosity
(radiation damage) dictates the detector technology

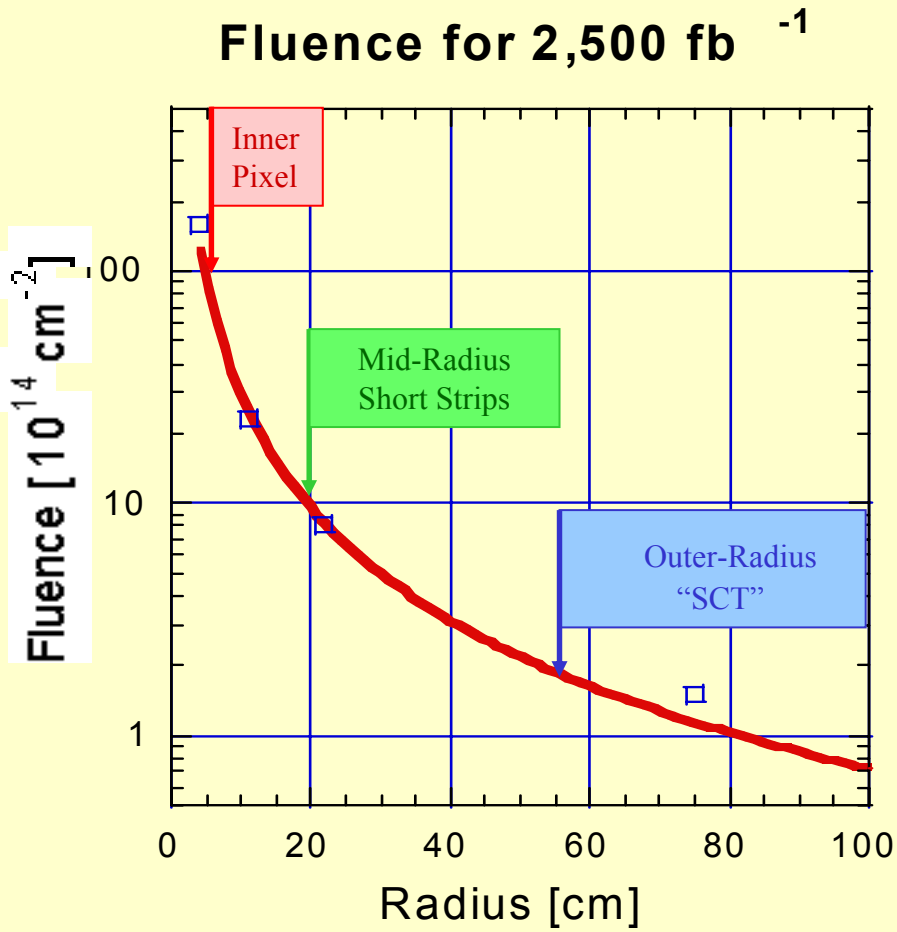
Instantaneous rate
(particle flux) dictates the detector geometry

Straw-man layout:

Inner: **6 cm ≤ r ≤ 12 cm**
pixels style readout
Threshold = 2.5 ke⁻ > 2.0ke⁻ ?

Middle: **20 cm ≤ r ≤ 55 cm**
short strips
Threshold = 4400 e⁻ (0.7 fC)

Outer: **55 cm ≤ r ≤ 1 m**
"long strips"
Threshold = 6250 e⁻ (1.0 fC)



Detailed sCMS Pixels (R. Horisberger)

Summary

- Propose 3 Pixel Systems that are adapted to fluence/rate and cost levels

- Pixel #1 max. fluence system ~400 SFr/cm^2

  100 μ * 150 μ

- Pixel #2 large pixel system ~100 SFr/cm^2

  160 μ * 650μ

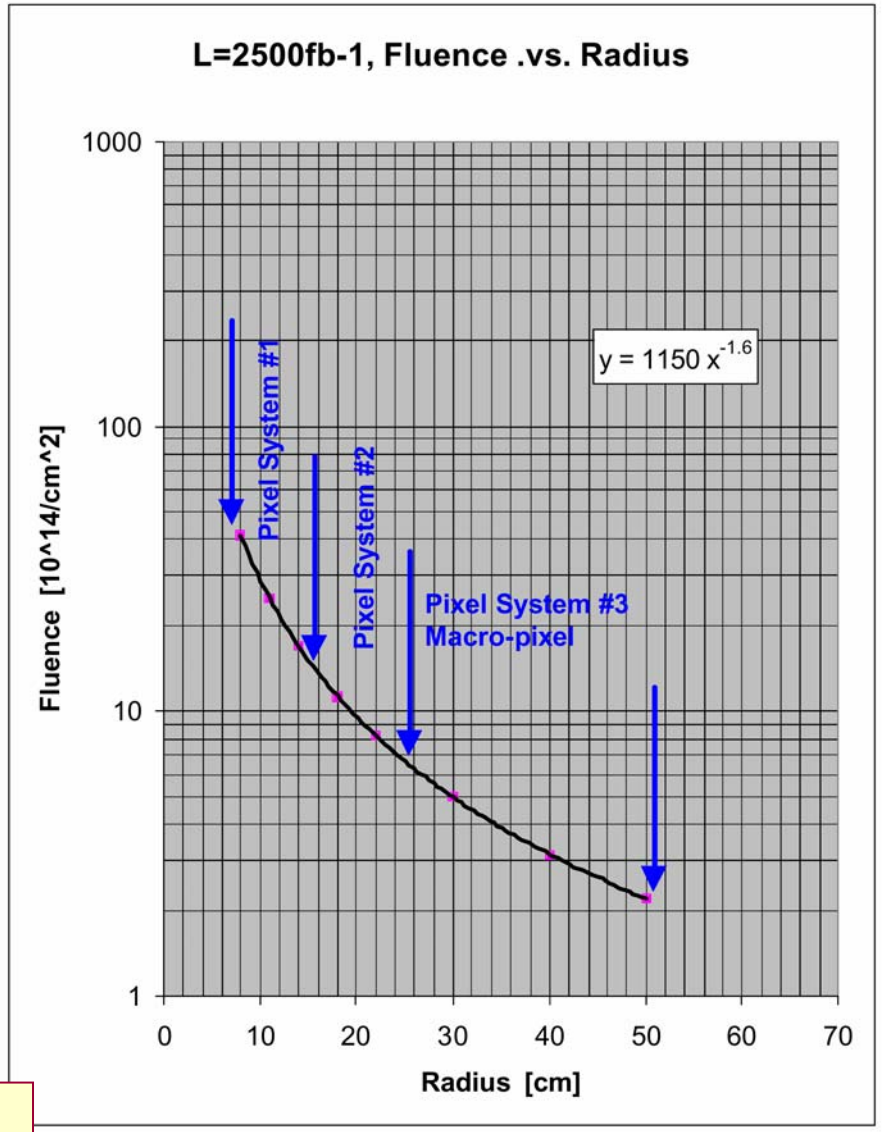
- Pixel #3 large area system Macro-pixel ~40 SFr/cm^2

  200 μ * 5000 μ

- 8 Layer pixel system can eventually deal with 1200 tracks per unit pseudo – rapidity

- Use cost control and cheap design considerations from very beginning.

- Can this be done for 2012/13 ????



CMS: Inside out: "Fat" pixels, strips
ATLAS Outside in: "Skinny" strips, pixels

Detector Materials for Pixels for R ≈ 5 cm

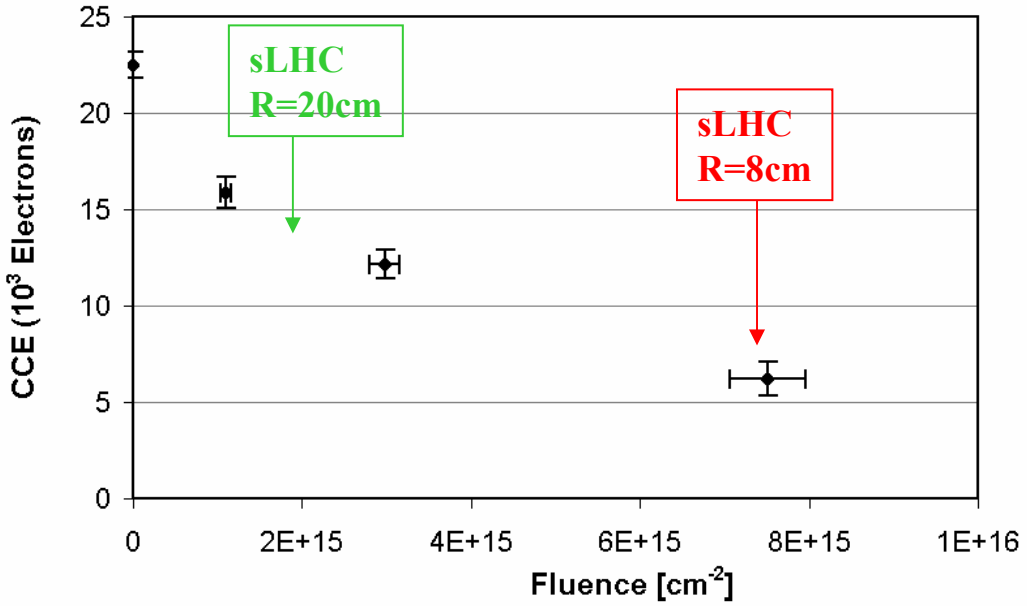
Results from **RD39, RD42, RD50, …**

Material		Collected Signal [e^-]		Issues
		Pre-Rad	$10^{16}cm^{-2}$	
Si	~ RT	24,000	~ 2,500	Depletion, Trapping, n-on-p ?
Si -75µm	Epi	6,000	~ 2,000	Small signal at intermediate fluences
Si	Cryo	24,000	?	Cryo Engineering
Si	3-D	24,000	~ 10,000	Efficiency "Holes"?
SiC	Epi	2,000	~ 0	Trapping? Slow collection Cost of wafers
Diamond	Poly	8,000	< 3,000 ?	Trapping ? Cost of wafers
Diamond	Single X-tal	12,000	"Same as Poly ?"	Trapping ? Cost of wafers

Charged Trapping in Si: the Good News

Efficiency of Charge Collection in 280 um thick p-type SSD

G. Casse et al., (RD50): After 7.5 *10^{15} p/cm^2, charge collected is > 6,500 e$^-$



Trapping Time is factor 2 longer than extrapolated from previous measurements (Krasel et al.)

No adverse effects of anti- annealing observed! (P.P. Alport, 2004 IEEE)

Charge collection in Planar Silicon Detectors might be sufficient for all but inner-most Pixel layer?

For 3-D after 1 *10^{16} n/cm^2, predicted charge collected is 11,000 e$^-$

Signal / Threshold S/T : Expected Performance

Efficiency in CMS Pixels **(T. Rohe, RESMDD04)**

Need S/T > 4 - 5

S/T	Inefficiency [%]
6	1
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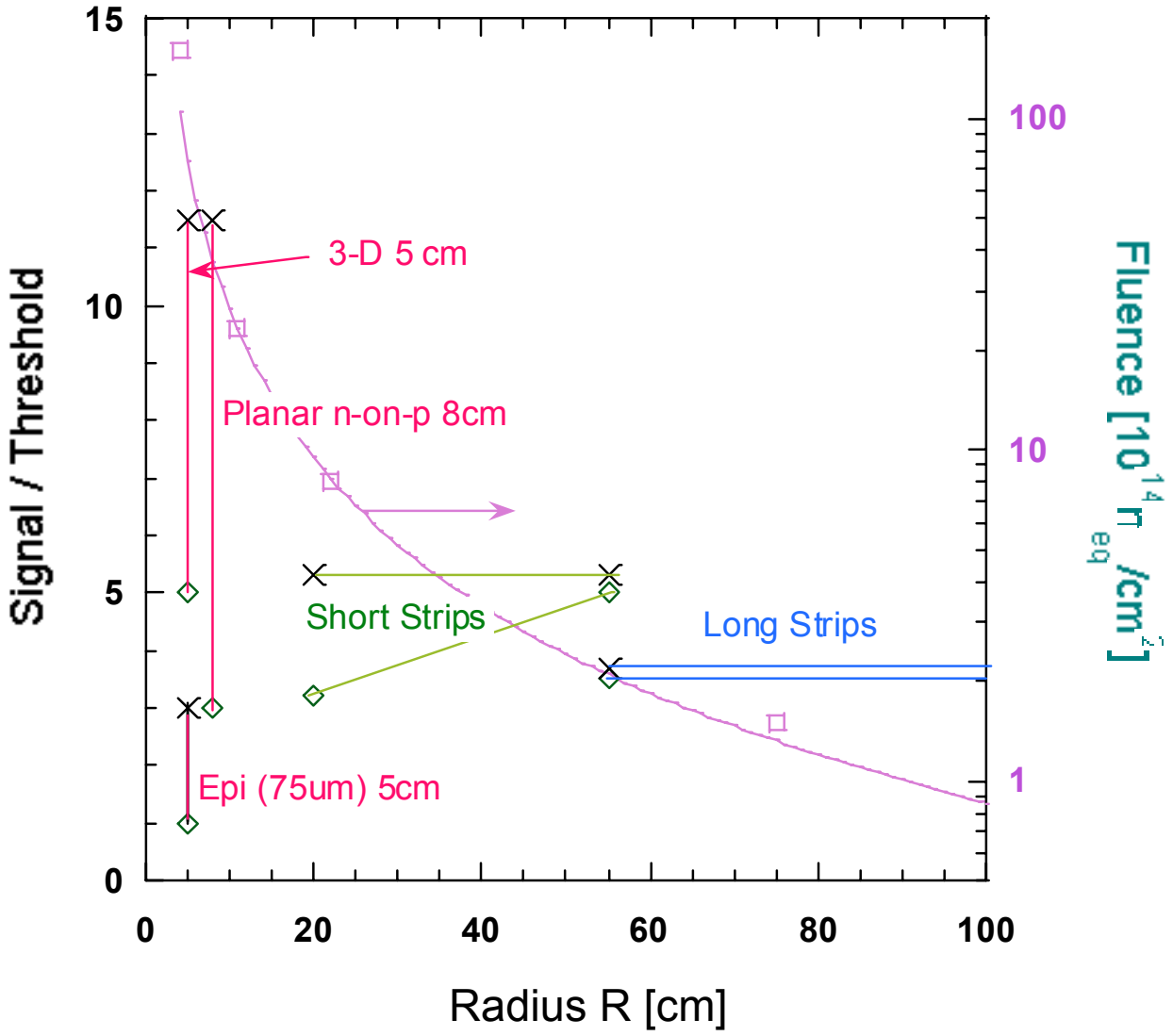
Radius [cm]	**Detector**	**Threshold [e^-]**	**Signal / Threshold**			**Comment**
			Pre-Rad	After 1250 fb^{-1}	After 2500 fb^{-1}	
> 55	Long strips	6250	3.7	3.7	3.7	~ SCT n-on-p
20 - 55	Short strips	4400	5.3	3.9	3.2	n-on-p
8 cm	Thick Pixel	2000	11.5	5.5	3.0	n-on-p
5 cm	Thin Pixel	2000	3.0	1.5	1.0	Epi 75 µm
5 cm	3-D	2000	11.5	7.5	5.0	100 µm cells

Signal / Threshold : Expected Performance



Signal/Threshold

x Pre-rad

◊ Post 2500 fb^{-1}

2nd CMS Workshop on Upgrades for SLHC (P. Sharp)

Conclusions from the 1rst SLHC Workshop

- CMS Electronics is very Robust, Handles increased rates well
- Pixel and Tracker Upgrades – (RH and GH)
- 8 cms – 15 cms Pixels 1 100 μ * 150 μ (Present System at 8, 11, 14 cms)
- 15 cms – 25 cms Pixels 2 160 μ * 650μ (C4 Bonding, at 18, 22 cms)
- 25 cms – 50 cms Pixels 3 200 μ * 5000 μ (at 30. 40, 50 cms)
- 50 cms - Silicon Strips (Rationalize Module Types)
- R&D E1: Review Electronics Systems for Level 1 trigger
- How will Tracker interface to: Calorimeters and μ Systems ?

2nd CMS Workshop on Upgrades for SLHC (P.Sharp)

Conclusions from the 1rst SLHC Workshop

- The Tracker upgrade will require access to DSM Electronics
- Will need to Characterize the 130 nm Processes
- Will need to Characterize < 130 nm Processes (Propose 65 nm)

- R&D E2: Continue to Develop Relationship with DSM Vendors and obtain access to Design Tools to continue to optimize the use of DSM processes in Particle Physics
- Cost : Must get design right in < 2 Iterations
  Must use > 100,000 chips / Design
  Then Cost / Chip is no worse than 250 nm

F.E.E. Technologies for sLHC:

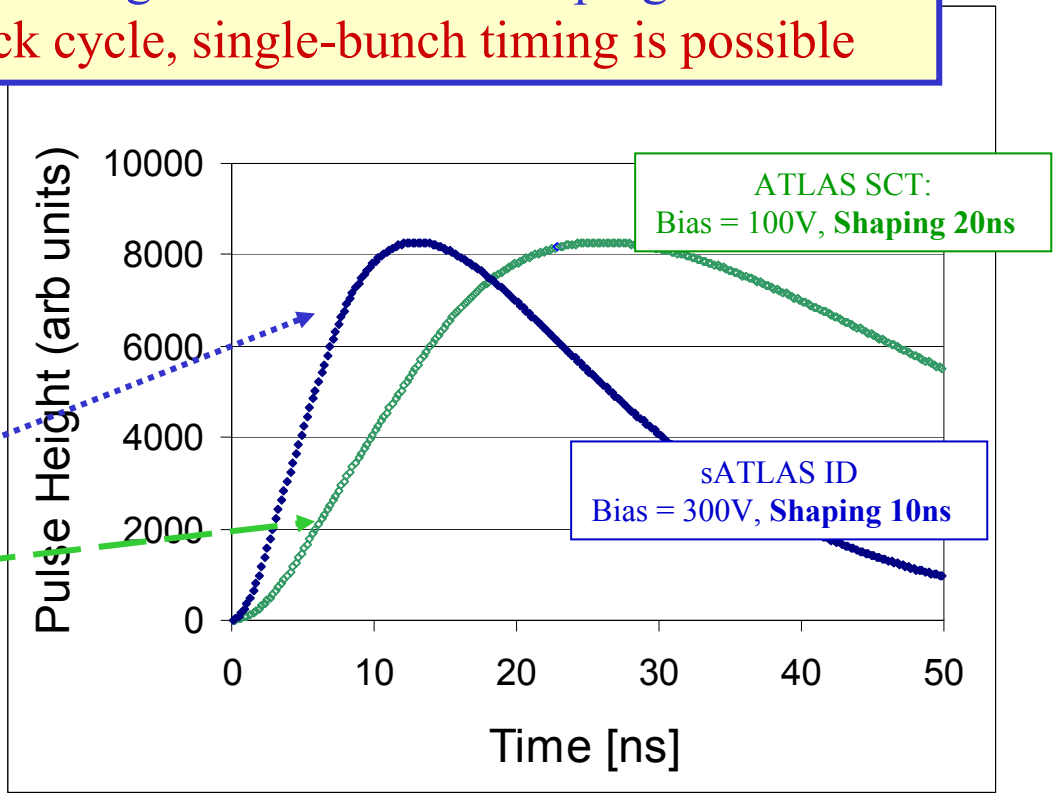
Sub-μ CMOS	"accidentally" rad-hard, low power, used for pixels,CMS, also in sCMS
Bipolar BiCMOS	power-noise advantages for large capacitances and fast shaping, also excellent matching technologies used in ATLAS SCT are not sufficiently rad-hard beyond the LHC because of current gain β degrading from about 100 to about 40 at $10^{14}cm^{-2}$, limited availability
SiGe BiCMOS	very fast (f_T > 50GHz and β > 300), used in cell phones, backend: DSM CMOS "du jour", available IBM–MOSIS rad hardness has been measured to $10^{14}cm^{-2}$ we have now measured test structures in the CERN beam! Survive $10^{16}cm^{-2}$, β useful above $10^{15}cm^{-2}$
SiGefor sLHC?	Expect that largest area of sLHC tracker will be made of strips, so SiGe could give an advantage, specially for short shaping times (noise, overdrive). (Power (SiGe) < Power (0.25 μm CMOS) for "long" strips).

Single-Bucket Timing

Pulse rise time depends on both charge collection and shaping time
If rise time falls within the clock cycle, single-bunch timing is possible

Decrease collection time with increased bias voltage

p-on-n (n-on-p even faster) (M.Swartz)	Collection Time [ns] 100V	300V
Holes	14	7
Electrons	5	2.5



With 20ns shaping and 100V bias, do single-bunch timing at LHC (25ns)
With 10ns shaping and 300V bias, the entire rise of the pulse is within 12 ns:
80MHz single-bunch timing is possible for sLHC, reducing occupancy by 1/2