FPIX2 for FP420?

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FPIX2 at a glance

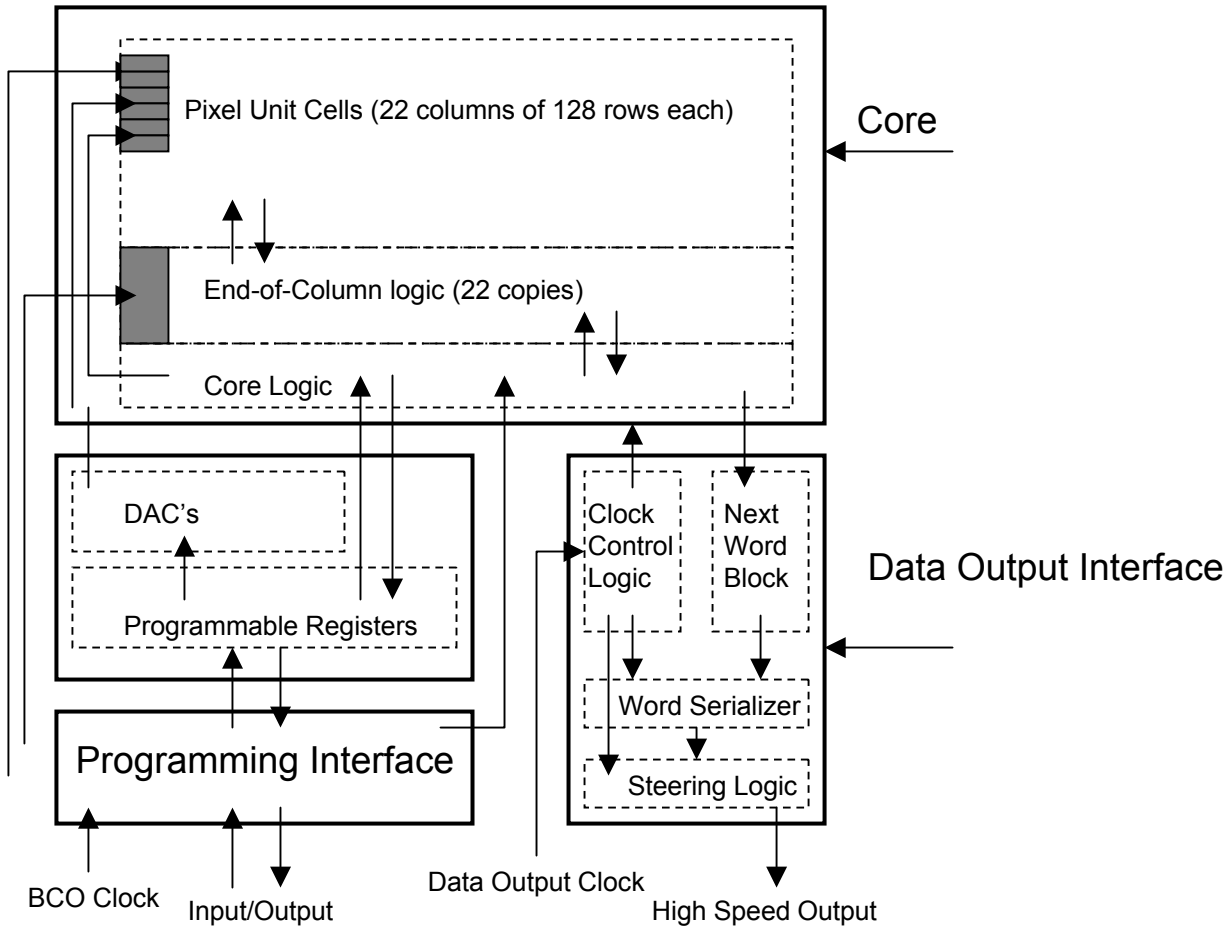
- Designed to be the BTeV pixel chip.
- 50μ x 400μ pixels (like ATLAS).
- 22 columns x 128 rows.
  - Designed to tile chips in one line with 600μ long pixels between chips; not designed to tile two lines of chip on one sensor module.
- High speed, zero suppressed readout.
  - Can be ~30ns/hit.
  - All chips read out in parallel on point-to-point links.
- NO TRIGGER.
- Easy to use.
  - One bias voltage (+2.5V)
  - All LVDS I/O – No other ASIC's required.

FPIX2 Block Diagram

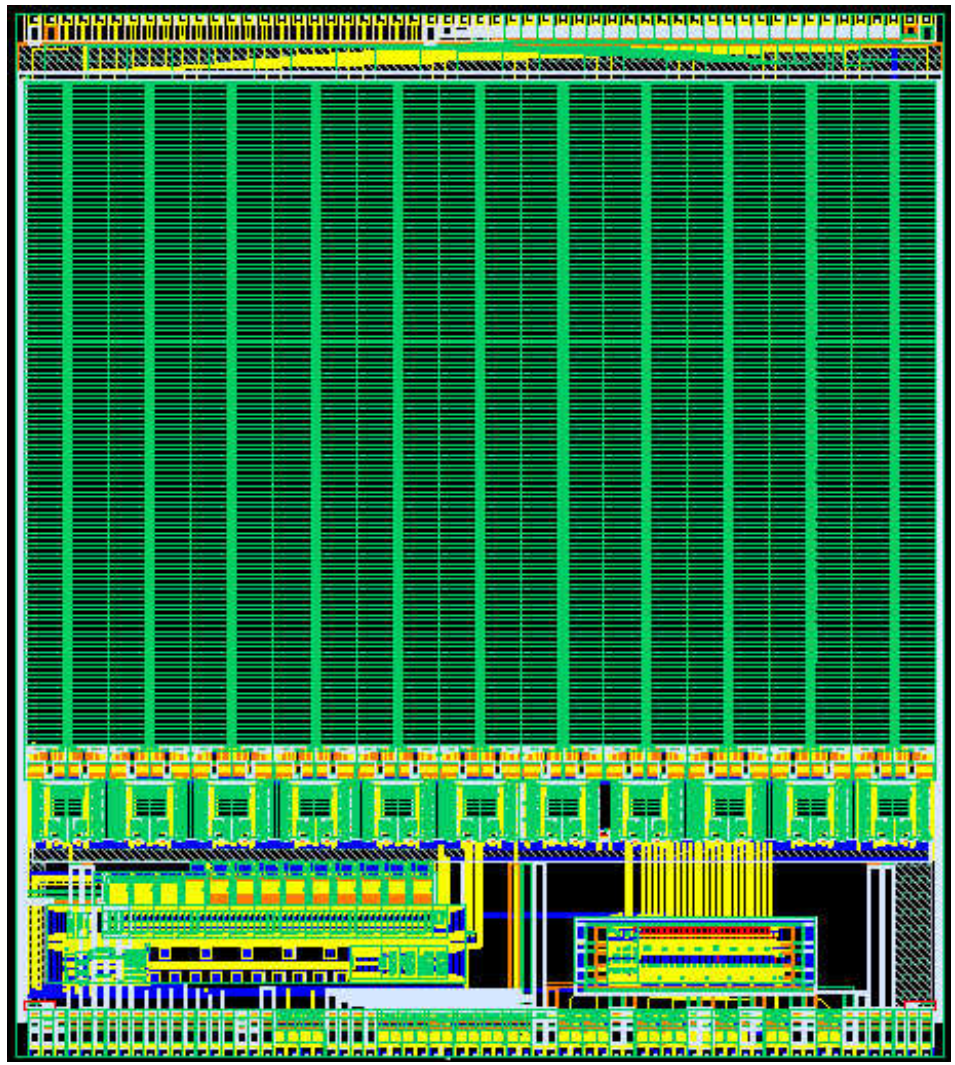
Fabricated by TSMC (through MOSIS).

Only bias voltages required are 2.5V & ground.

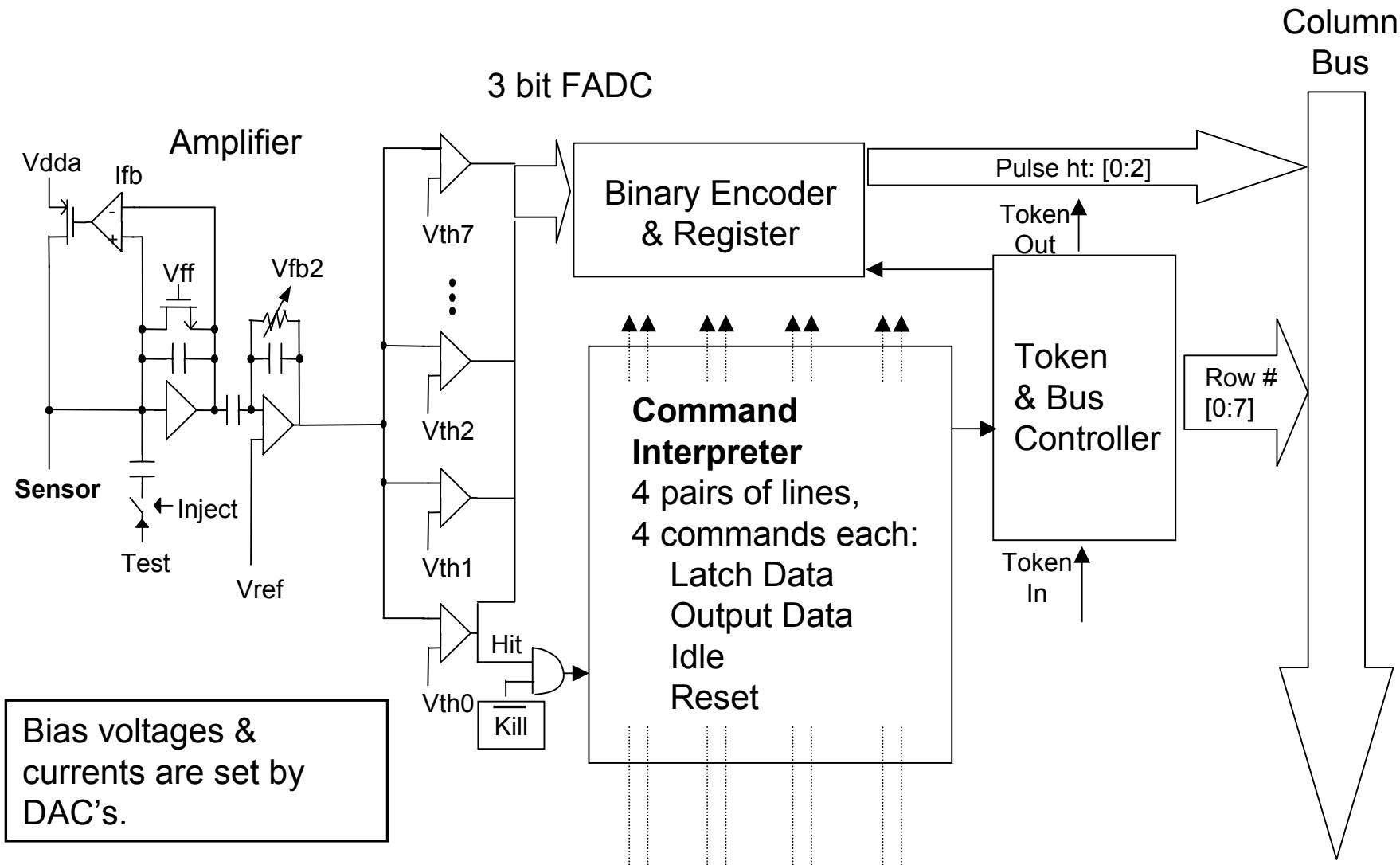
All I/O is LVDS.



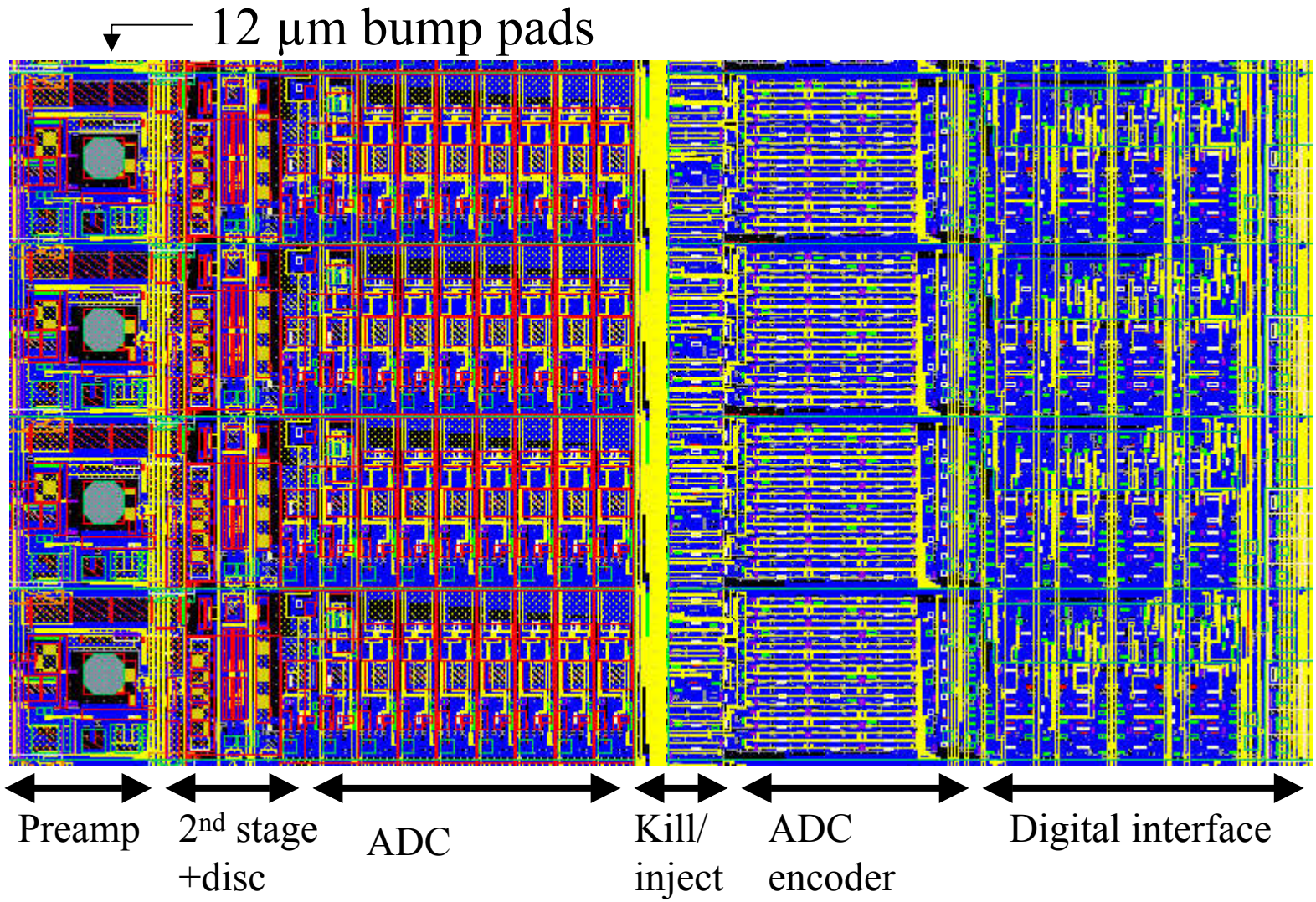
FPIX2 Layout



Pixel Unit Cell



Pixel Cells (four 50 x 400 mm cells)



(Top metal layer not shown)

Status & Plans

- Final submission of FPIX2 = end of May ‘05.
  - Fixes two fatal flaws in current chips.
  - Expect chips back in August – September.
- Will construct modules using BTeV sensors
  - Tesla moderated p-spray sensors, VTT solder bump bonds
  - 8x, 6x, 5x, 4x, 1x
  - Expect modules ~Feb. ’06
- Plan bench tests & beam tests of modules before and after irradiation.
  - Tests will run through fall ’06.

Possible use for FP420

- Study how fast the BCO clock can go.
  - Designed for 7.5 MHz (132 nsec).
  - Will probably NOT work at 40 MHz.
    - May work at 20 MHz.
    - ~50ns time resolution?
- Could bond FPIX2's to other detectors and compare to BTeV silicon modules.