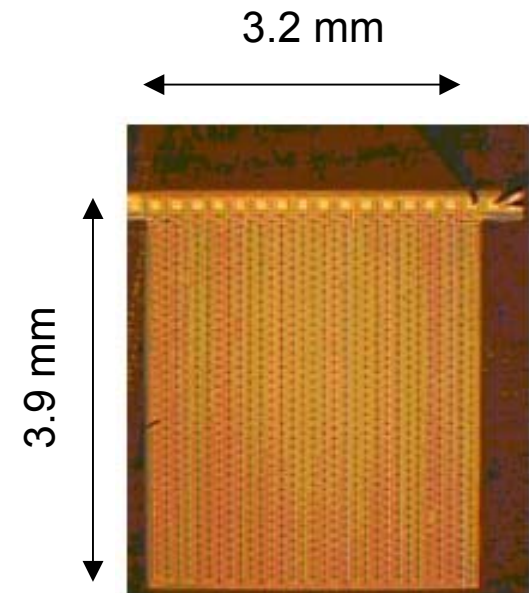
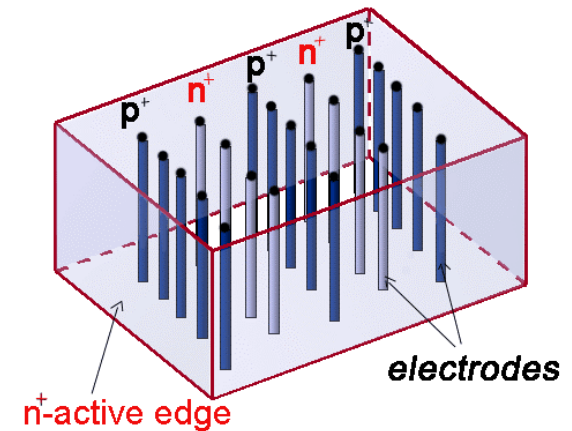


3D detectors: progress and plans



Outline:

- ❖ Requirements at 420 m
 - Edge sensitivity
 - Radiation hardness
 - Spatial resolution - tracking
- ❖ Which RO electronics?
- ❖ Plans for 2005-2006
- ❖ Key issues on: Processing, RO- electronics, Yield



C. Kenney, E. Westbrook, D. Gnani, A. Thompson (Molecular Biology Consortium) C. Da Via', J. Hasi, A. Kok, S. Watts (Brunel U.) S. Parker (U. of Hawaii) G. Anelli, M. Deile, P. Jarron, J. Kaplon, J. Lozano (CERN), V. Bassetti (Genova), H. Yamamoto (Tohoku U.) E. Mandelli (Lawrence Berkeley Lab) J. Morse (European Synchrotron Radiation Facility), E. Perozziello and members from the TOTEM Collaboration for the 2003 test beam.

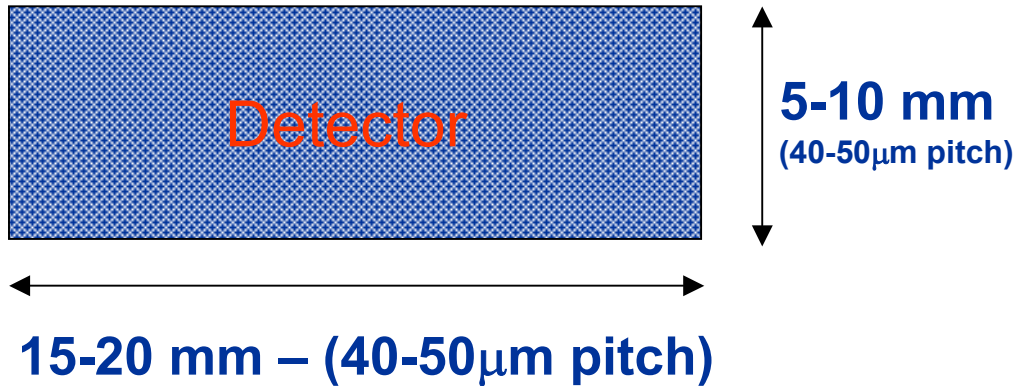
Detector Requirements at 420m

- ❖ High and stable efficiency near the edge facing the beam, insensitive edge region $< 10 \mu\text{m}$ ($10\sigma \sim 3\text{mm}$ in the x- direction!)
- ❖ Compactness, robustness (limited access)
- ❖ S:N = 20:1 (electronics?)
- ❖ Spatial resolution $\sim 10\text{-}15 \mu\text{m}$
- ❖ Overall alignment precision $\sim 20 \mu\text{m}$
- ❖ Immunity from induced RF pickup from bunches
- ❖ Required radiation tolerance $> 10^{15} n_{\text{equiv}}/\text{cm}^2$ at $L=10^{34} \text{ cm}^{-2}\text{s}^{-1}$
- ❖ Operate at low ($\sim 240\text{K}$) or cryo-(1.9K ?) T
- ❖ Be suitable for local event selection and/or trigger capability (L2?)

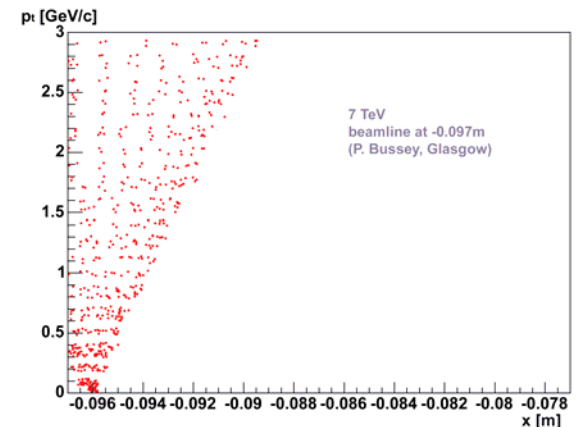
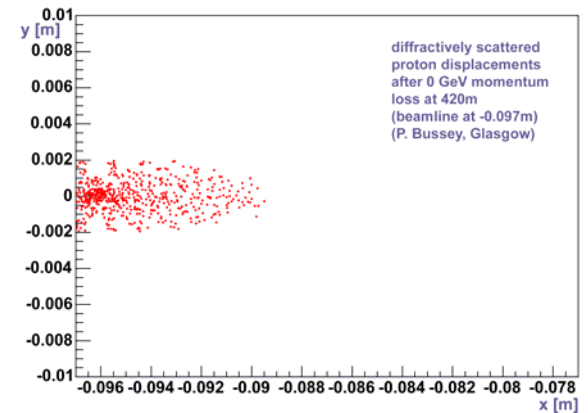
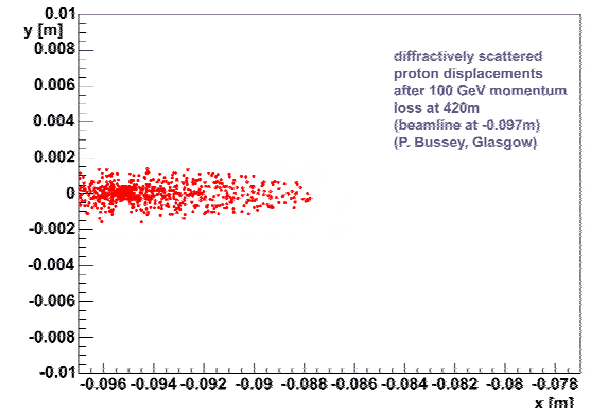
Suitable FE - RO + interface electronics essential!

- ❖ For the moment we have to live with existing LHC compatible RO electronics chips!

Detector size and layout for best resolution (10-15 μm in x and y)



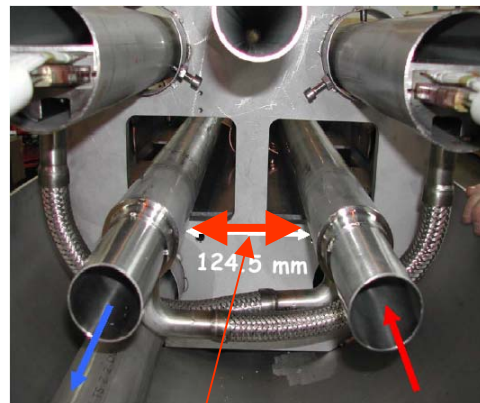
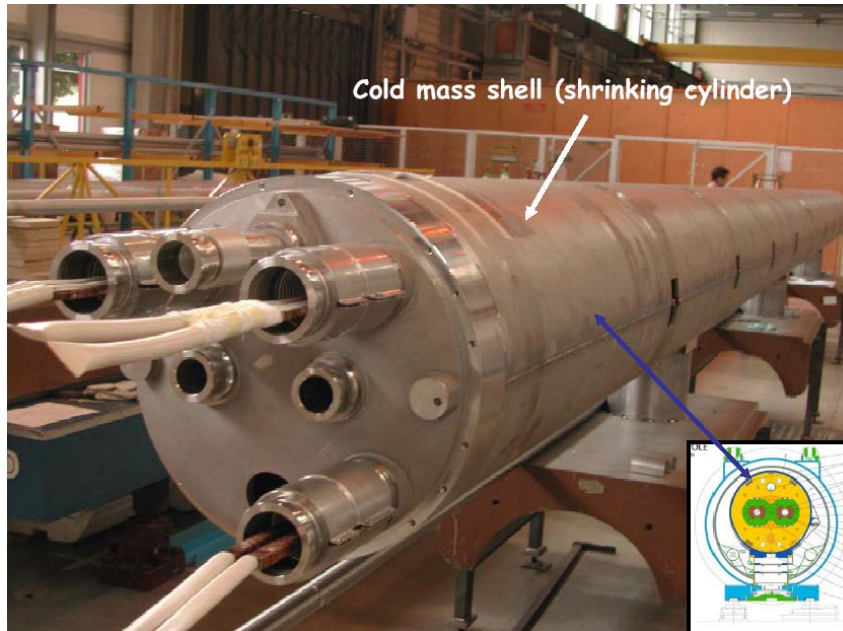
Needs detailed event simulation
See P. Bussey talk



Leading diffractive protons seen at 420m ($\beta^* = 0.5\text{m}$)

The environment (slides from D. Macina)

3D



124.5 mm

- ❖ Lots to do from the mechanical point of view (see R. Orava talk)
- ❖ Two or more insertions to optimise tracking?
- ❖ Electronics interface card + services needs to be small example TOTEM Tower October 2004:

~300 mm



Electronics motherboard

Vacuum flange

Detector planes

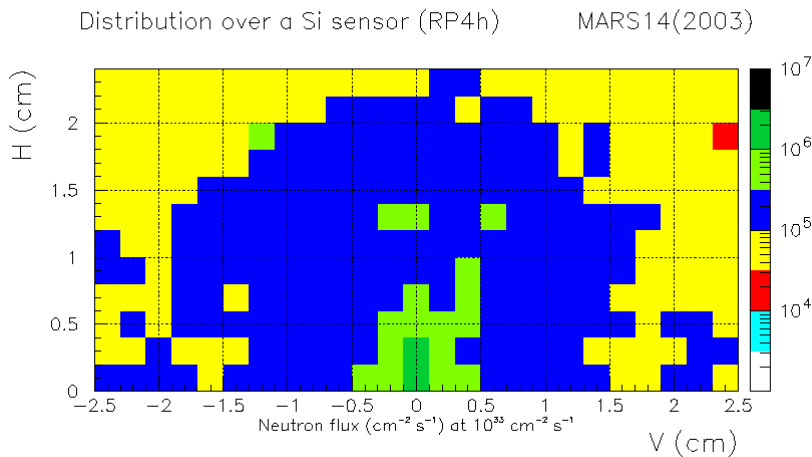
**Cryo+Mechanical+Electronic
Engineering TEAM from the beginning!**

Radiation hardness (220m)

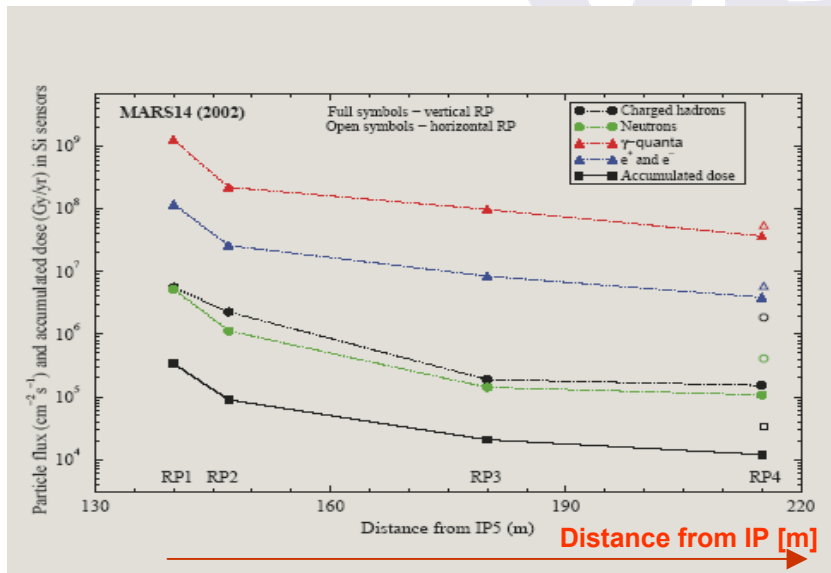
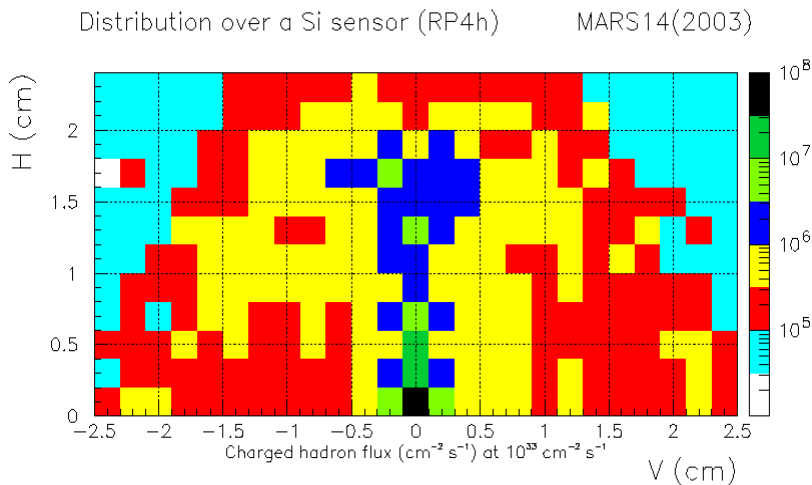
See talk of I. Rakhno

Extrapolation at 420m $\sim 10^{15} \text{n/cm}^2$ ($L=10^{34} \text{cm}^{-2} \text{s}^{-1}$)
Detailed simulations are part of this proposal

Neutron flux



Charged hadrons flux



Work done by Nikolai Mokhov and Igor Rakhno (FNAL, USA LHC) with the simulation code MARS14. Peak luminosity is $L=10^{34} \text{cm}^{-2} \text{s}^{-1}$
 $\beta^* = 0.5 \text{ m}$

Charged hadrons and neutrons fluence integrated over 3 years:

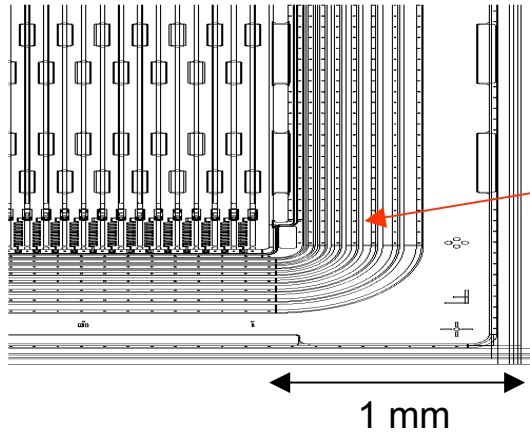
10^{11}cm^{-2} during the dedicated TOTEM runs
 $\langle \mathcal{L} \rangle = 2 \cdot 10^{30} \text{cm}^{-2} \text{s}^{-1}$ and 10^6s

10^{12}cm^{-2} during the high luminosity runs
 (RP in the retracted position)
 $\langle \mathcal{L} \rangle = 0.5 \cdot 10^{33} \text{cm}^{-2} \text{s}^{-1}$ and 10^7s

Rad Hard up to $10^{14} \text{ "n" / cm}^2$ at 220m

to take into account beam accidents and uncertainties on beam halo

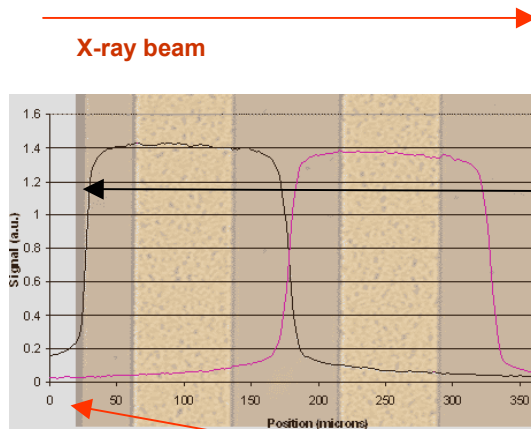
Why Si 3D detectors for 420m and not other existing LHC Si designs?



ATLAS microstrip and pixels
Radiation hard up to $>10^{14}$ (pixels 10^{15}) n/cm²
but ~ 1 mm dead edge for multi-gard rings



Detail of 3x4 cm² Totem Planar/3D Detector fabricated within P324



Planar-3D structure (p⁺-on-p)
Edge sensitivity (measured using
A 12 KeV X-ray beam $\sim 5 \mu\text{m}$
but radiation hard max $\sim 10^{14}$ n/cm²

Previous Beam Tests



**LBL – Advanced light source – 12 KeV, x-ray microbeam – July '03
full 3D, planar 3D / active edges**

CERN / Totem – X5 – 100 GeV muons – Aug. / Sept. '03 – full 3D

**LBL – Advanced light source – 12 KeV x-ray, molecular biology – July '04
planar 3D / active edges**

**ESRF – 12 KeV x-ray microbeam – June '04
full 3D – test of electrode sensitive volume**

**CERN / Totem – SPS – Roman pots, main ring protons – Oct. '04
full-size (3cm x 3cm) planar 3D / active edges**

**CERN / Totem – X5 – 100 GeV muons – Nov. '04
full-size (3cm x 3cm) planar 3D / active edges**

**Numerous x-ray, beta, and gamma tests for speed, radiation hardness,
energy resolution. Irradiation tests at LBL, CERN, Praha.**

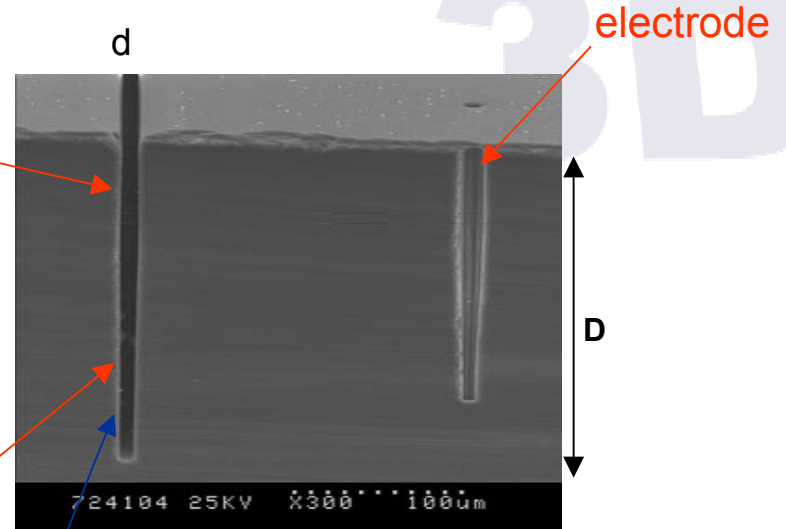
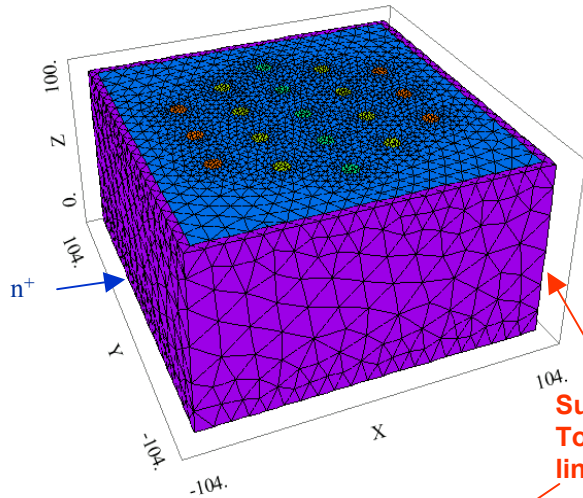
3D detector status



What do we know	Still to do	When
Edge efficiency ~6 μm	done	----
S/N =14:1 with 180μm thick substrate	Optimise structure with RO	2005
Tracking capability Yes with strip RO	Test with LHC-pixel RO	2005
Radiation hardness CCE up to $1 \times 10^{15} \text{p/cm}^2$ Depletion up to $2 \times 10^{15} \text{n/cm}^2$	Check radiation hardness limit: Samples have been irradiated up to 10^{16}n/cm^2	2005
Size tested with LHC RO Works with $3.9 \times 3.2 \text{mm}^2$ LHC-strip RO electronics	Test bigger size detectors We have fabricated working $6 \times 9 \text{mm}^2$	2005
Big detector area can be achieved by 'butting' several devices together	To be done needs engineering	2006
EM pickup	To be done	??? 2006
Can operate at cryo-T	Done down to 130K	----

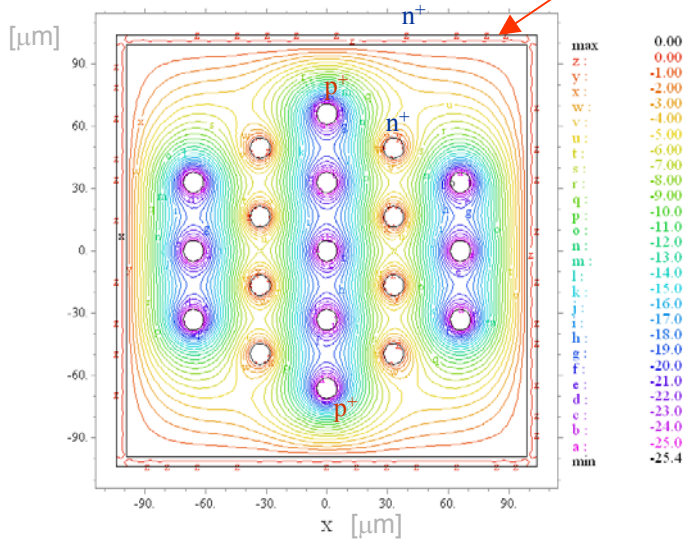
Edge sensitivity: 3D

fabrication details later in this talk

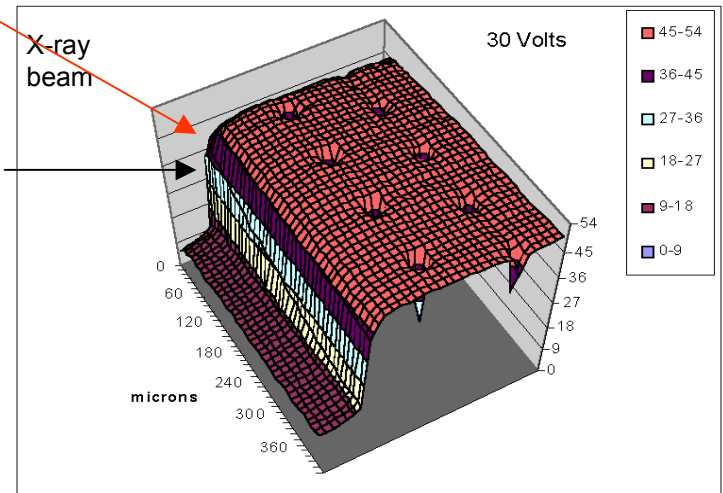


Surrounding n+ electrode
To complete the e-field
lines

Trench = active edge

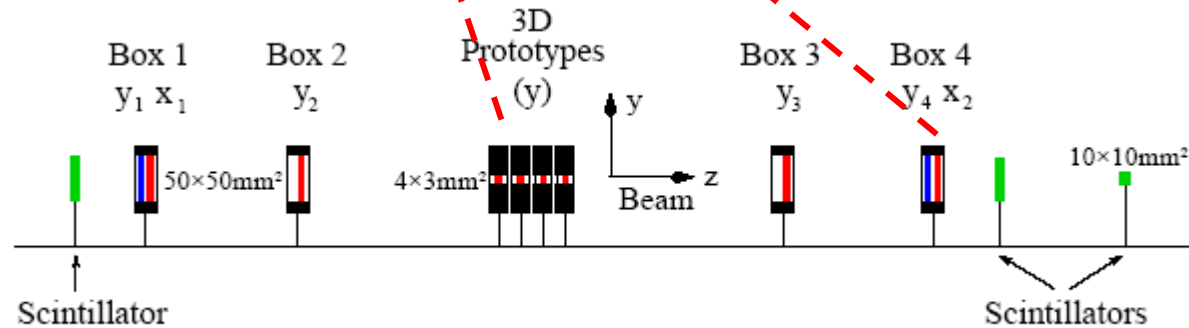
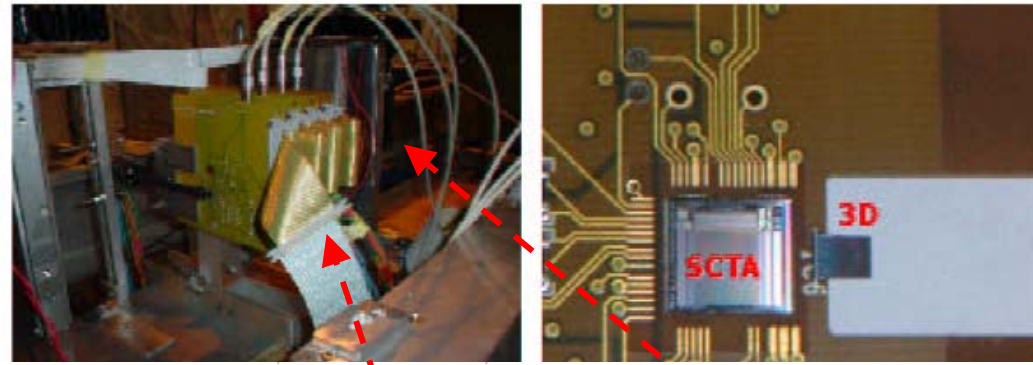


10-90% - 6 μm



Tracking capabilities

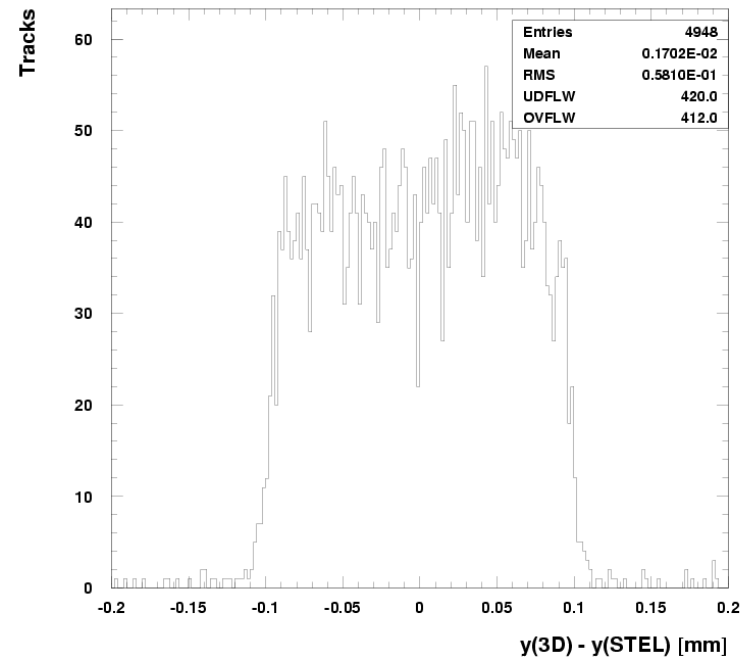
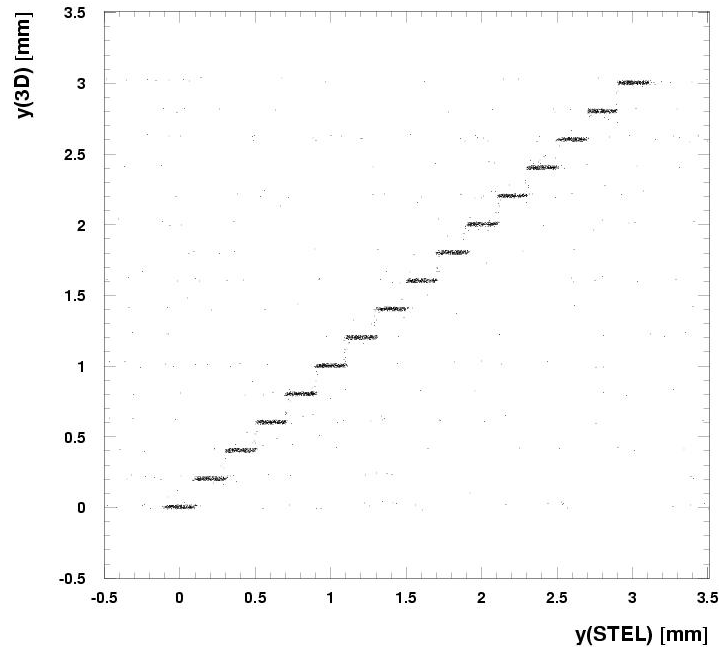
3D



Totem X5 test beam at CERN - 2003.


1. The 3D planes: 16 -- 200 μm (y) by 40 -- 100 μm (x) cells, n bulk and edges.
2. They are tied together in x-rows for a y readout using SCTA integrated circuits and a scintillator trigger.
3. The 3D planes are centered between a 4-plane silicon strip telescope with 4 y planes and 2 x ones. $\sigma_y = \pm 4 \mu\text{m}$.
4. The beam was set for 100 GeV muons.

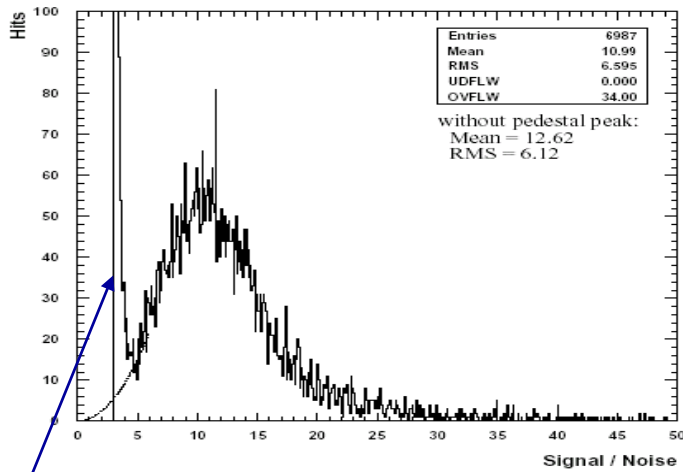
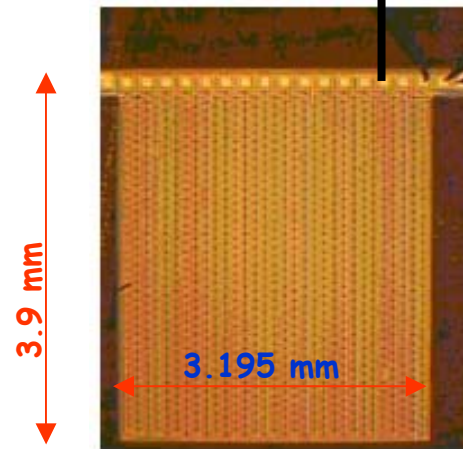
Spatial resolution SPS - TOTEM test beam 2003



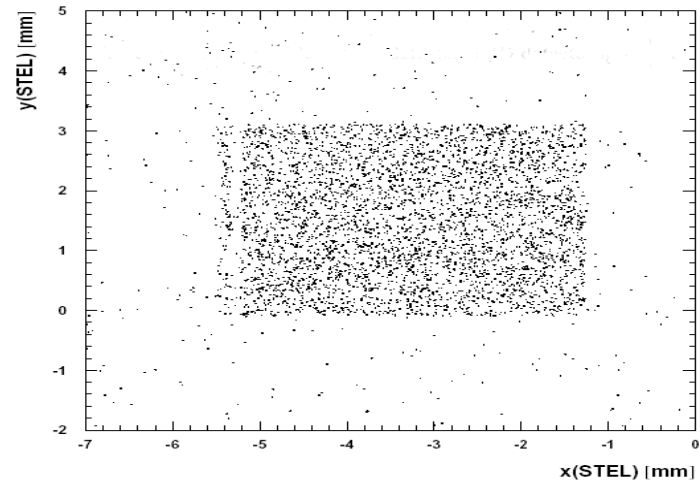
**Correlation and residual distribution: telescope resolution = 4 μm
3D inter-electrode spacing = 200 μm**

Tracking Efficiency ~98%

Electrodes connected together
Using Al strips  To SCTA input



pedestal



SPS - TOTEM test beam 2003

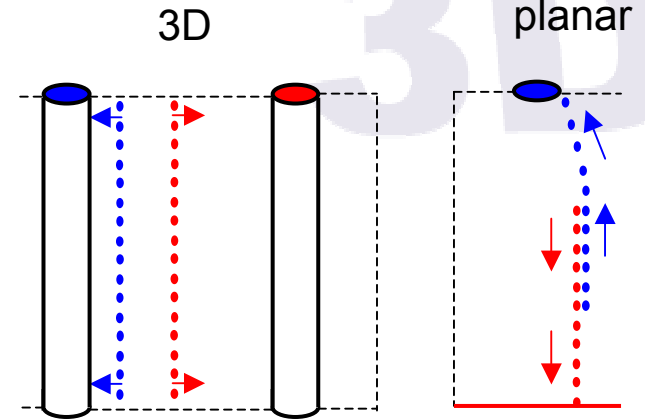
3D design and radiation hardness

- ❖ Short collection distance
- ❖ High average e-field with moderate V_{bias} (5-10V)
- ❖ Parallel charge collection
- ❖ Always use full substrate thickness (MIP $\sim 80 e^-/\mu m$)

❖ Drawback: higher Capacitance

(measured 200 fF/121 μm /electrode) \rightarrow

Pixel readout or strixels

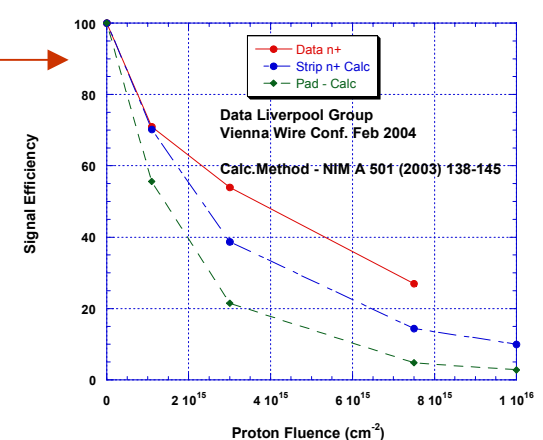
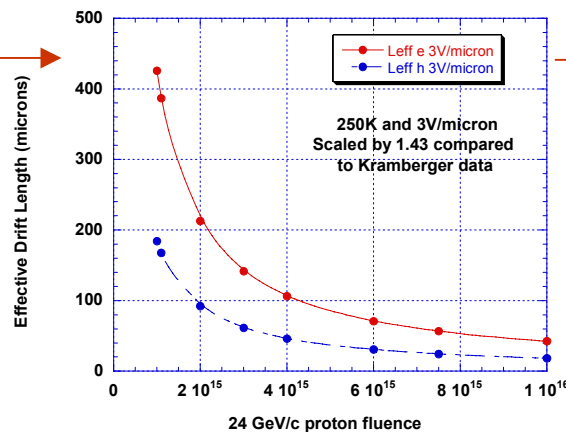
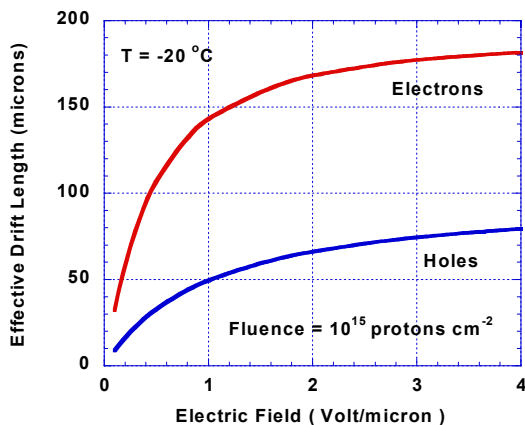


$$L_{eff} = V_D \times \tau_{eff}$$

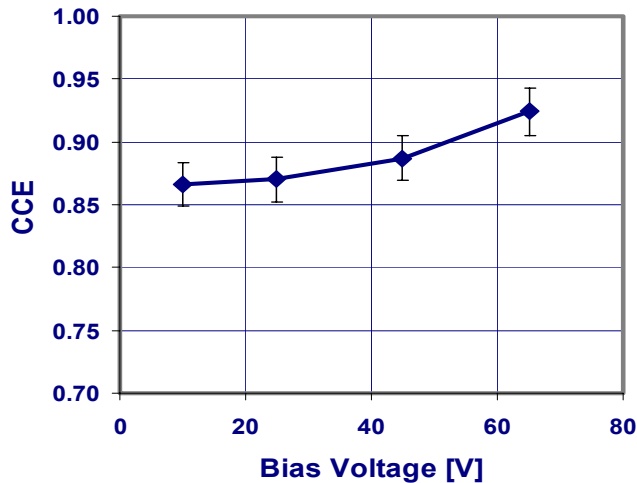
Ramo's theorem + charge trapping

$$P(x) = e^{-\frac{x}{L_{eff}}}$$

$$CCE = \frac{1}{1 + K_c \phi} \quad K_c = \frac{L_0 K_\tau}{V_D}$$

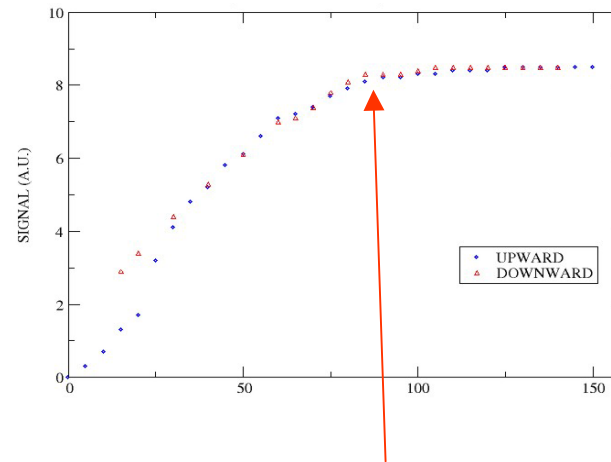
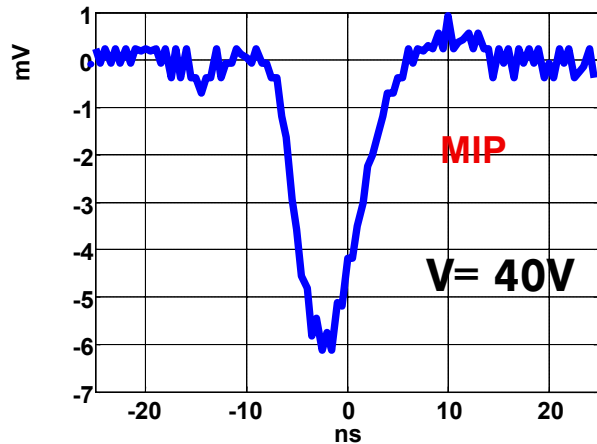


Radiation Hardness of 100 μm inter-electrode spaced 3D



Irradiated up to 10^{15} p/cm ($5 \times 10^{14} n_{\text{eq}}/\text{cm}^2$)

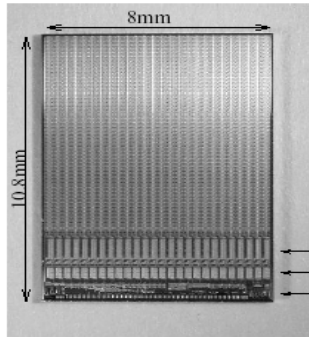
- ❖ Speed: 3.5 ns typical rise time
- ❖ full pulse width < 10 ns
- ❖ Irradiated, stored and measured at $T = 20^\circ\text{C}$
- ❖ Not oxygenated,
- ❖ Collecting holes



❖ full depletion voltage at $20^\circ\text{C} = 105$ V after $2 \times 10^{15} n_{\text{eq}}/\text{cm}^2$!!

Existing LHC Rad-Hard pixel readout electronics chips

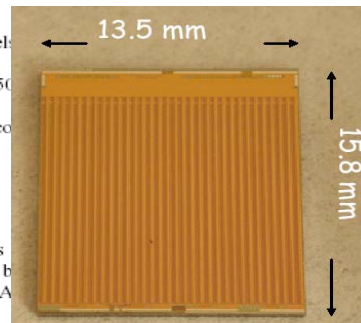
CMS



52 x 53 pixels
150µm x 150µm
26 double-co

data-buffers
time-stamp b
Interface, DA

ALICE+LHCB 22x60 mm²)



From pixel 2002 W. Erdmann

From vertex 2004 – A. Kluge

ATLAS

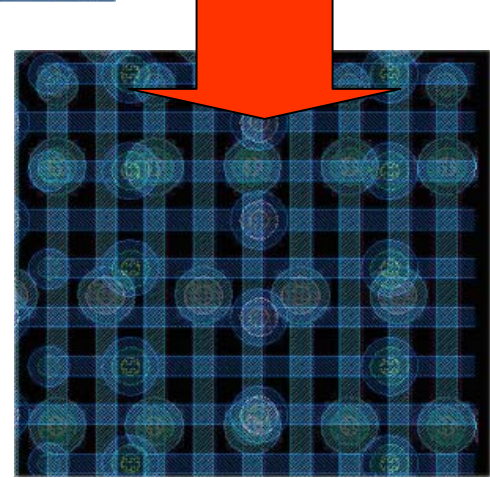
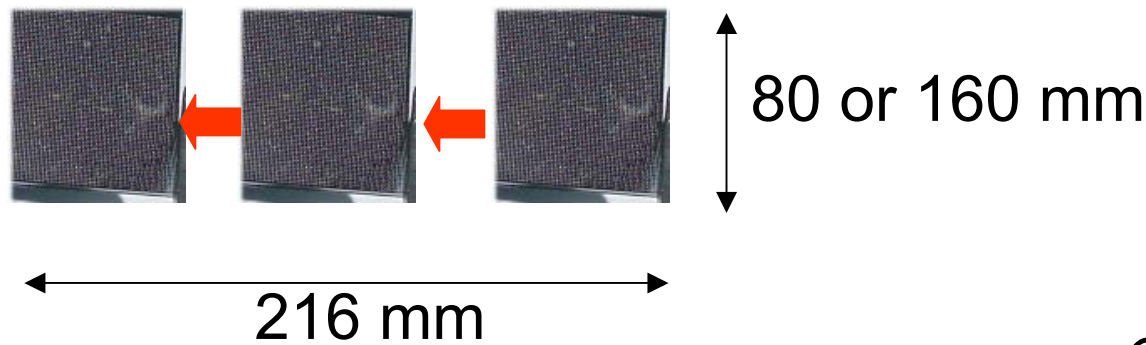
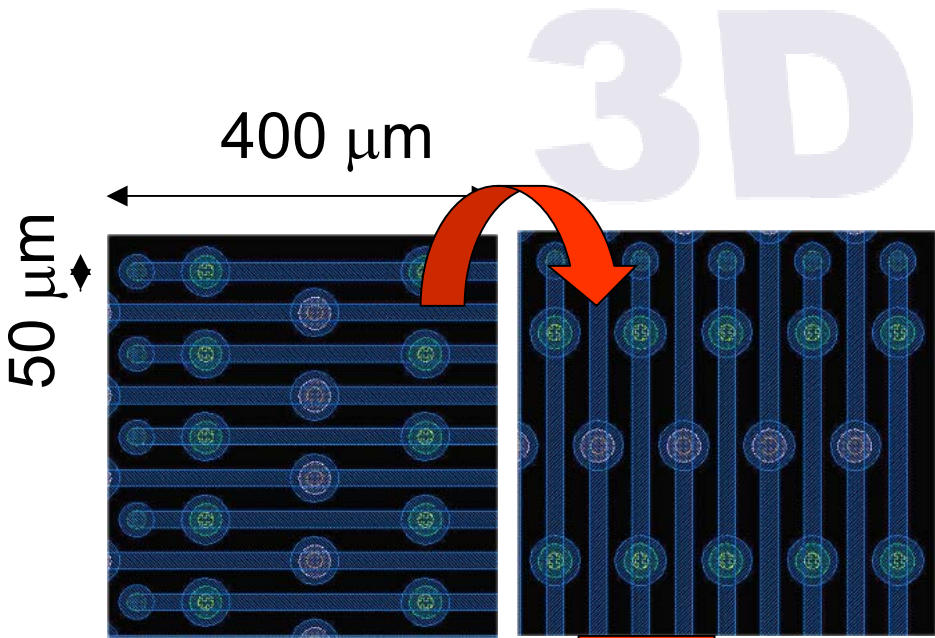
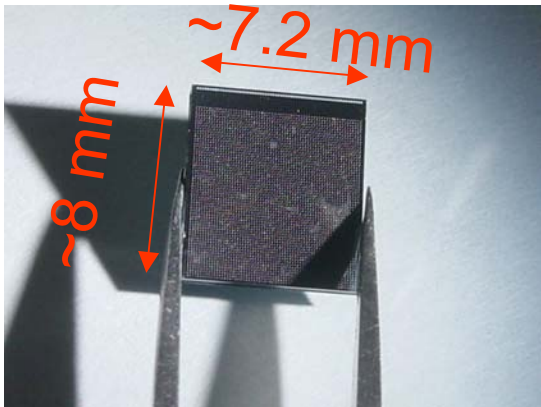


From pixel 2002 R. Beccherle

LHC EXPERIMENT	DIMENSIONS	RO SIGNAL	TRIGGER	BUFFER
ATLAS	50x400 µm ² 7.2x8mm ²	binary and time over threshold	Internal fast-OR	2 - 6.4µs 40 MHz
CMS	125x125µm ² 8x8mm ² ?	analogue	---	---
ALICE	50x425 µm ² 13.5 x15.8 mm ²	binary	Internal fast-OR	51.2 µs 10 MHz
LHC-B	62.5 X 500 22X60mm	binary	Fast-Or +analogue signal	51.2 µs 40 MHz

Modifications:
1 year +190kChF

A possible starting layout:
 7.2x8 mm² 3D edgeless
 ATLAS pixel compatible
*..more on edgeless RO
 later..*



$$\sigma_{x,y} = \frac{50 \mu\text{m}}{\sqrt{12}} = 14.4 \mu\text{m}$$

3D Plan:

2005:

- ❖ Rad hard tests: sample irradiated up to $\sim 10^{16}$ n/cm²
to be measured!
- ❖ Tests with existing RO electronics
- ❖ Process improvements including high yield criteria
- ❖ Simulations

2006:

- ❖ Design of electronic board for full size detector
- ❖ Lab test with controls, daq, etc..
- ❖ Test beam with dedicated insertion

- ❖ ISSUES: funds, manpower, coordination

3D420 working plan and possible Contributions:

Activity	Team
Device fabrication	MBC - Hawaii – Brunel at Stanford
Lab Tests with RO electronics	Under discussion
Read-Out electronics and data transmission card design	Team work with mech. And electr. engineers
Radiation Hardness tests	3D collaboration (MBC-Hawaii-Brunel)
Detector card design and Insertion integration	Team work with elect. Engineers and insertion groups
Beam tests	All
EM pickup studies	??
Device simulation	Brunel..
Detector Simulation for Physics	??

We need to form NOW a FP420-Detector task force!

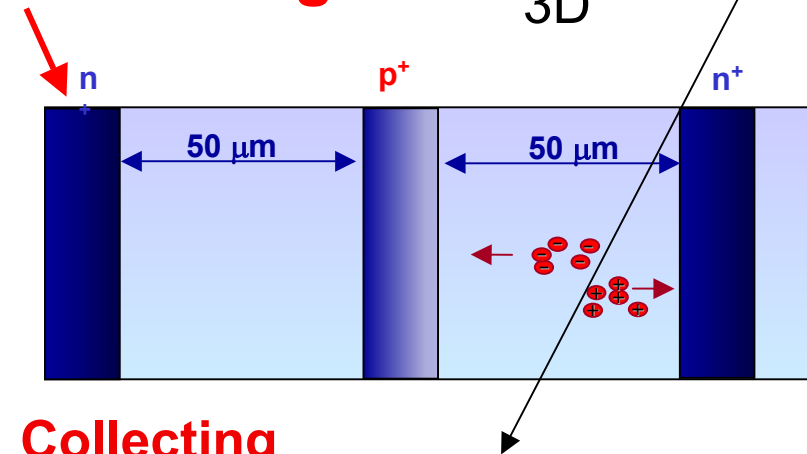
Key issues to be addressed about 3D

- **Fabrication**
- **Active edges and existing readout chips**
- **Timing**
- **Yield**

3D versus planar detectors (not to scale)

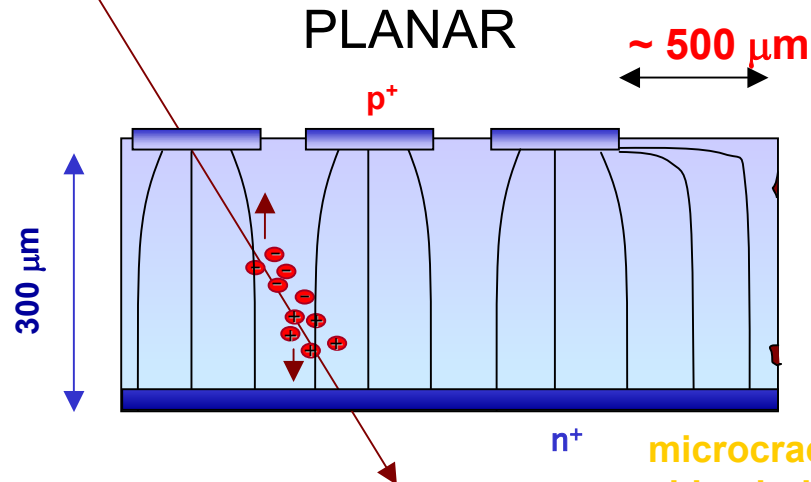
3D

Active edge



particle

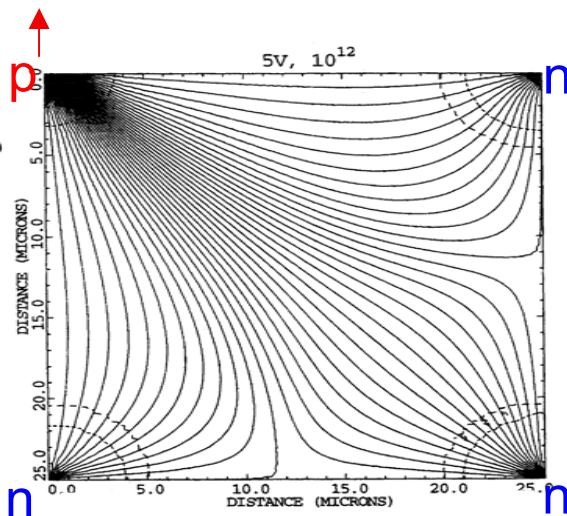
PLANAR



~ 500 μm

Collecting electrode

microcracks, chips induce surface leakage current



MEDICI simulation of a 3D structure

- ❖ **DEPLETION VOLTAGES**
- ❖ **EDGE SENSITIVITY**
- CHARGE 1 MIP (300 μm)**
- CAPACITANCE (121 μm)**
- COLLECTION DISTANCE**
- SPEED**

3D

planar

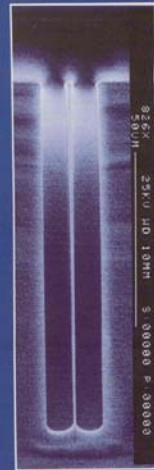
< 10 V	70 V
< 10 μm	500 μm
24000e⁻	24000e⁻
200fF	100-200fF
50 μm	300 μm
1-2ns	10-20 ns

Keys to the technology



1. Plasma etchers can now make **deep, near-vertical holes and trenches:**
 - a. SF_6 in plasma \rightarrow F, F $-$ \rightarrow driven onto wafer by E field
 - b. $\text{Si} + 4\text{F} \rightarrow \text{SiF}_4$ (gas)
 - c. SF_6 replaced with $\text{C}_4\text{F}_8 \rightarrow \text{CF}_2$ + other fragments which
 - d. form teflon-like wall coat protecting against off-axis F, F $-$
 - e. repeat (a – d) every 10 – 15 seconds
2. At $\sim 620^\circ\text{C}$, ~ 0.46 Torr, **SiH_4 gas molecules** bounce off the walls many times before they stick, mostly entering and leaving the hole. When they stick, it can be anywhere, so they form a conformal polysilicon coat as the H leaves and the silicon migrates to a lattice site.
3. Gasses such as **B_2O_3** , B_2H_6 (diborane), **P_2O_5** , and PH_3 (phosphine) can also be deposited in a conformal layer, and make p+ and n+ doped polysilicon.
4. Heating drives the dopants into the single crystal silicon, forming p–n junctions and ohmic contacts there. Large E drift fields can end before the poly, removing that source of large leakage currents.
5. Active edges are made from trench electrodes, capped with an oxide coat. Plasma dicing up to the oxide etch stop makes precise edges.

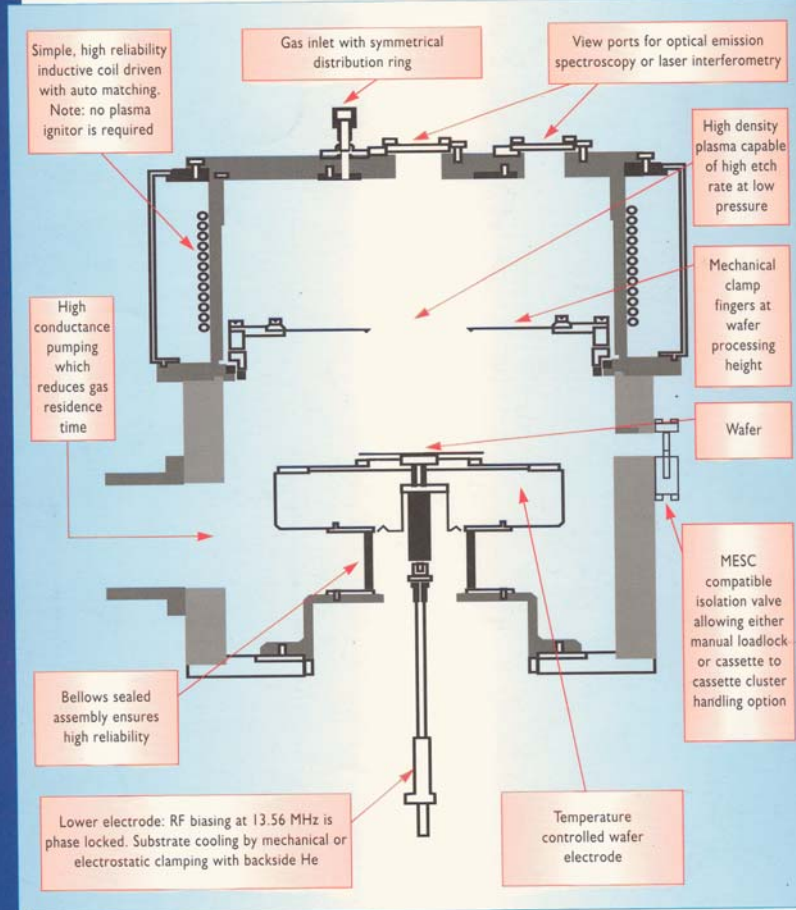
The original STS etcher. (Newer ones by Alcatel, STS, and others have a number of design changes. Etching should be faster. It should be possible to make narrower trenches and holes.)



Multiplex ICP

Conventional plasma sources are unable to meet the progressive demands of modern processes which include higher etch rate and selectivity values, tighter profile control reducing CD and increasing aspect ratio while maintaining minimal microloading and

macroloading effects. An advancement in plasma source design is essential to accomplish realisation of these requirements. The Multiplex Inductively Coupled Plasma (ICP) from Surface Technology Systems provides the solution.



SURFACE TECHNOLOGY SYSTEMS LIMITED, PRINCE OF WALES INDUSTRIAL ESTATE, ABERCARN, NEWPORT, GWENT, NP1 5AR, UK
 TELEPHONE +44 (1493) 249044 FAX: +44 (1493) 249478

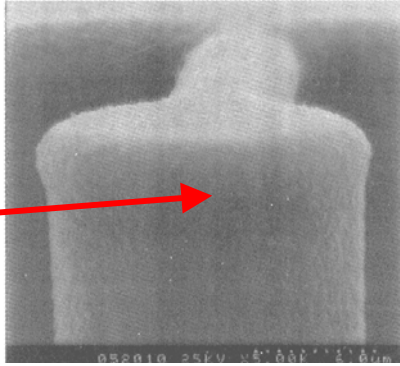
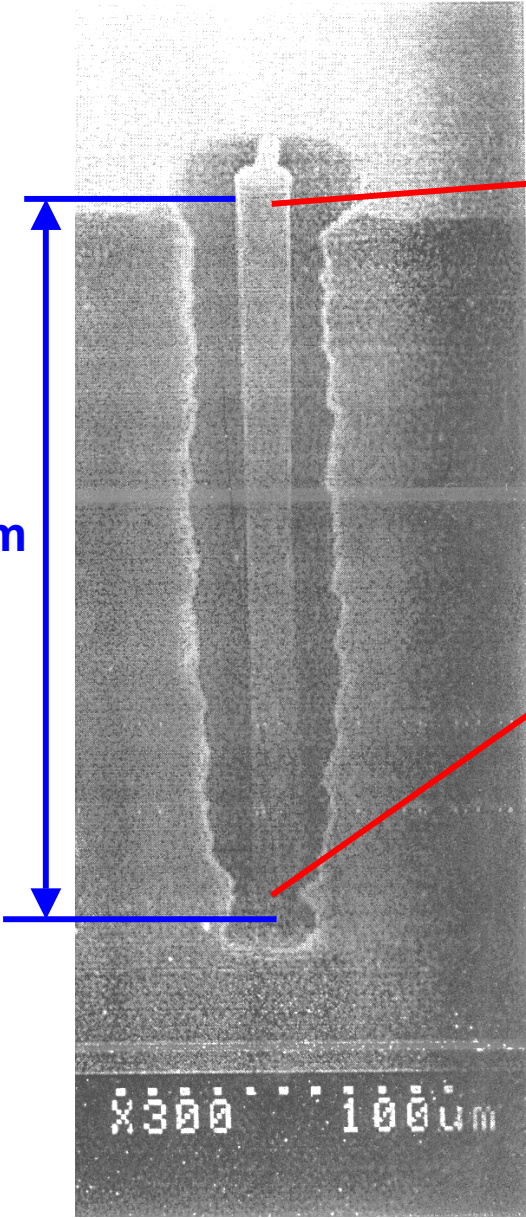
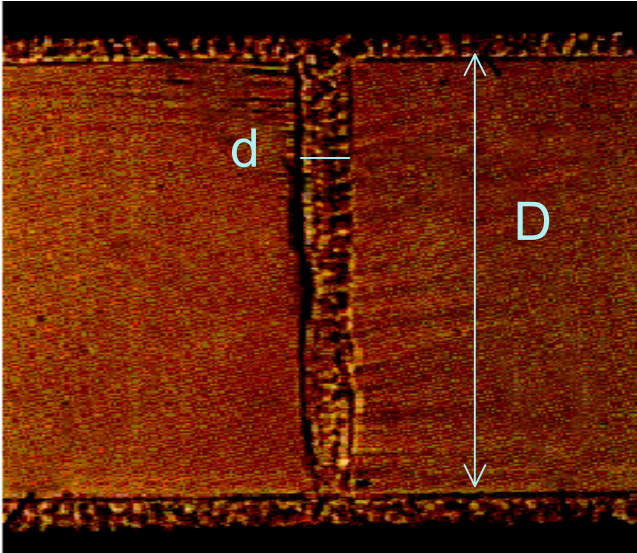
(1633) 652400

Examples of etching and coating with polysilicon.

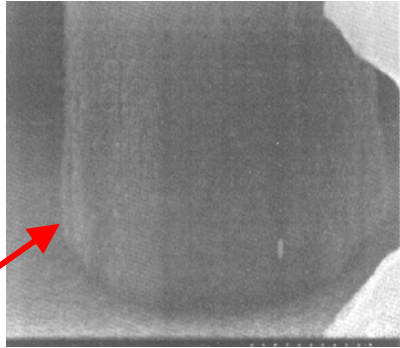
An early test structure by Julie Segal, etched and coated (middle, right), showing conformal nature of poly coat.

An **electrode hole, filled**, broken (accidentally) in a plane through the axis, showing grain structure (below). The surface poly is later etched off.

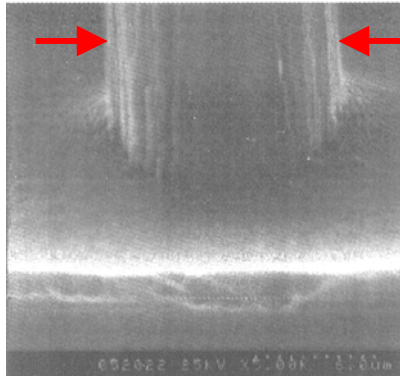
290 μm



coated, top

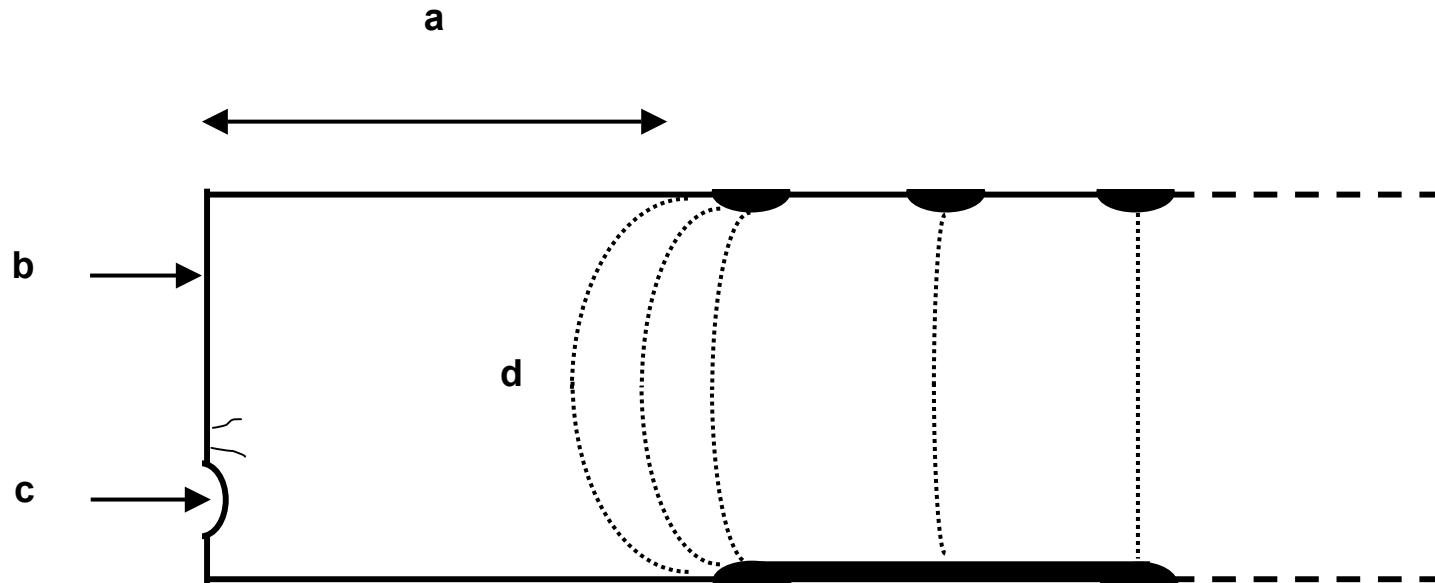


coated, bottom



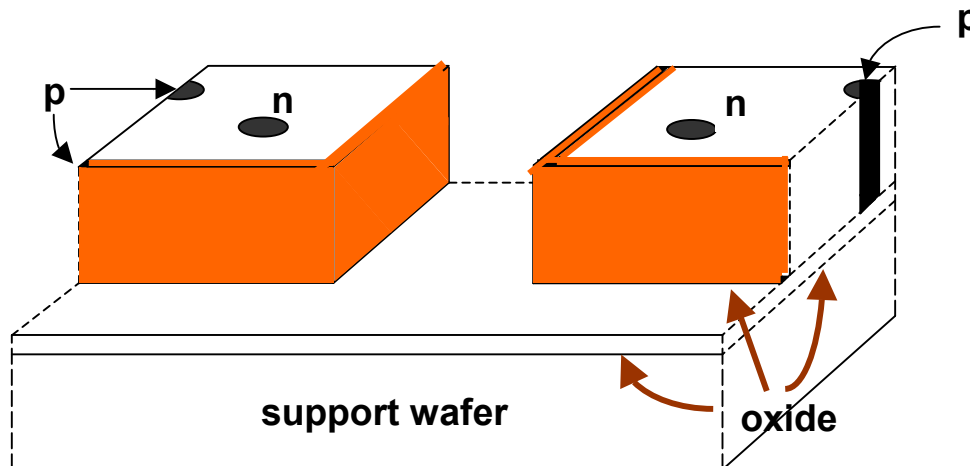
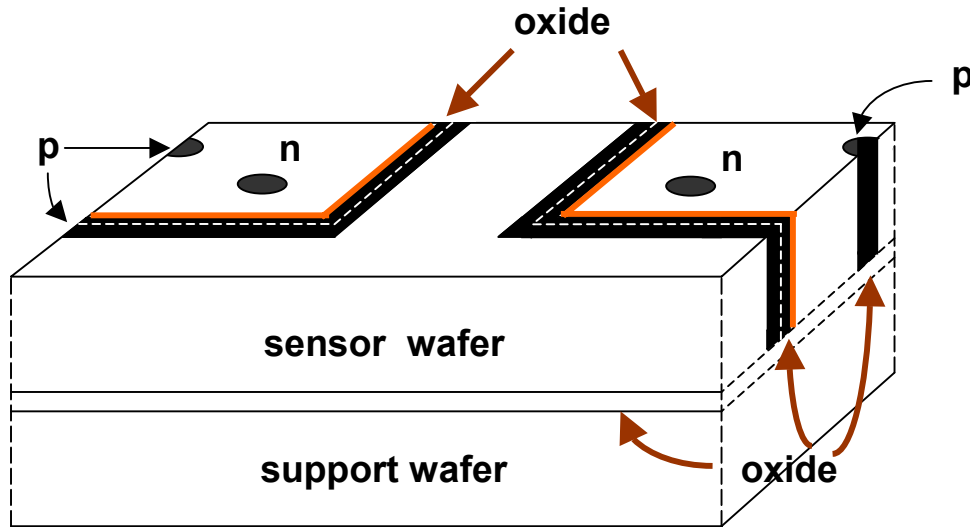
uncoated

Reasons for dead borders on standard planar technology sensors



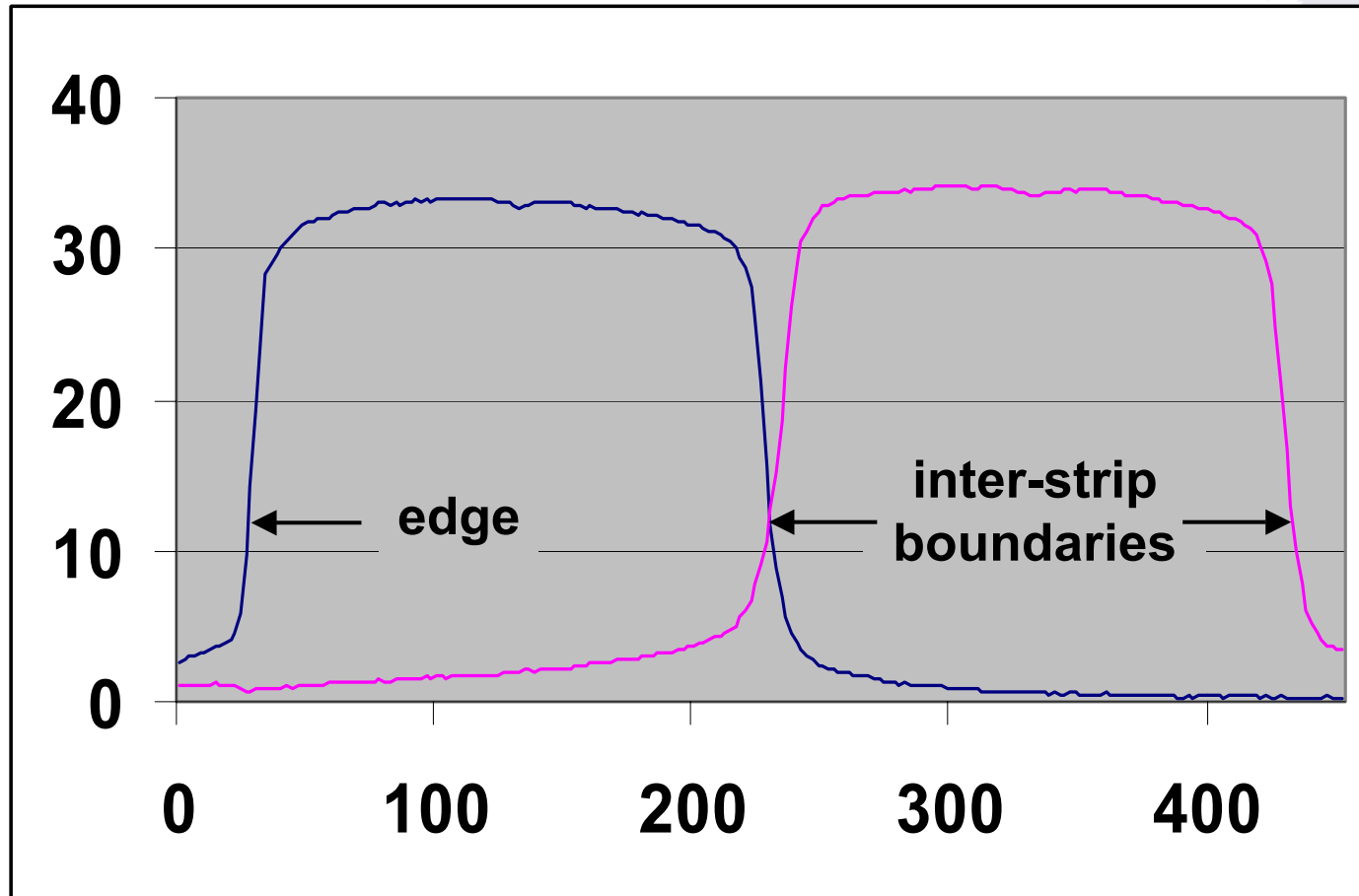
- a. space for guard rings
- b. sawed edges connecting top and bottom are conductors
- c. chips and cracks are also conducting and can reach inside the edges
- d. the field lines bulge out, and should be kept away from b and c

Active Edges

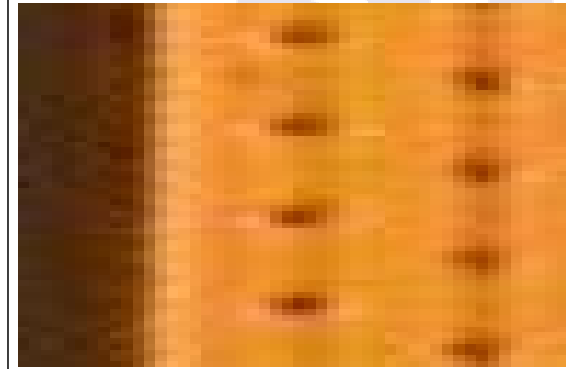
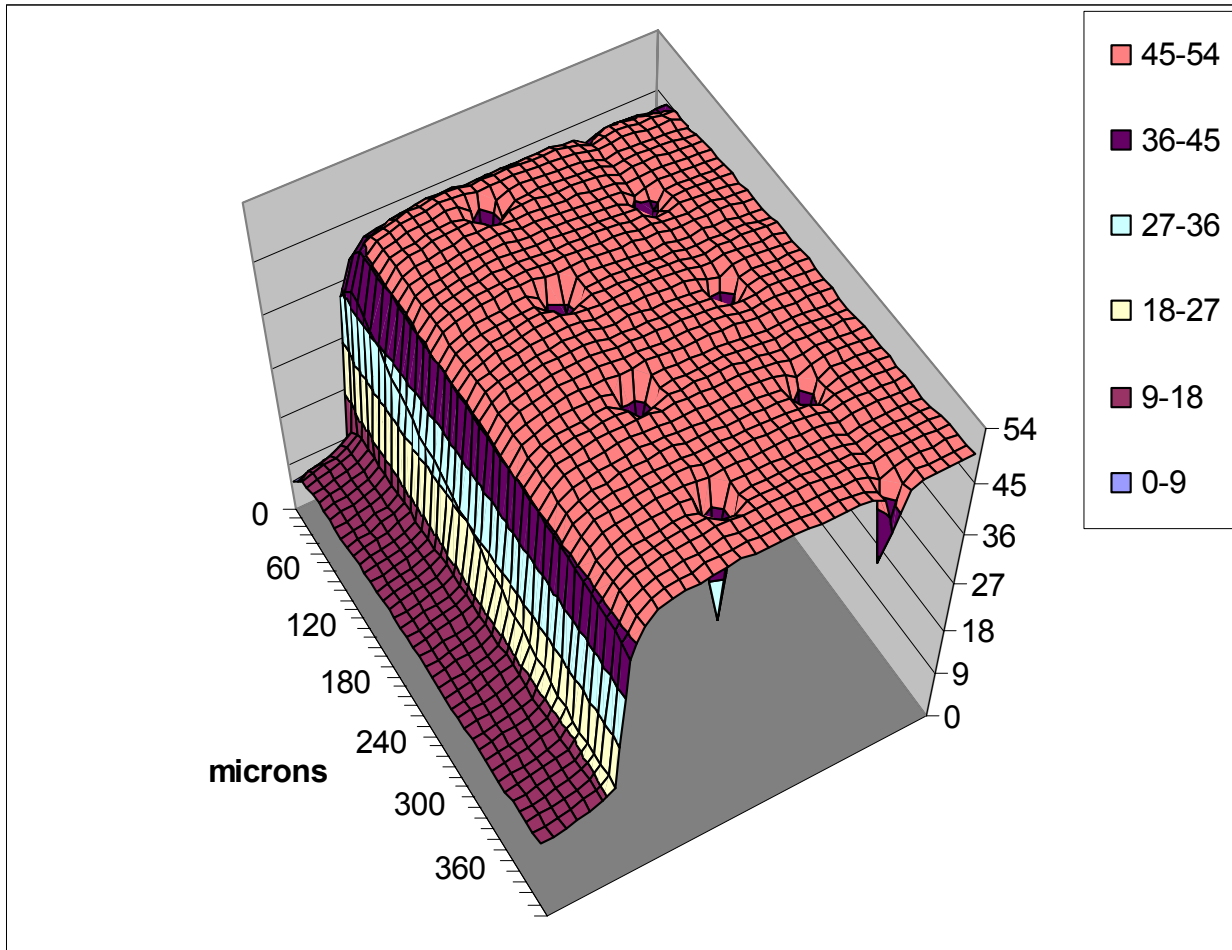


1. etch border trenches
2. diffuse in dopant
3. grow protective oxide cover
4. fill trench with poly
5. vertical, directed etch (to dotted lines)
6. turn off sidewall protection step
7. isotropic etch to oxide stop
8. additional steps are not included on this slide (and note, bonding oxide to support wafer not colored)
9. n and p electrodes can be reversed

X-ray microbeam results for a 3D sensor

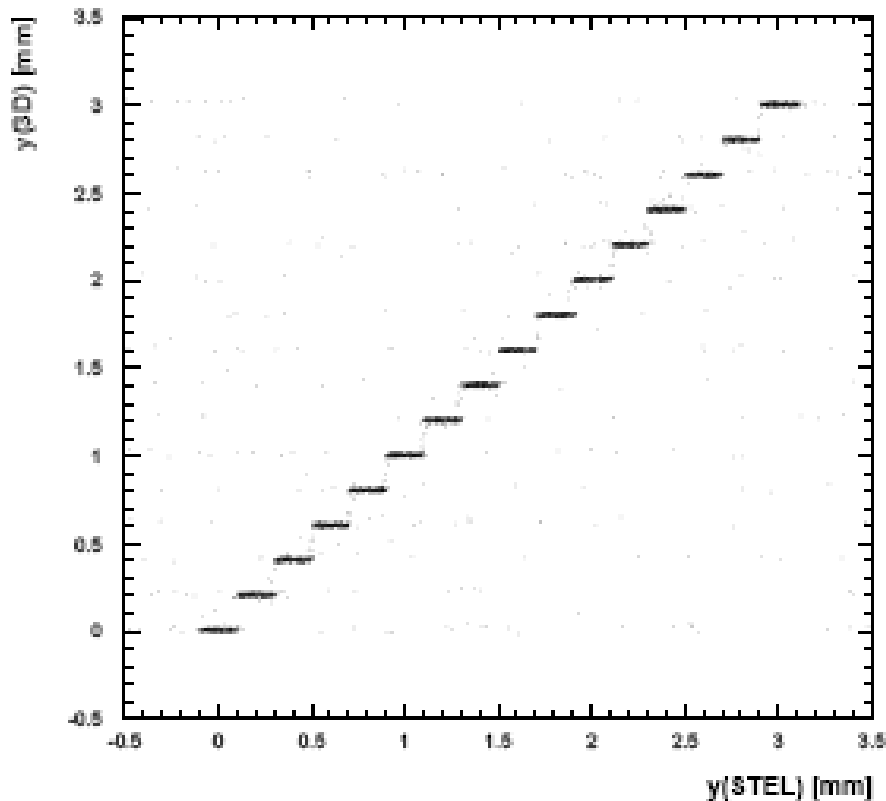


X-ray micro-beam scan, in 2 μm steps, of a 3D, n bulk and edges, 181 μm thick sensor. The left curve is for the edge p channel. The horizontal scale is in μm ; the vertical is arbitrary. The small dip in each center is from nearby 3D electrodes. The left edge tail is from reflected gold x-rays and from leakage current.

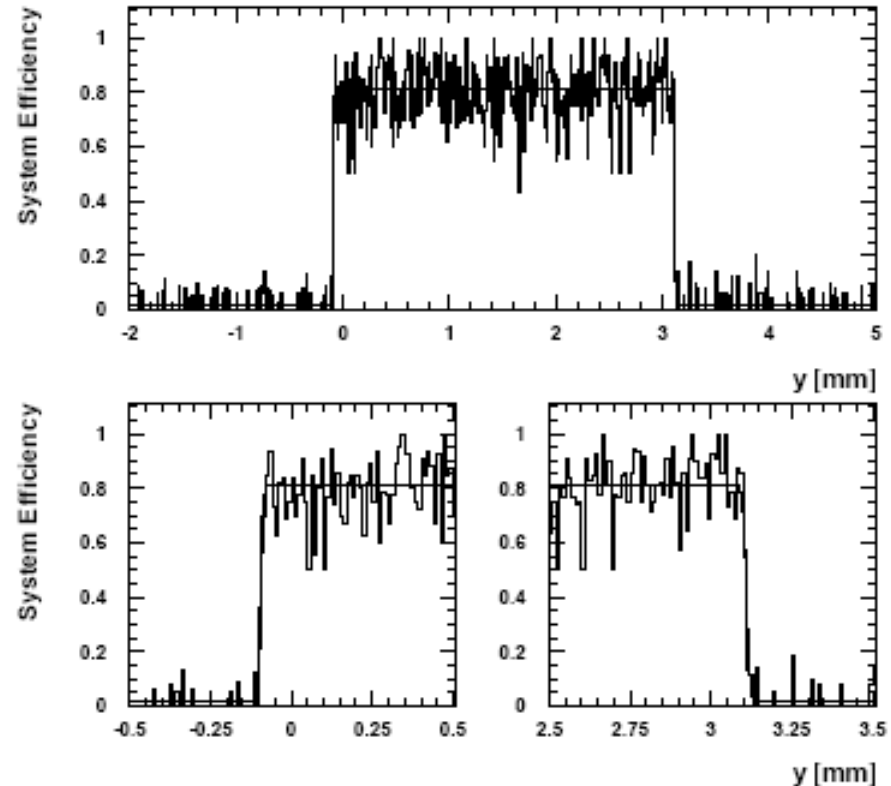


Current from scan in an x-ray microbeam, of another 3D sensor with a photomicrograph of the corresponding part on the right. Grid lines are spaced 10µm apart.

Some results from the CERN X5 beam test (100 GeV muons)



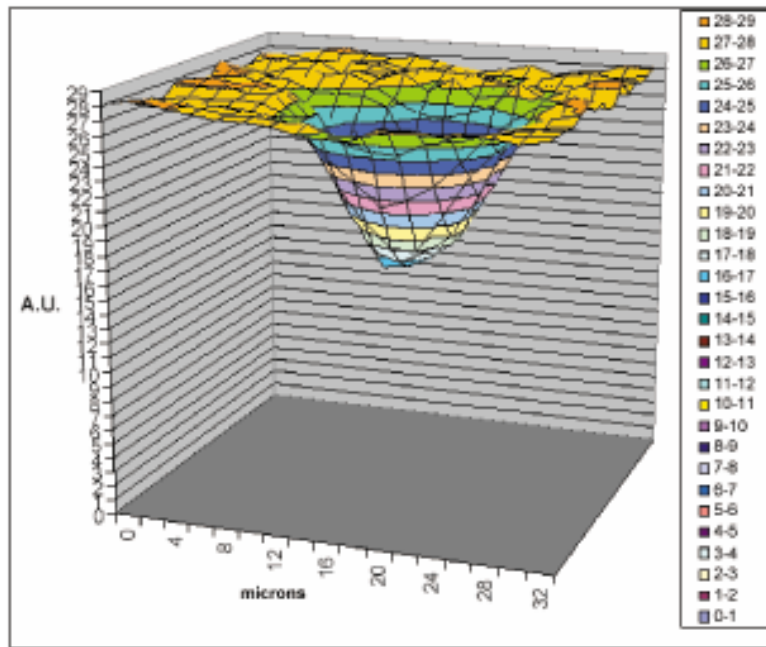
Measured hit position in 3D sensor plane #3 vs. predicted position from beam telescope.



**Fitted 3D sensor width = 3,203 μm .
Drawn width = 3,195 μm . Sensor efficiency = 98%. System efficiency less due to DAQ, triggering electronics.**

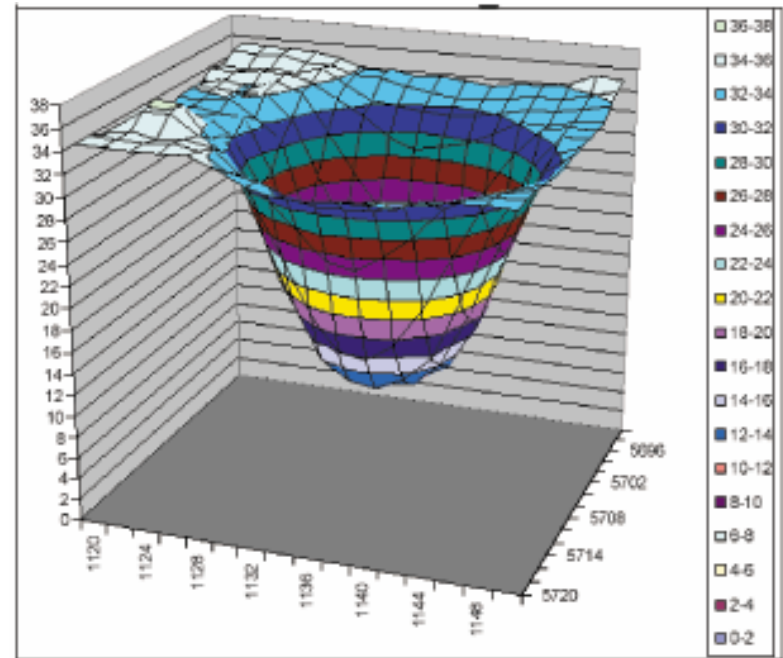
Where is the remaining 2% gone? Electrode efficiency (ALS X-Rays)

3D



N – Electrode

Signal Reduction 43%



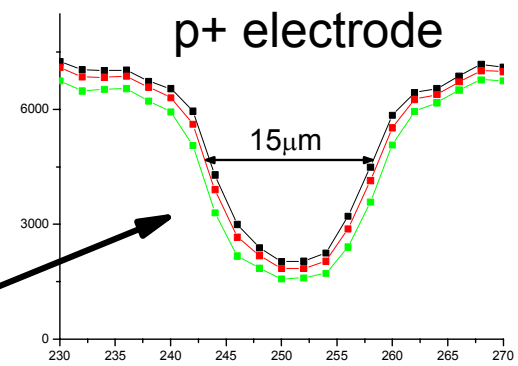
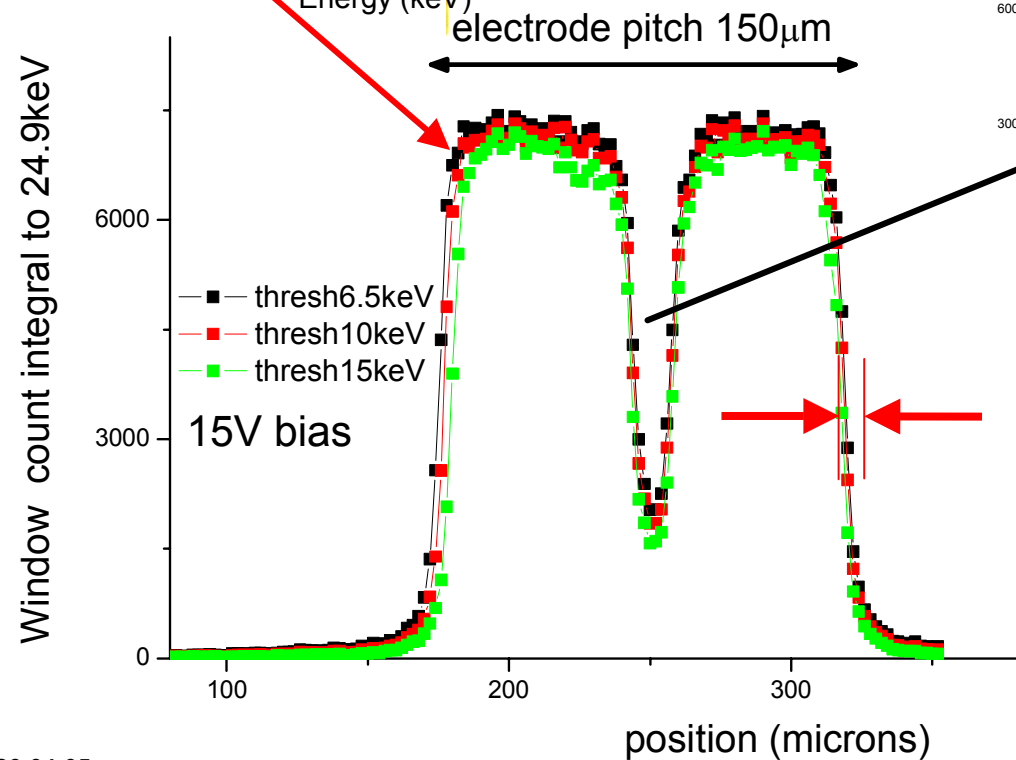
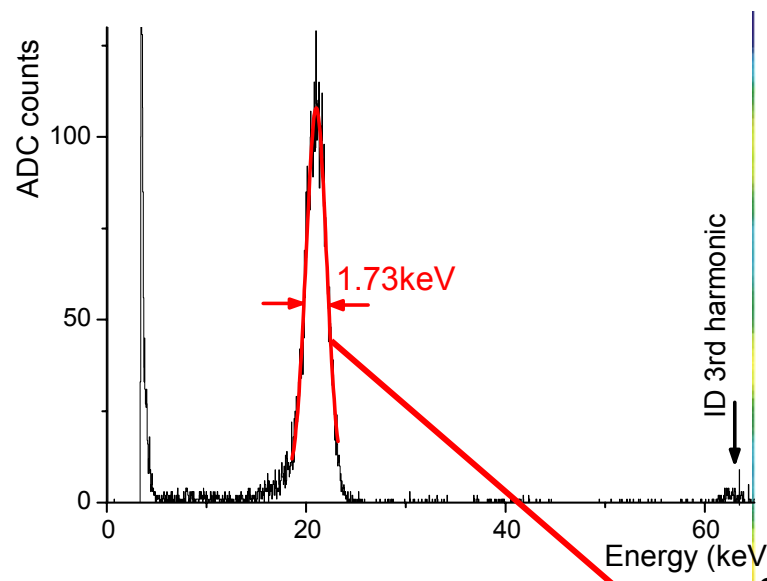
P – Electrode

Signal Reduction 66%

Differences between N and P:

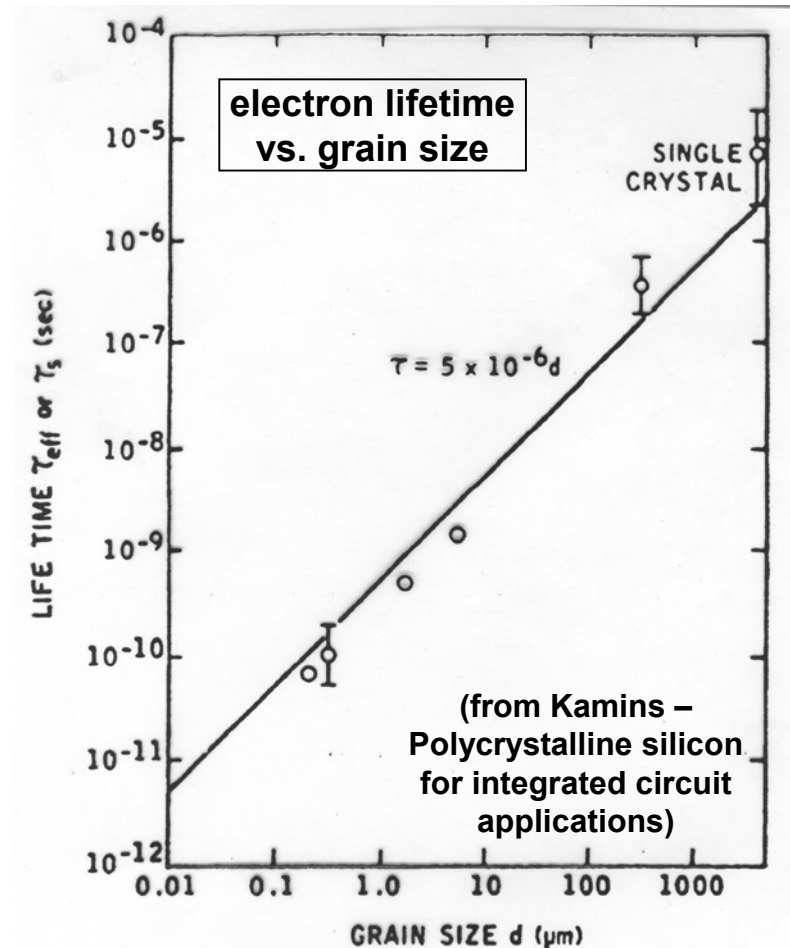
Grain size of poly, Diameter, Diffusion rate, Trapping, Doping

linescan through p+ electrode column and across active edge



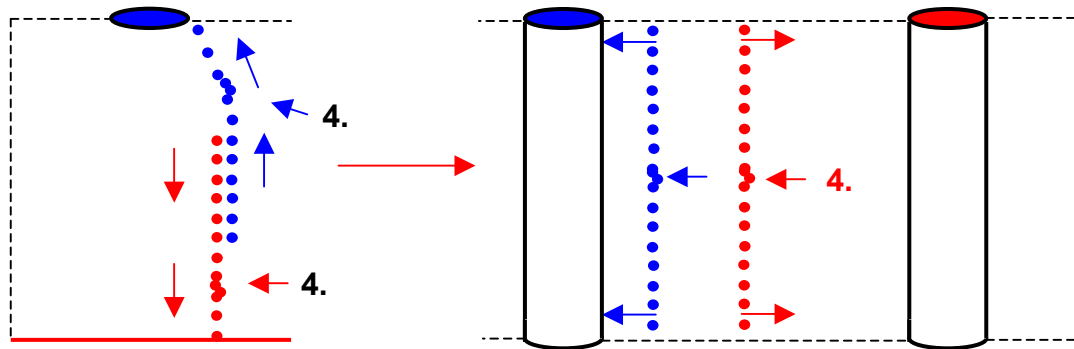
Some possible sources of the observed differences in collection efficiencies seen from n and p electrodes:

1. Differences in electrode diameters and thermal history (increased Dt increases dopant diffusion distances and radius of built-in fields, and can increase grain sizes – the N electrodes were done first).
2. The dopant gasses available at SNF produce an oxide layer on the hole surface which remains after the hole is filled; they may differ in radii and effectiveness as barriers.
3. Electrons and holes have different diffusion rates and lifetimes in the poly electrodes.
4. Note: The CERN -- X5 beam test data shows counts, not signal heights, and discrimination levels will affect the results.



Speed: planar → 3D

3D



1. 3D lateral cell size can be smaller than wafer thickness, so → 1. shorter collection distance
2. in 3D, field lines end on cylinders rather than on circles, so → 2. higher average fields for any given maximum field (price: larger electrode capacitance)
3. most of the signal is induced when the charge is close to the electrode, where the electrode solid angle is large, so planar signals are spread out in time as the charge arrives, and → 3. 3D signals are concentrated in time as the track arrives
4. Landau fluctuations along track arrive sequentially and may cause secondary peaks (see next slide) → 4. Landau fluctuations arrive nearly simultaneously
5. if readout has inputs from both n+ and p+ electrodes, → 5. drift time corrections can be made
6. for long, narrow pixels and fast electronics, → 6. track locations within the pixel can be found

Electrostatic simulations for the design of silicon strip detectors and front-end electronics

R. Sonnenblick, N. Cartiglia, B. Hubbard, J. Leslie, H.F.-W. Sadrozinski and T. Schalk
Santa Cruz Institute for Particle Physics, University of California, Santa Cruz, CA 95064, USA

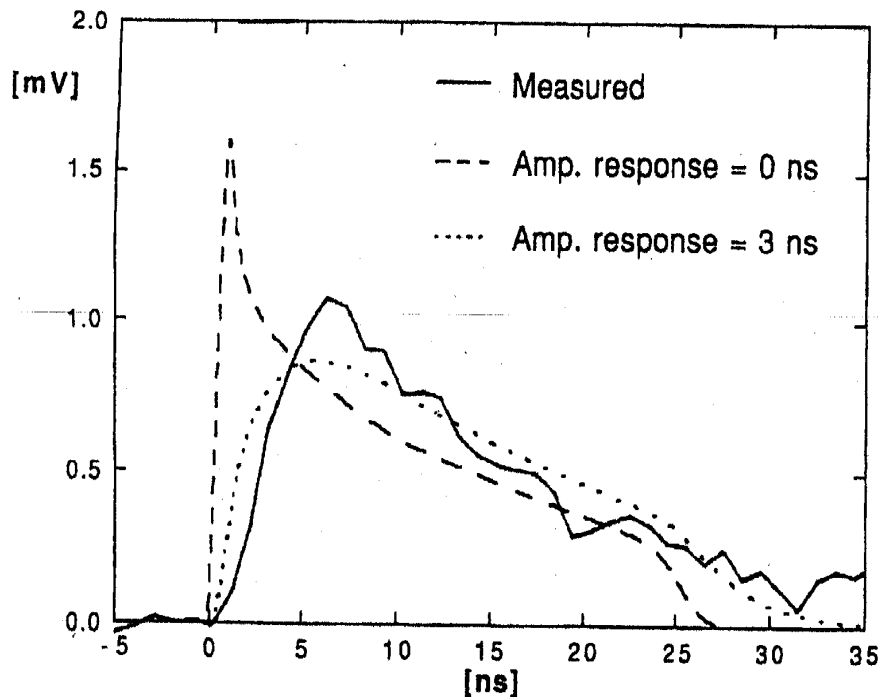


Fig. 3. Pulse shape at the junction side from a minimum ionizing particle. The three curves are the simulated current (with initial diffusion), the simulated current convoluted with the preamplifier response, and a typical observed pulse, respectively.

0.13 μm chips now fabricated – rise, fall times expected to be ≈ 1.5 ns

A high-speed low-noise transimpedance amplifier in a 0.25 μm CMOS technology

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Nicolas Pelloux^a, Shahyar Saramad^{b,c}

rise times ≈ 3.5 ns

fall times ≈ 3.5 ns

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^c Institute for Studies in Theoretical Physics and Mathematics (IPM), Tehran, Iran, P.O. Box 19395-5531

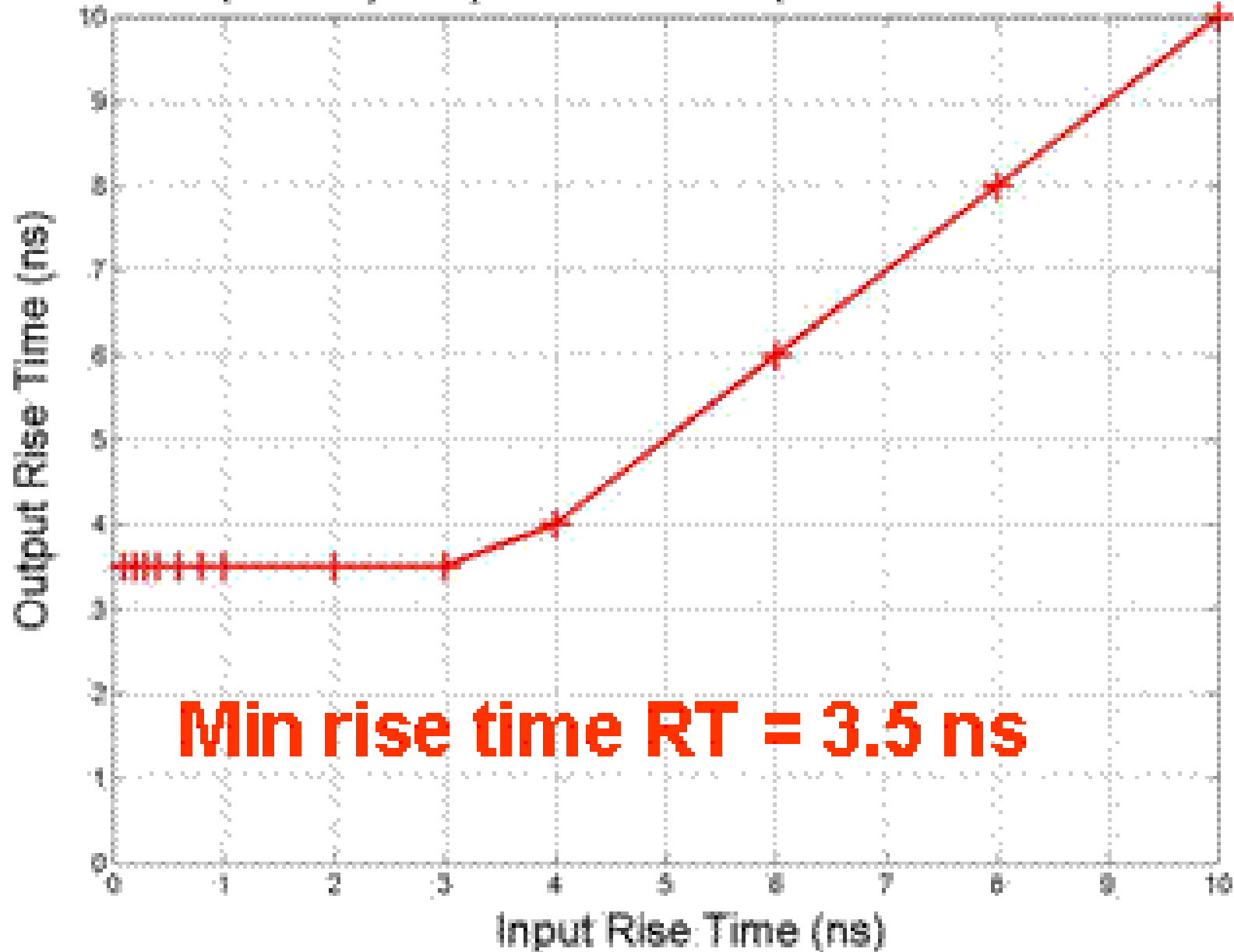
Elsevier use only: Received date here; revised date here; accepted date here

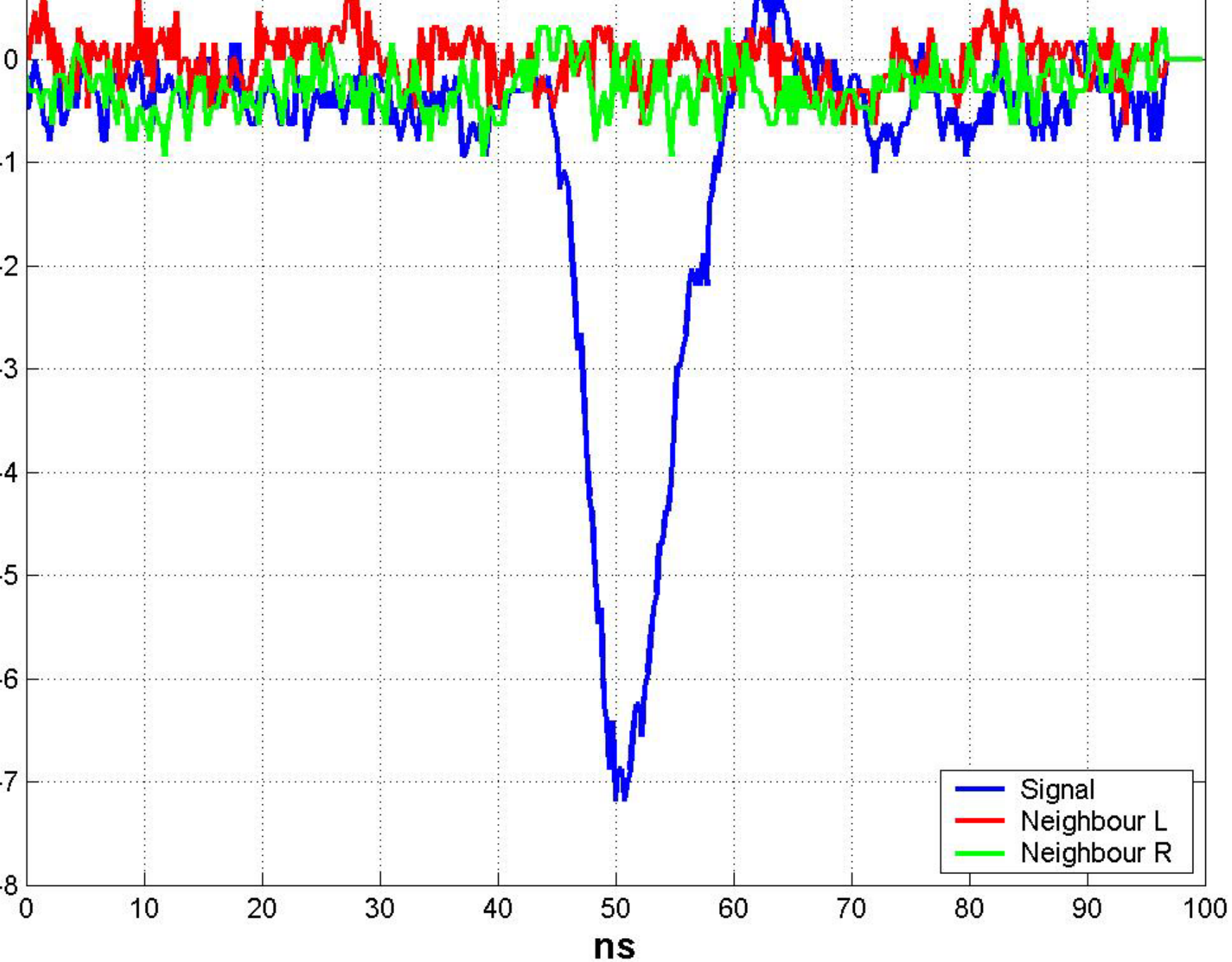
Abstract

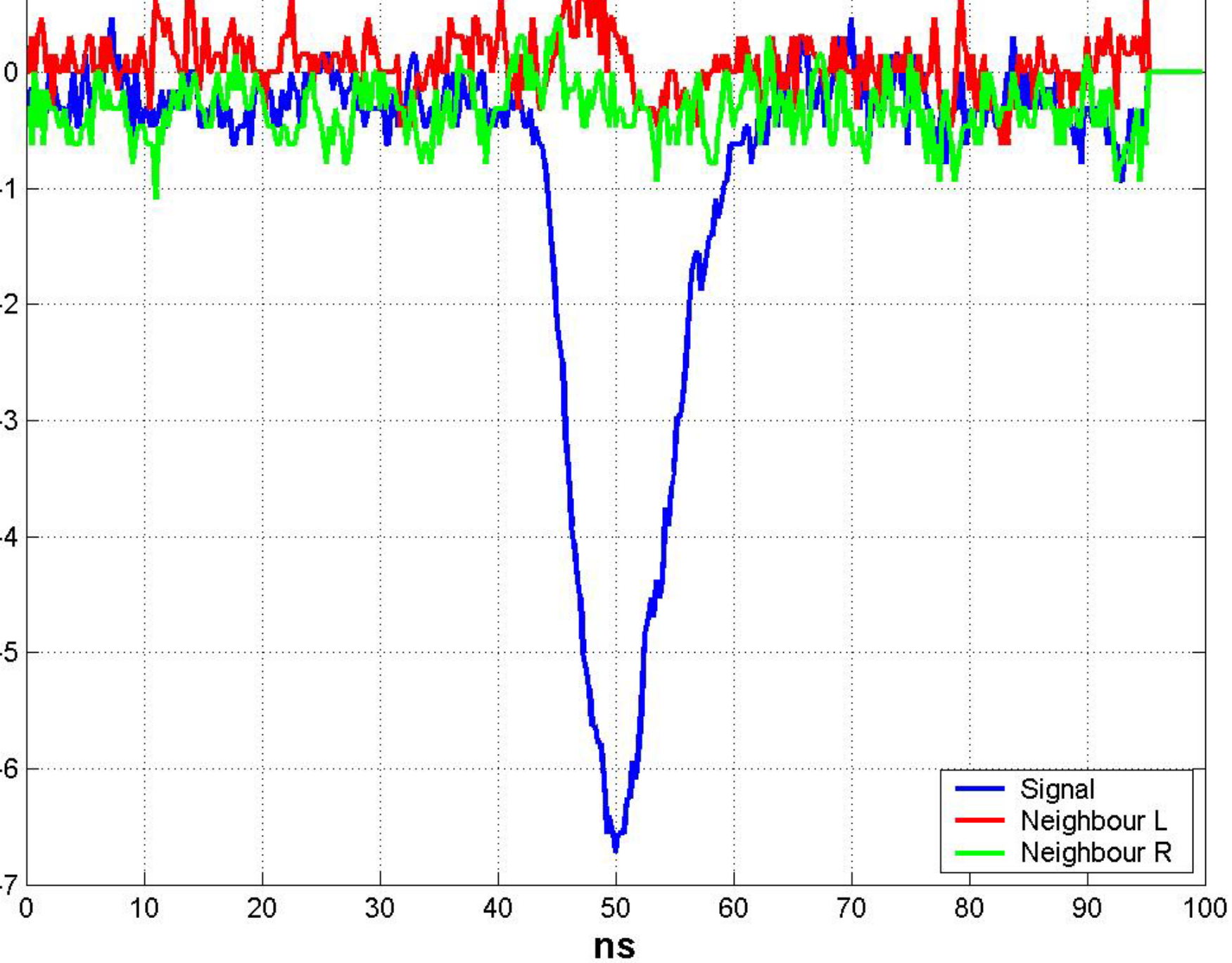
We present the simulated and measured performance of a transimpedance amplifier designed in a quarter micron CMOS process. Containing only NMOS and PMOS devices, this amplifier can be integrated in any submicron CMOS process. The main feature of this design is that a transistor in the feedback path substitutes the transresistance. The circuit has been optimized for reading signals coming from silicon strip detectors with few pF input capacitance. For an input charge of 4 fC, an input capacitance of 4 pF and a transresistance of 135 k Ω , we have measured an output pulse fall time of 3 ns and an Equivalent Noise Charge (ENC) of around 350 electrons rms. In view of a utilization of the chip at cryogenic temperatures, measurements at 130 K have also been carried out, showing an overall improvement in the performance of the chip. Fall times down to 1.5 ns have been measured. An integrated circuit containing 32 channels has been designed and wire-bonded to a silicon strip detector and successfully used for the construction of a high-intensity proton beam hodoscope for the NA60 experiment. The chip has been laid out using special techniques to improve its radiation tolerance, and it has been irradiated up to 10 Mrd (SiO₂) without showing any degradation in the performance. © 2002 Elsevier Science. All rights reserved

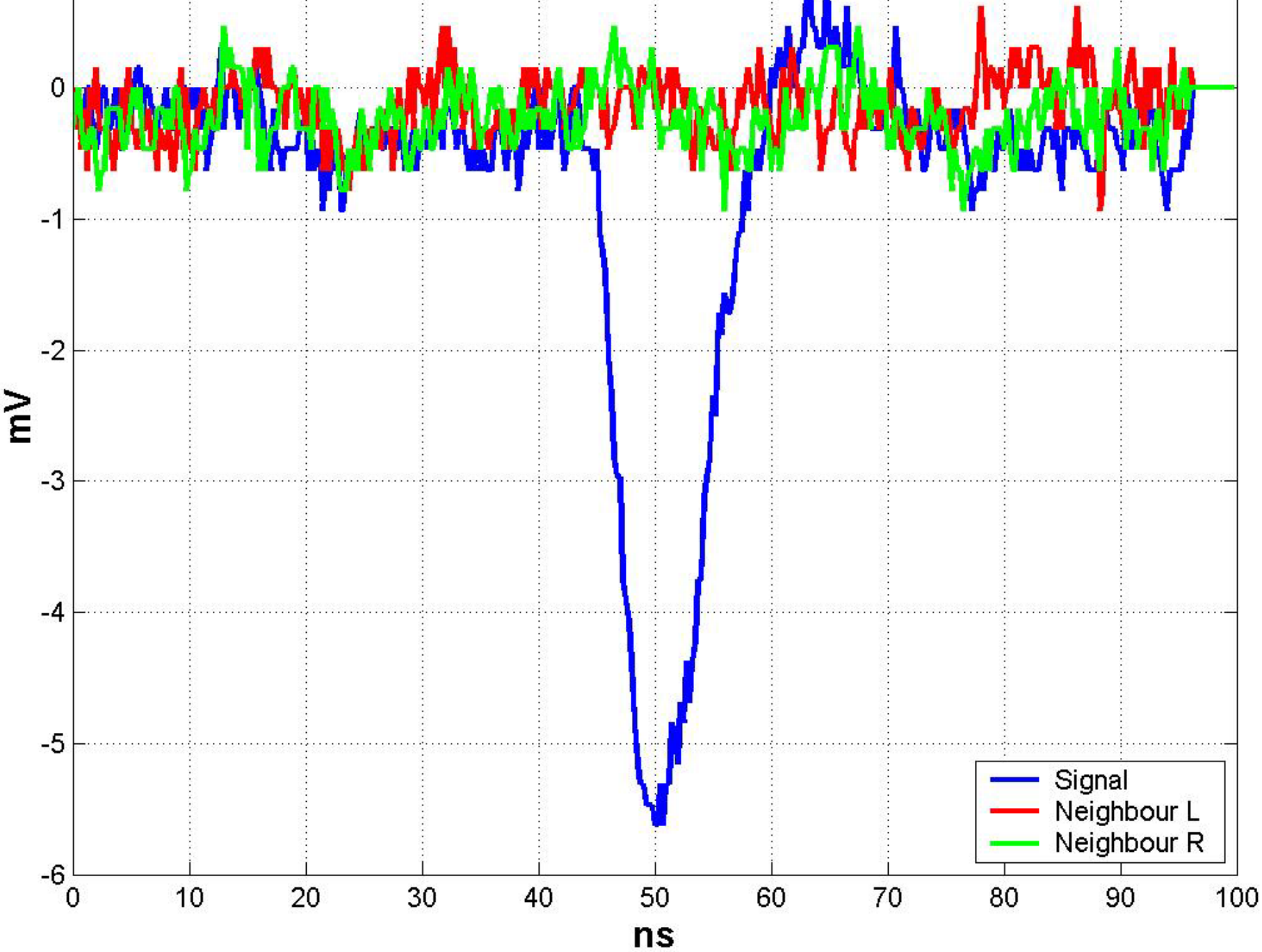
Keywords: Deep submicron; CMOS; Transimpedance amplifier; Radiation tolerance; Low temperature CMOS

Input Output Speed relationship of Electronics RT

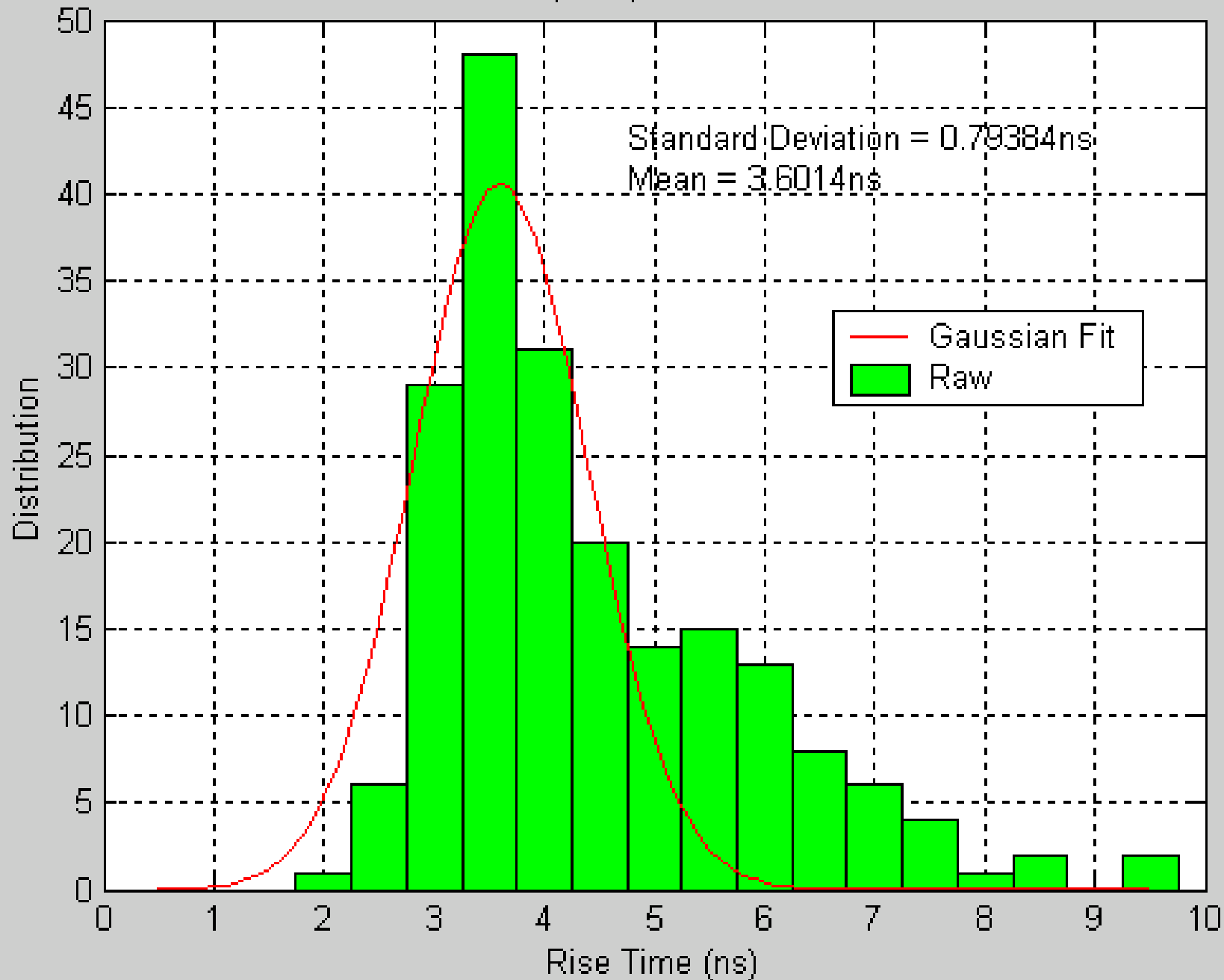




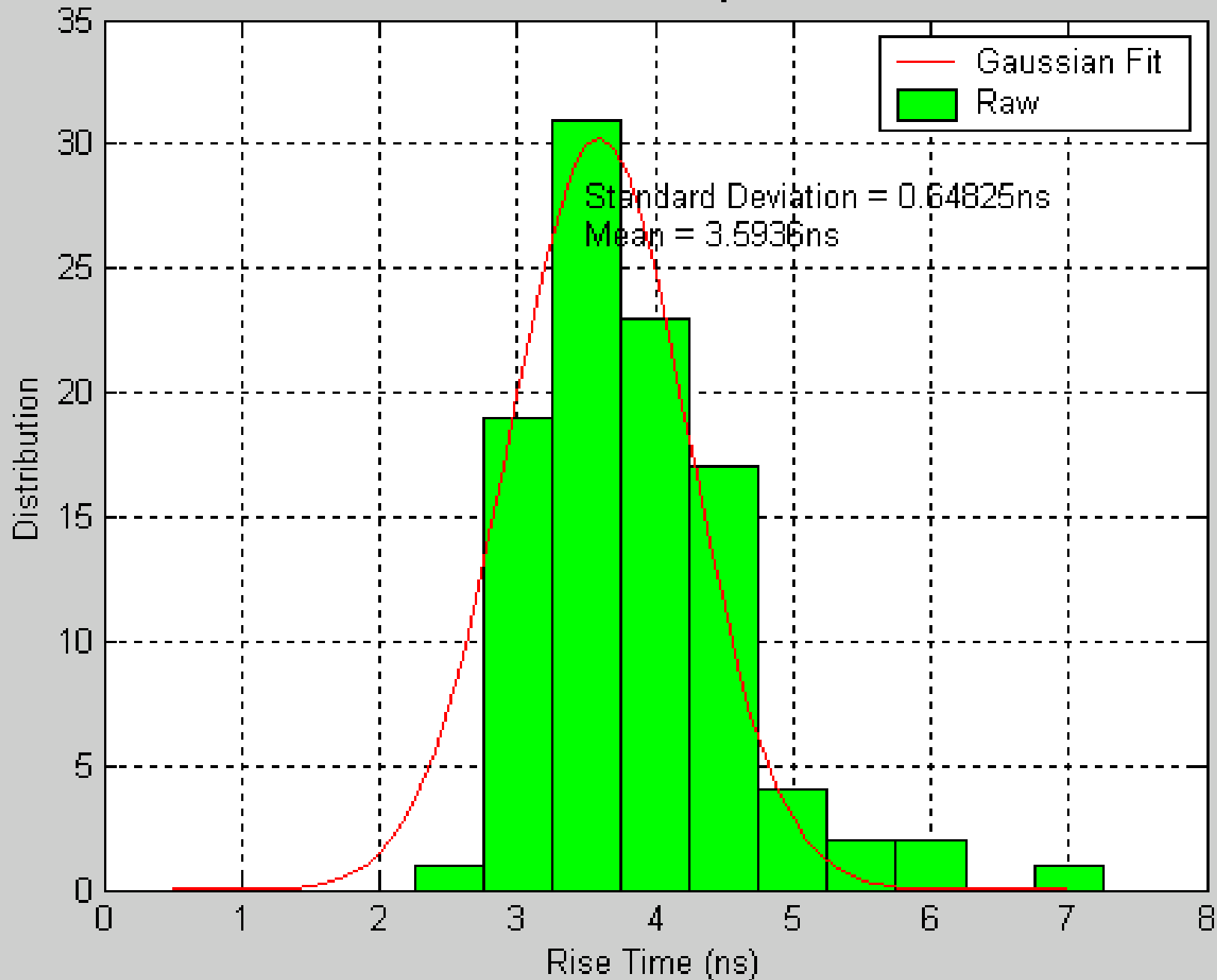




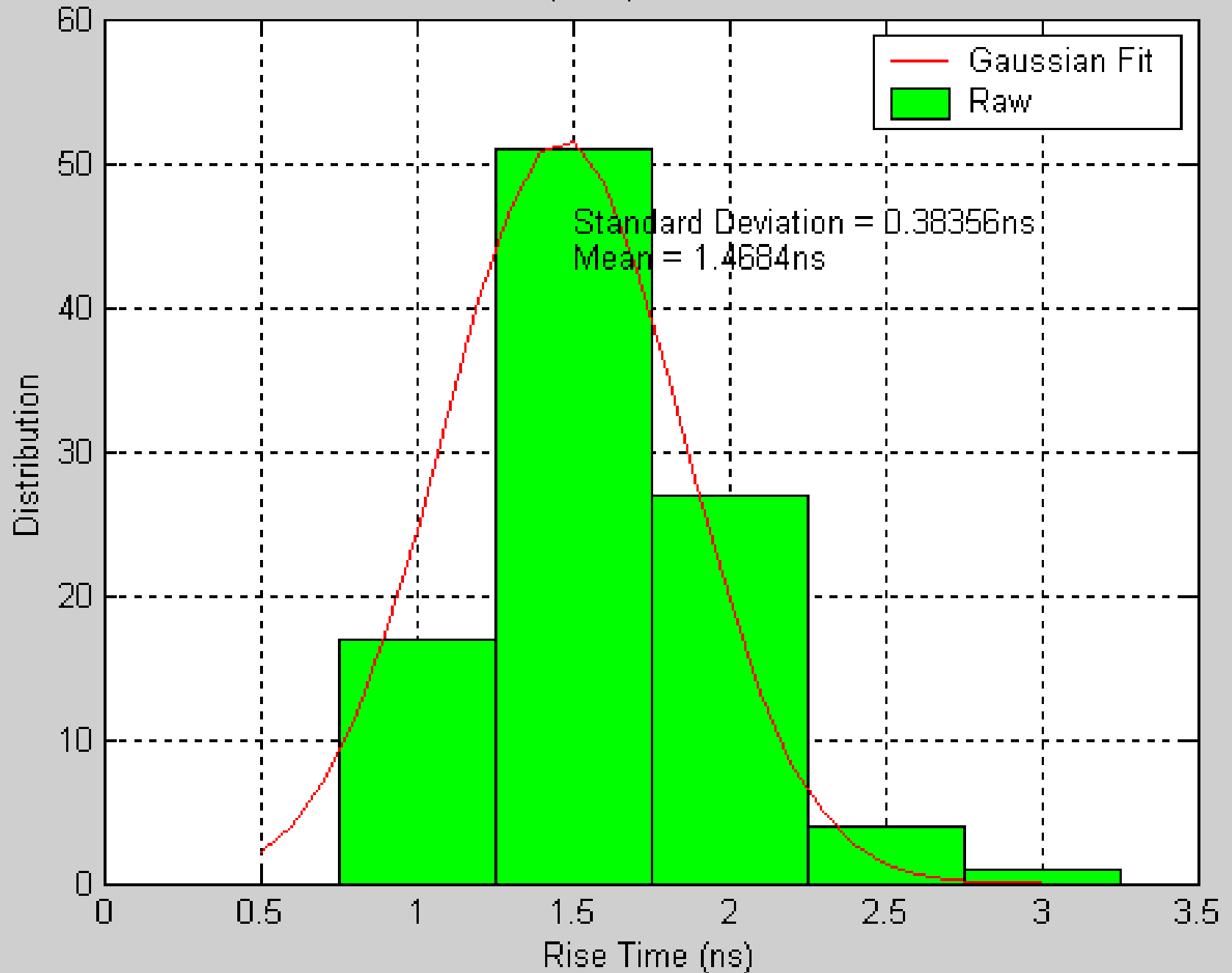
Sr(Beta) 40V 300k



1ns Rise Time Input 300k

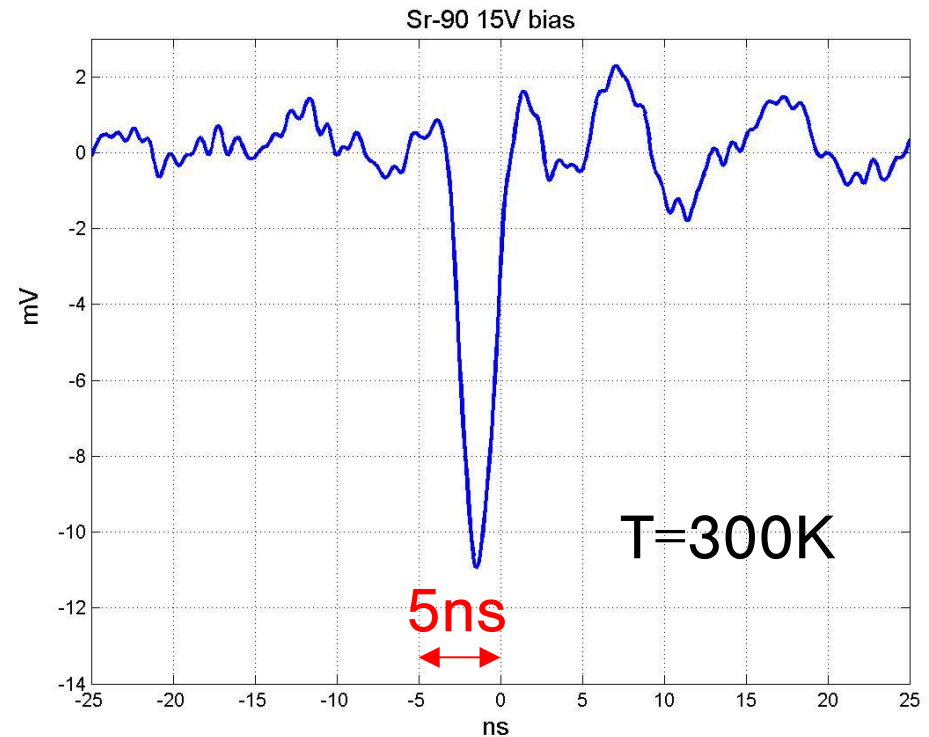
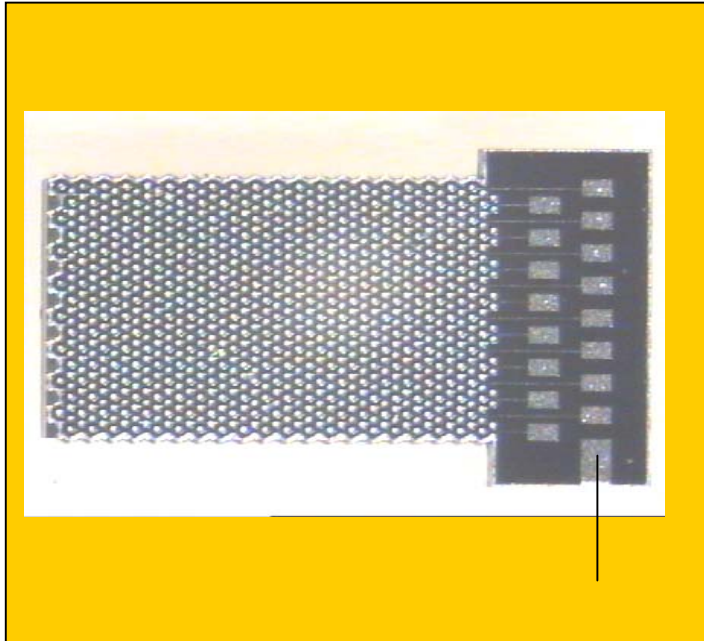


Sr(Beta) 40V 130k



3D Tests in progress with a 0.13 μm CMOS Amplifier chip (designed by Depeisse-Anelli-CERN MIC)

3D



3D Inter-electrode
distance = 50 μm
Expected response
– 2 ns

Yield



- **First exploratory fabrication runs had multiple copies of many types of small sensors – so yield was not a problem.**
- **Now we need larger sensors and so have started to add yield enhancement steps:**
- **Inspect wafers after every lithography step. Remove resist and repeat the photoresist application if necessary.**
- **For the thick trench-etch resist, cover any defects with polyimide tape.**
- **After the trenches are filled with polycrystalline silicon, etch it off the top surface, and then repeat the fill and etch procedure again in an effort to better fill the trenches.**
- **Widen the plasma dice lane from 50 microns to 120 microns to avoid mechanical chips.**
- **Use evaporated aluminum instead of sputtered gold for the backside contact.** (planar / 3D active edge sensors only)

Yield steps – results

- **Widening the dicing lane seems to have eliminated chip defects, which were a 25% loss for the first batch.**
- **All the steps together raised the fraction of full-size Totem sensors with $> 99\%$ of their strips good, from $1/28$ to $14/20 = 70\%$.**
- **For full 3D, we plan to develop and test additional yield steps.**

RESULTS: full-sized, 512-strip, planar / 3D active-edge sensors, 60V

	sensor	leakage current (μ A)	strips with defects	% good strips	comments
1	t4 - 4c	0.7	0	100	
2	t4 - 5c	0.8	0	100	
3	t4 - 7c	0.7	0	100	
4	t4 - 4a	0.7	1	99.8	100% at 30V
5	t4 - 5b	0.8	1	99.8	defect is on back
6	t4 - 6c	0.6	1	99.8	
7	t4 - 8b	0.9	1	99.8	
8	t4 - 7a	1.1	2	99.6	
9	t4 - 7b	0.7	2	99.6	
10	t4 - 4b	0.8	3	99.4	100% at 30V
11	t4 - 8a	1.2	3	99.4	
12	t4 - 8c	1.6	3	99.4	
13	t4 - 8d	1.9	3	99.4	
14	t4 - 5d	1.3	>5	99.2	
15	t4 - 7d	0.7	8	98.4	
16	t4 - 4d	1	>10	<98.0	testing stopped at 255
17	t4 - 5a	-	-	-	hole etched through chip
18	t4 - 6a	-	-	-	hole etched through chip
19	t4 - 6b	-	-	-	not tested
20	t4 - 6d	-	-	-	not tested

Conclusions

1. **Expectations for 3D sensors from the initial calculations have been verified:**
 - a. **They are fast. Amplifier-limited rise and fall times of 3.5 ns at room temperature, even after irradiation by 10^{15} / sq. cm. have been measured. (A new 0.13 micron line-width amplifier, with a rise time of 1.5 ns is undergoing initial testing.)**
 - b. **They deplete at low voltages ($\sim 5 - 10$ V) and have wide plateaus for infrared microbeam signals.**
 - c. **Good resistance to radiation damage has been verified. (A sensor not designed for radiation hardness, with no oxygen diffusion, and no beneficial annealing had a signal plateau from 105 V to 150 V for an infrared light beam after irradiation by 10^{15} 55 MeV protons / sq. cm ($\approx 1.8 \times 10^{15}$ 1-MeV neutrons / sq. cm.).**
2. **Outside the center parts of the electrodes, charge collection is efficient: a 14 KeV x-ray line from a 241-Am source fits a symmetric Gaussian with a sigma of 282 eV.**

- 3. Sensors have reasonable leakage currents: about 1 nA / cu. mm. Active edge channels have the same leakage currents as interior ones. (Some recent runs have had higher leakage currents, possibly due to an iron-contaminated furnace tube.)**
- 4. A new feature, active edges, has been developed, bringing full sensitivity to within several microns of the physical edges.**
- 5. A new kind of sensor has been fabricated and tested – planar / 3D. It has standard planar electrodes on the top surface, a single implant on the bottom, and a 3D electrode on its edges which is continuous with the bottom. It has similar edge properties as full 3D sensors with no dead volume anywhere inside, but without the speed or radiation hardness of full 3D.**