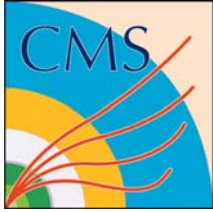


Ideas about Optical Links for Calorimeter Trigger at SLHC



What constraints?

- Detector:
 - Tracker: complete redesign
 - Calorimeter: Detector and front-end unchanged
 - Muons: Minimum change on detector
- Latency (from BX to L1A at front end) $5\mu\text{s}$ max.
- L1A rate $\sim 200\text{kHz}$ max (limited by ECAL VFE)
- See <http://agenda.cern.ch/fullAgenda.php?ida=a043274>
(LECC '04) for more discussion



Constraints



- Trigger (apart from trigger primitives generators) not in a harsh radiation environment
 - Can use commercially available components
- Low latency is critical
 - Latency buffers cost money!
 - Could relax current fixed latency “in-order” L1 trigger, but latency will still be important

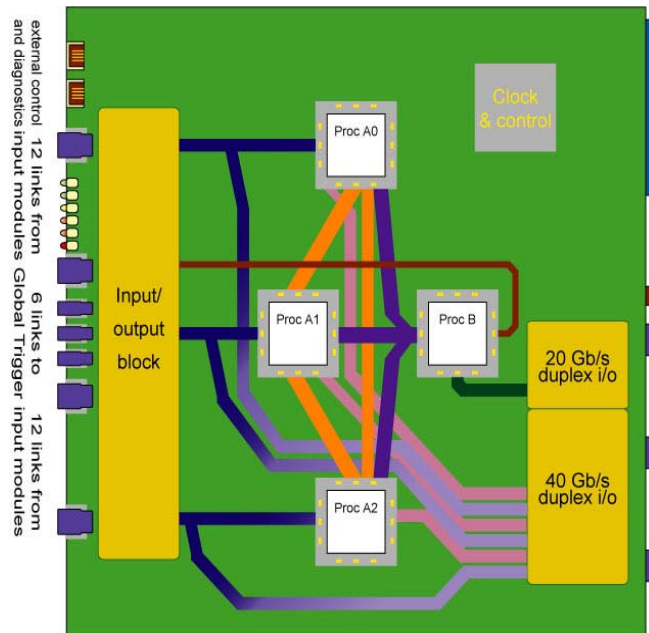


Trigger Links

- Trigger system currently uses copper links
- e.g. GCT receives data from RCT 15metre on parallel 80Mbit/s cables.
- Data flow would increase at SLHC. For many links there is a case for moving to optical.
- Can use commercial systems (e.g. XFP) where possible (but watch latency)

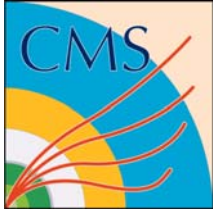


How? (Extrapolate GCT TPM)



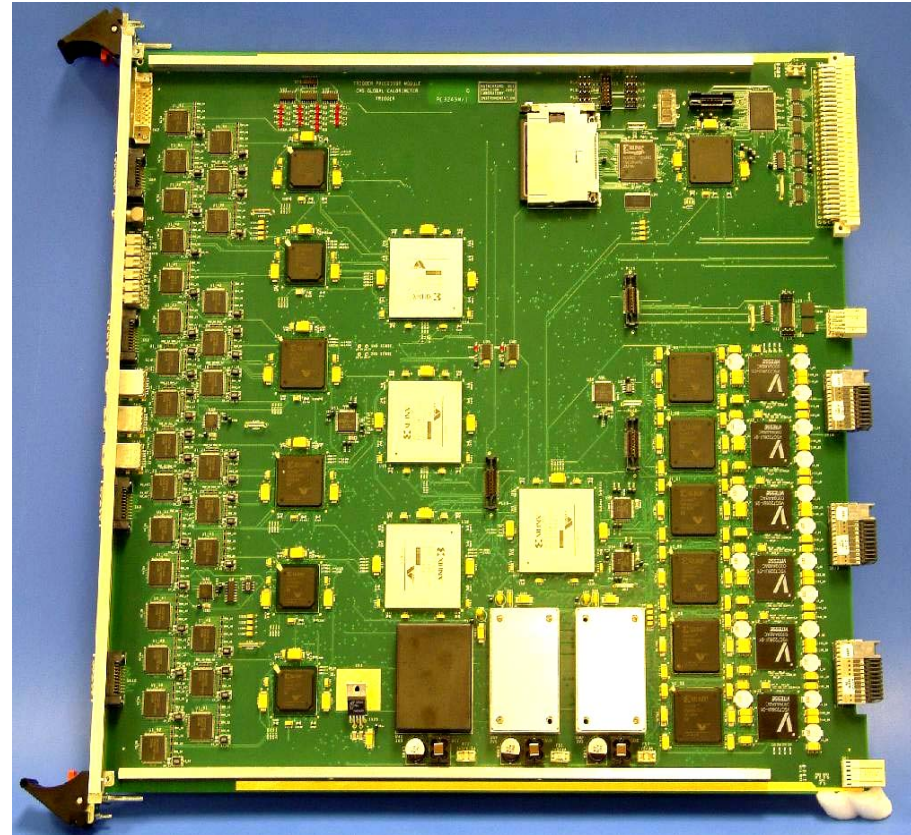
- Based on commercial components for processing and data transfer
- Four processing FPGAs, 3M gates, 14k logic cells
 - Pipelined logic and data transfers clocked at 160 MHz
- 1.44Gbit/s Front-panel I/O
 - 30 Gbit/s input data on 24 links
 - 7.5 Gbit/s output
- 3.2Gbit/s backplane
 - 60 Gbit/s in & out on 24+24 backplane links

Can we extend to a generic trigger processor for SLHC?



TPM design challenges

- Processing technology
 - Xilinx Virtex-II has been very successful
- High-speed data links
 - Serdes choice
 - Connectors and cables
 - Synchronisation
- System issues
 - Configuration
 - Control
 - Power distribution
- Firmware development and management





System Architecture

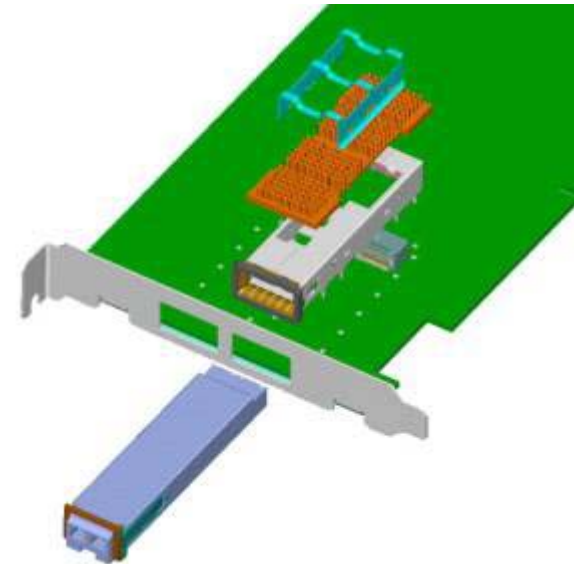


- GCT used a VME 9U based system:
 - Custom power
 - Custom J2/J3
- Move to a telecoms standard? E.g. Advanced TCA?
 - 8U boards
 - 6HP board pitch
 - Defined Gbit/s backplanes.



Front-Panel I/O Extrapolation

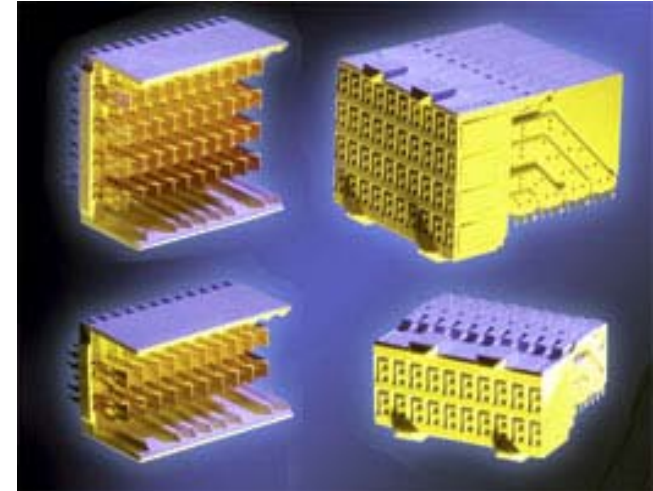
- Use serdes inside processing devices
 - Increase density w.r.t discrete serdes
- Current TPM uses 1.44Gbit/s per pair over Infiniband connectors.
- Use a pluggable system like XFP?
 - 10Gbit/s in 25mm front-panel space. (Can be double sided)
 - Standard fitting on board
 - plug in copper module for up to 1.5m
 - Fibre for inter-crate.
 - Up to 120 Gbit/s on front-panel (240Gbit/s double-sided)

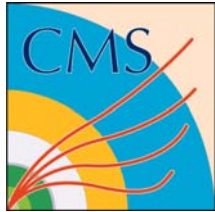




Backplane I/O Extrapolation

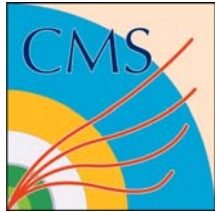
- Currently 3.2Gbit/s per pair over Teradyne VHDM-HSD connectors. (Probably good to ~ 6 Gbit/s)
- 10Gbit/s per pair over backplane with Tyco ZPack HM-ZD connectors. Up to 2Tbit/s per board
 - (c.f. Xilinx demo at SuperComm '04)
 - 9.8 Tbit/s on standard backplane.
16Tbit/s possible with custom backplane





TPM Summary

- System Platform: VME -> AdvancedTCA
- Serial I/O: 1.44Gbit/s / 3.2Gbit/s -> 10Gbit/s
 - I/O per board: 9Gbit/s -> 2TBit/s
- Bus speed: 160Mbit/s.line -> 640Mbit/s.line
 - Number of high-speed lines – try not to increase to much (already 3000)
 - Clocking: system-synchronous -> source-synchronous?



Summary

- Off detector trigger electronics has the luxury of benefiting from the rise of fast serial optical links in industry
 - but watch latency in serializer/deserializers
- Eager to collaborate with other groups (though probably mainly as a consumer)
 - Links need increasingly sophisticated knowledge to design. Move to more “S-LINK” type projects and/or fewer varieties of cable/connectors/....