Radiation Test for the LHC Upgrade (SLHC)

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1. Introduction

The LHC upgrade (SLHC) is being designed to increase the luminosity from $10^{34}cm^{-2}s^{-1}$ to $10^{35}cm^{-2}s^{-1}$. The fluences at the SLHC will be 10 times higher than at LHC. Figure 1 shows the accumulated fluence after two and a half years of SLHC data taking for different parts of the inner detector. For radii greater than 20 cm the expected fluence is 10^{15} cm^{-2}. It is not clear, if the current opto-electronic components of the inner detector readout system are able to cope with this challenging radiation environment of SLHC.

Previous radiation tests have shown that the opto-electronic components (VCSELs, PINs and fibres) can survive 10 years of LHC operation. Radiation tests by the Pixel group have demonstrated that these components can survive fluences and doses up to a factor of two higher than the SCT values.

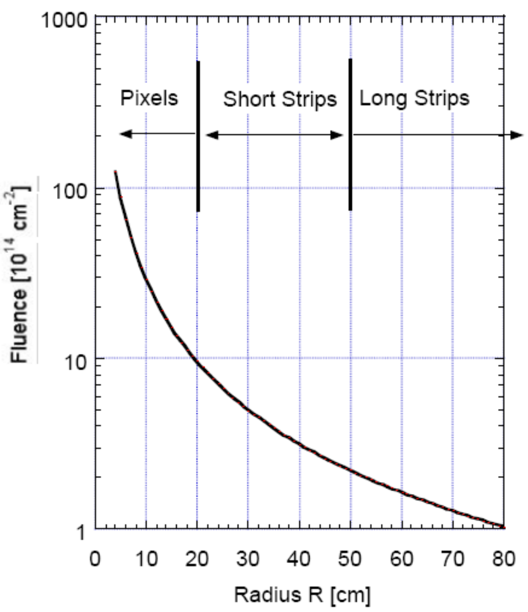

Figure 1: Fluence after 2500 fb^{-1} data taking at SLHC as function of radius [1].

Therefore there is an open question of whether this type of opto-electronics could be used on the upgraded SCT detector at the SLHC. This is a critical question for the design of this detector as it will have a major influence on the layout of all the readout services and therefore needs to be answered before the detector design can advance very far.

The current opto-electronic readout system of ATLAS is operated at 40MBits/sec and it is not using the full bandwidth of 1.6 GBits/sec of what would be possible with this system. Each module is readout by one optical fibre. For the upgraded inner detector it is considerate that depending on the design of the detector more than one module is readout in series by one optical fibre where the readout system is operated at rates in the order of GBits/sec. The bandwidth for readout of six modules in series is estimated to be between 3.4 and 4.8 GBits/sec (see Annex).

The main objective of our near term R&D plans is to determine the performance degradation of the current opto-electronic devices as function of radiation dose (up to 100 Mrad and F ~ n x 10^{15} p/cm^2) and to find out at which doses the devices are damaged fatally. The second objective is to determine the SEU cross section of the devices while operating them at GBits/sec rate.

Devices we will be testing are VCSELs, PIN-diodes, fibres, the driver chip GOL, and Phase-Locked-Loop-IC (QPLL) with the goal to evaluate if these devices are suitable for the inner detector readout for SLHC.

Depending on whether the current devices will fail the SLHC irradiation and SEU tests we would need to explore COTS, try to find more radiation hard components or place the devices at larger radii where they can be operated.

2. Radiation Tests

2.1 VCSELs and PINs (Proton)

Our radiation tests have shown that VCSELs and PIN diodes suffer from bulk damage but are insensitive to surface charge effects. The tests have also demonstrated good agreement with the NIEL scaling hypothesis, so we can use any suitable high intensity hadron beam and scale the results to the hadron spectrum at the LHC. Therefore we need to study these devices in hadron beams.

We propose to use the Indiana University Cyclotron Facility (IUCF) for these tests. The IUCF has been used successfully by our collaborators in Taiwan before and can provide the necessary fluences. We will also investigate the possibility of using neutrons from the Ljubljana research reactor.

We received six pixel VCSELs from Taiwan, which we are currently characterising. We send one of the VCSELs mounted on a PCB board to Ljubljana and will let it irradiate in order to determine its activation. We also received a PIN-Diode testing box from the University of Birmingham with PIN-diode array tiles, which we will use to measure the diode's characteristics after irradiation.

2.1.1 Proposed Radiation Test Programme

The current fluences at the SCT are corresponding to F=1.5*10^{14} protons/cm^2 and scaling them up by a factor of 10 defines the maximum fluence for the proposed radiation tests: **F=(1.5*10^{15} protons/cm^2** (corresponds to 20 hours of beam at IUCF).

For the irradiation studies of VCSELs we will need to perform several cycles of irradiation and annealing as we have demonstrated that nearly full recovery of the VCSEL performance can be achieved with injection annealing (i.e. running the VCSELs with a DC current of 10 to 20 mA). To save beam time we intend to irradiate the VCSELs and PINs at the same time. We intend to irradiate 5 VCSELs and 10 PIN diode arrays (8 diodes) in order to collect statistics.

What to measure: We will measure the light output of the VCSELs and the responsitivity ($R = I_{out}/L_{in}$) of the PINs after each radiation cycle. The necessary test equipment is available.

2.2 SEU Cross Section Measurements (GOL & QPLL)

For the SEU cross section measurements of the optical readout system we need to design a board where we can operate the system at GBits/sec while irradiation. We are planning to adapt the in-house LHCb GOL board for the SEU testing. First discussions with the workshop show that we don’t need to change much on the LHCb board’s design. The SEU-board should be designed by the end of 2005 or begin of 2006. We will have a close collaboration on developing this test system and on irradiation tests with the Southern Methodist University group. We are planning to apply for funds in order to buy a 4 GBits/sec signal analyzer and a high bandwidth optical probe. First SEU tests are expected in 2006.

2.3 Fibres (Gamma)

The radiation damage mechanism in fibre is due to creation of “colour centres” in the electronic levels of the molecules. This is then only sensitive to ionising dose, so can be most conveniently studied with a gamma source. We need a high dose rate gamma source and a large area source to give a uniform dose over the sample. A suitable facility would be the INER, Taiwan.

2.3.1 Proposed Radiation Test Programme

The inner detectors at SLHC have to stand is **100 Mrad**, which corresponds to 200 hours of beam at INER. We intend to irradiate a minimum of 10 fibres.

What to measure: We will measure the induced attenuation of the fibres during irradiation. The necessary test equipment is available.

4. Time Schedule

The gamma and proton irradiation test can be performed in parallel, since they we will be done by Academia Sinica and Oxford Group respectively. We intend to start proton irradiation tests in May 2005, where as the gamma irradiation test can start earlier depending on the schedule of Academia Sinica. 2006 the SEU testing board should be designed and first tests are planned then.

Annex: Bandwidth Estimation for Inner Detector at SLHC

We will estimate in this section the required bandwidth for the SLHC inner detector read out system assuming that

- The granularity of the detector increases by a factor of 6.
- Luminosity increases by a factor of 10.
- Occupancy increases by a factor of 10/6 = 1.66; current occupancy is assumed to be 1%, hence SLHC occupancy is estimated to be 1.66%.
- A module has 1536 strips.
- The average trigger rate is 100 kHz.

Based on these assumptions one SLHC stave is consisting out of 36 upper and 36 lower modules[1]. The estimations made in this paper are upper limits.

Current SCT data format

We will base our estimation on the current data format, which is briefly described below. Figure 1 shows the Module Data Format for one halve of the module.

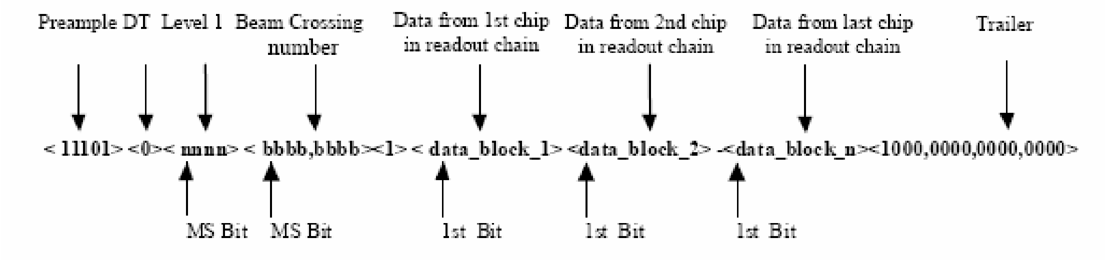

Figure 2: Module Data Format [2]

The Module Data consists out of 2 elements, a 14-bit header, 5 bit preamble, a string of physics data packets, from all the ABCD chips daisy-chained together including the Master ABCD chip and a 16 bit trailer.

The Data Block is the data packet set from each chip including the master chip. This data block can be any of the four following types: Physics Data, No-Hit Data, Error Data or Configuration Data.

For the following we consider the case that the Data Block is Physics Data. There are two types of data packets for the Physics Data: isolated hit packet (Figure 2) and non-isolated hit packet (Figure 3). A physics data packet can consist of any combination of these 2 types of packets.

[1] A SLHC stave is corresponding to 1/2 row of modules on the current SCT detector.

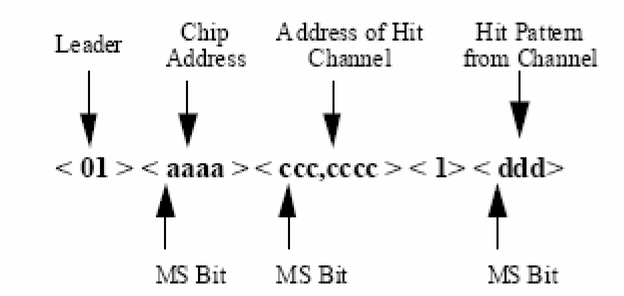

Figure 3: Isolated hit data packet [2] .

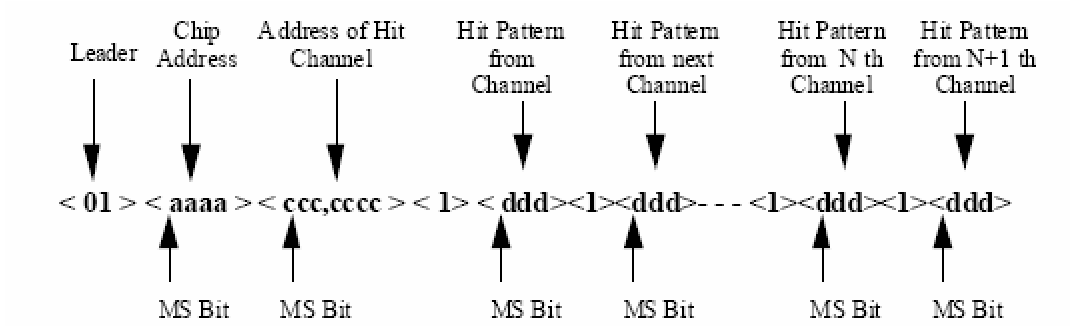

Figure 4: Non isolated hit data packet [2] .

SLHC binary readout (normal data taking mode)

- Preamble + Header + Trailer = 5 + 1 + 4 + 8 + 1 + 16 = 35 bits
- Number of bits for a Isolated hit data packet per hit = 17 bits

Assuming that the occupancy will be 1.66% we will have 25.5 hits per module. For upper limit estimation we assume that all of these hits will be isolated and that each module is sending its own header, preamble and trailer. For a halve stave this results in

Number of Modules:=a	Number of hit channels per module:=b	Number of bits per hit:=c	Sum of Header, Preamble and Trailer:=d	bits to be readout:= B
36	25.5	17	35	16866

Table 1: Number of bits to be read out per level 1 trigger in a binary read out: B = a * (b*c + d).

Assuming we have an average trigger rate of 100 kHz the bandwidth required to read out a halve stave would be 1.68 GBits/sec; including a safety factor of two gives **3.36 GBits/sec**.

SLHC digital readout (normal data taking mode)

For the digital read out I assume that the data information of a hit channel is encoded in 8 bits like in the svx4 chip of Run2b. In order to run the read out in different mode, we need to introduce a mode flag, which shall be 3 bits long. The “Hit Pattern Channel” is replaced by 8 bits, which do encode data signal on the hit channel. Summing this up the number bits per pit increases from 17 to 25 bits.

Number of Modules:=a	Number of hit channels per module:=b	Number of bits per hit:=c	Sum of Header, Preamble and Trailer:=d	bits to be readout:= B
36	25.5	25	35	24210

Table 2: Number of bits to be read out per level 1 trigger in a binary read out: B = a * (b*c + d).

Assuming we have an average trigger rate of 100 kHz the bandwidth required to read out a halve stave would be 2.4 GBits/sec; including a safety factor of two gives **4.8 GBits/sec.**

References

[1] Fred Hartjes, "ATLAS Upgrade for SLHC", NIPHAD Meeting, 11-3-2005
[2] Project Specification, Project Name: ABCD Chip.