R&D Plans for Pixel On-detector Optical Link Upgrade

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Outline

- Current pixel on-detector opto-link
- Upgrade assumptions
- R&D Plans
Inner Detector Optical Links

- **SCT**: ~ 12,000 links, including data transmission redundancy
- **Pixel**: ~ 4,000 links
  - on-detector opto-link designed/constructed by OSU/Siegen
  - collaboration will continue on the upgrade
- **Pixel link** was originally based on SCT design
- **both use driver/receiver of similar architect:**
  - **VDC**: VCSEL Driver Circuit
  - **DORIC**: Digital Optical Receiver Integrated Circuit

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Inner Detector Optical Chips

● SCT:
  ◆ AMS 0.8 µm bi-polar
  ◆ VDC: two channels/chip
  ◆ DORIC: one channel/chip
  ◆ optical package: 2 Truelight VCSELs + 1 Centronic PIN
    ■ use two data links for redundancy
  ◆ speed: 40 Mb/s

● Pixel:
  ◆ IBM 0.25 µm CMOS
  ◆ four channels/chip
  ◆ optical package: 8-channel Truelight VCSEL/PIN arrays
  ◆ speed: 80 Mb/s using both clock rising/falling edges
    ■ B-layer uses two data links to transmit at 160 Mb/s
Optical Link/FE Connections

- **SCT:**
  - use short flex to avoid electromagnetic interference

- **Pixel:**
  - use ~ 1 meter of micro-twist pairs (100 µm)
    - greatly simplify construction
  - 2 BeO board flavors
  - few production problems
Pixel Upgrade Assumptions

● pixel detector will occupy ~ same real estate

● opto-link can operate at same location (PP0)

● pixel size will not decrease significantly
  ♦ use all fibers in 8-fiber ribbon instead of having 1-2 fibers unused
  ♦ can use 12-channel VCSEL/PIN arrays
  ⇒ higher density transmission with small increase in size of fiber ribbon since cladding is a significant contribution

● desirable to preserve Module Control Chip (MCC) architecture instead of starting from scratch
  ♦ preserving current opto-link architecture but operate with higher speed is a viable solution
    ■ transmit data at 1.28 Gb/s with 16 times faster clock is probably adequate for 10 times increase in luminosity
Facilities at OSU

- equipment in new high energy physics clean room:
  - two automatic wire bonders (K&S 1470 and 8060)
  - two manual wire bonders
  - wire-bond pull tester
  - dice probe station
  - high speed scope (6 GHz/20 GS/s)
  - high resolution IR camera
  - optical vision machine (± 3 μm, on order)
  - optical comparator
  - fiber polisher and fusion splicer
  - high power UV light source
  - precision scale (± 0.1 mg)
Cable R&D Plans

● Can ~ 1 meter micro-twisted pair transmit data at Gb/s?
  ◆ If not, what is minimum diameter?
    ■ status: wires acquired and test setup under construction

● Pixel opto-link has few meters of rad-hard pure silica core
SIMM fiber spliced to rad-tolerant GRIN fiber
  ◆ SIMM: low bandwidth
  ◆ GRIN: intermediate bandwidth
    ■ Can the fiber transmit data at Gb/s?
  ◆ status: fibers acquired and waiting to be spiced
    and mounted with MT connectors for testing
Chip R&D Plans

● convert VDC and DORIC to operate at Gb/s:
  ✦ status: completed conversion of schematics from 0.25 to 0.13 µm library
    ⇒ need to improve speed etc.
    ⇒ layout prototype chips, simulate, submit, test, irradiate
      ■ 3-year program?

● producing enough voltage to drive VCSEL is a challenge:
  ✦ Truelight VCSEL needs ~1.9 V to produce 10 mA
    ■ higher current is needed for efficient annealing
  ✦ operating voltage of 0.13 µm chip is 1.2 V
    ■ thick oxide can operate at 2.5 V
    ⇒ need to test irradiation hardness of thick oxide chip
Summary

- continue use of VCSEL/PIN arrays but operate at 1-2 Gb/s is a possible upgrade scenario
- design of high-speed driver/receiver will be a major challenge