Optical Link Driver/Receiver R&D for SLHC Pixel Detector

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The optical link of the pixel detector uses a VCSEL Driver Chip (VDC) to drive a VCSEL and a Digital Optical Receiver Integrated Circuit (DORIC) to decode the signal received at a PIN diode. The VDC converts an LVDS signal into a single-ended signal appropriate to drive a VCSEL and the DORIC decodes the bi-phase marked encoded signal to extract the 40 MHz clock and command. The pixel chips are rad-hard versions of those used in the strip detector, SCT. The pixel detector uses 8-channel PIN and VCSEL arrays.

A natural upgrade path for the optical link is to drive the VCSEL and PIN at higher speed since the diodes are rated at Gb/s. For example, operating the VCSEL at 16 times the 40 MHz clock will allow transmission rate of 1.28 Gb/s, using both edges of the clock. The use of a 12-channel VCSEL/PIN array would allow 50% higher data transmission with no significant increase in space required for the optical cables given that the cable volume is dominated by the protective shielding.

The above upgrade path will preserve much of the architect of the current pixel electronics. This takes advantage the many years of development in the front-end chip, MCC (Module Control Chip), and optical chips. Any new optical link that requires major overhauls of the front-end chip or MCC is probably not practical or desirable.

Commercial drivers and receivers are capable of operating at Gb/s. The supply voltages are all at 3.3 V which implies that the chips are fabricated using 0.8 μm technology. We need to develop new chips using 0.13 μm technology, probably with enclosed layout transistor and guard rings to enhance the radiation hardness. Unfortunately, the nominal operating voltage is 1.3 V, which is inadequate to drive a VCSEL. The thick oxide option has a nominal supply voltage of 2.5 V and this must be used in the driver design. By developing the chips using the same technology as the front-end chip and MCC will allow submissions of prototype and production chips in the same run for cost saving as in the present development of the optical chips.

We developed the VDC and DORIC chips using 0.25-μm technology in collaboration with Siegen University. The plan is to continue this collaboration for the new chips.