Irradiation of SiGe Bipolar Transistors as part of the RD50 Common Project Oct. 2004 Run

D.E. Dorfan, A. A. Grillo, J. Metcalfe, M Rogers, H. F.-W. Sadrozinski,
A. Seiden, E. Spencer, M. Wilder
SCIPP, UC Santa Cruz, CA 95064,USA
A. Sutton, J.D. Cressler
Georgia Tech, Atlanta, GA 30332-0250, USA

Bipolar circuits using SiGe technology have potential advantages
when compared with CMOS for fast shaping times and large capacitances.
Thus they are good candidates for the technology choice of the frontend
of readout ASICs for the silicon strip detectors planned for the LHC upgrades,.
.
In the inner detector layers, pixel detector will be needed, and their small capacitances
allows the use of deep sub-micron CMOS as an efficient readout technology.

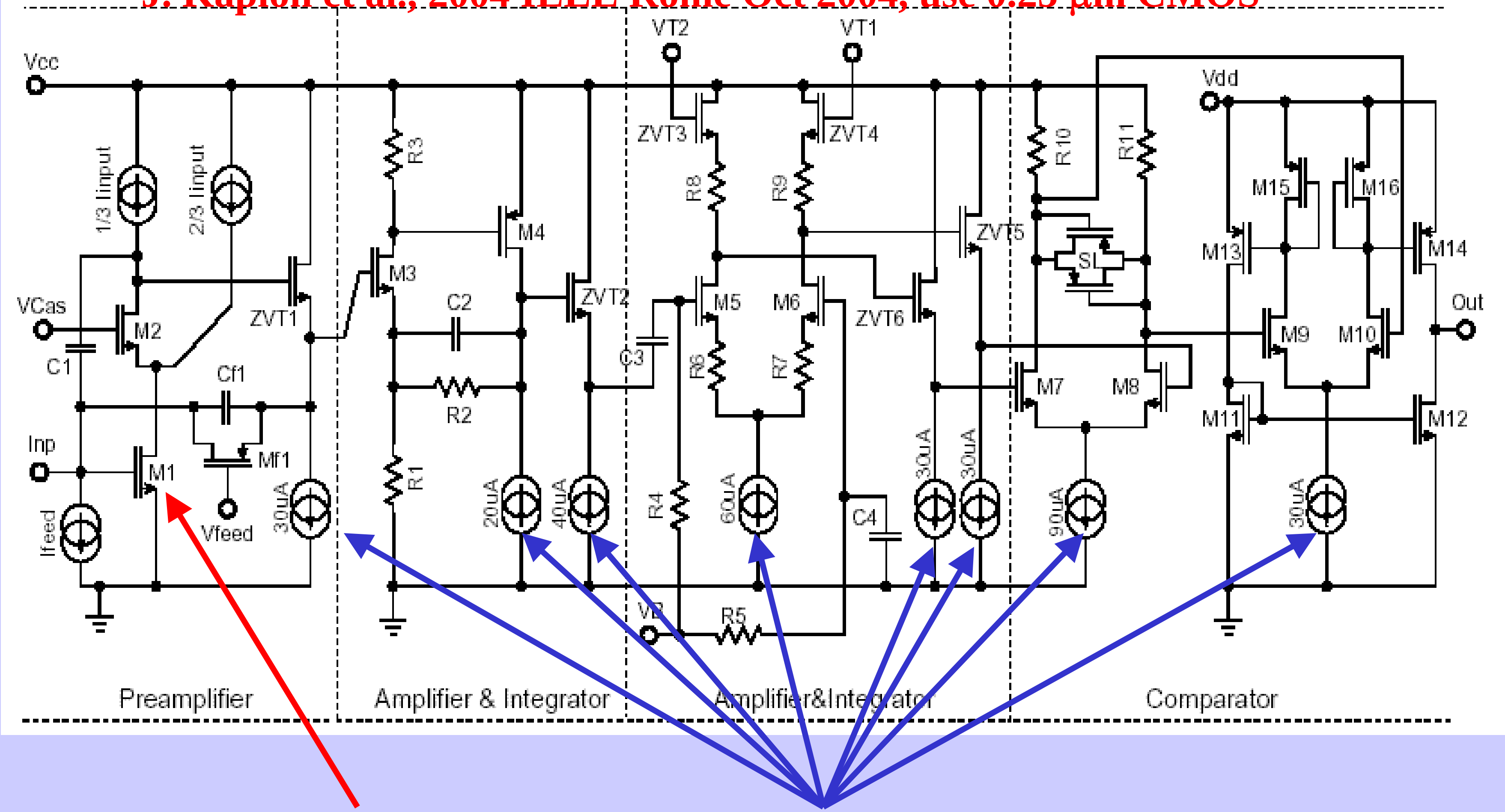
Starting at a radius of about 20 cm, at fluence levels of 10^{15} n/cm^2, short strips can be used,
with a detector length of about 3 cm and capacitances of the order of 5 pF.
At a radius of about 60 cm, the expected fluence is about a few times 10^{14} p/cm^2,
and longer strips of about 10 cm and capacitance of 15 pF can be used.

In the two outer regions where bipolar SiGe might be used in the front-end readout ASICs,
power savings and fast shaping to identify the beam bucket are important requirements.

The analog section of an amplifier for silicon strips typically has a special front transistor,
selected to minimize noise (and often requiring a larger current than the other transistors)
and a large number of additional transistors used in the shaping sections
and for signal-level discrimination.

Architecture of the Front-End channel

J. Kaplon et al., 2004 IEEE Rome Oct 2004, use 0.25 µm CMOS



For CMOS: Input transistor: 300 µA, other transistors 330 µA (each 20 – 90 µA)

Transistor Sizes and measured Current Gain β:
(modified IBM 5HP process)

Fluence: 1.34E15 p/cm^2
I_c=150μA

Transistor Size μm^2	β_{pre}	β_{irrad}	partial β_{anneal}
0.5x1	200	80	105
0.5x2.5	270	65	89
0.5x10	258	40	73
0.5x20	260	28	52
4x5	325	51	83

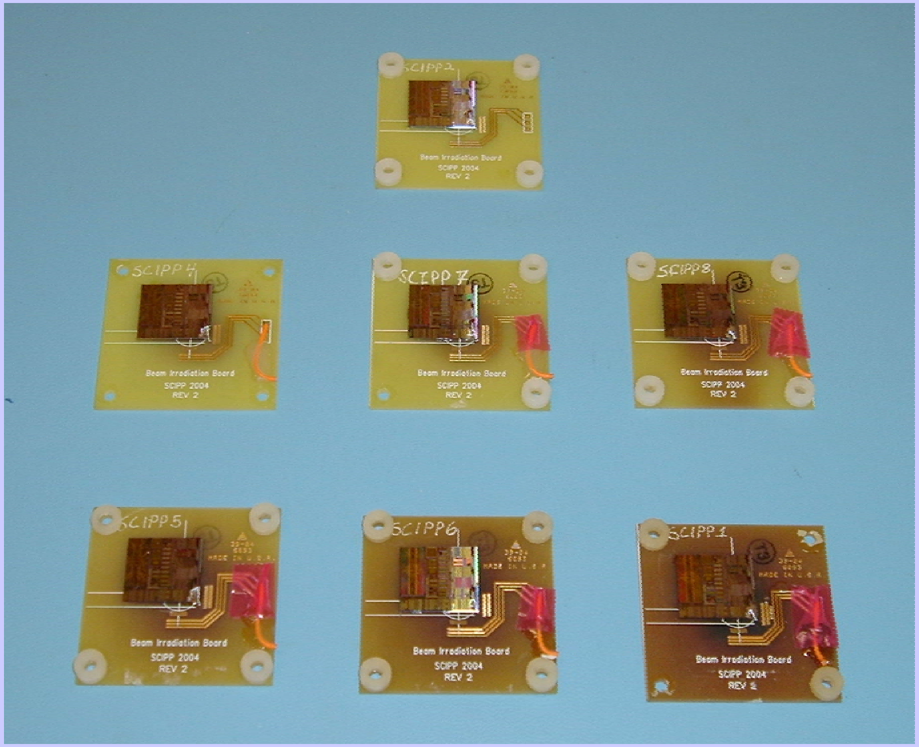
Large β

Degradation of β Geometry dependent?

See below

Strong Annealing

The irradiations were performed in October 2004 at CERN with 24 GeV protons as part of the common RD50 project.
Special thanks to Michael Moll and Maurice Glaser

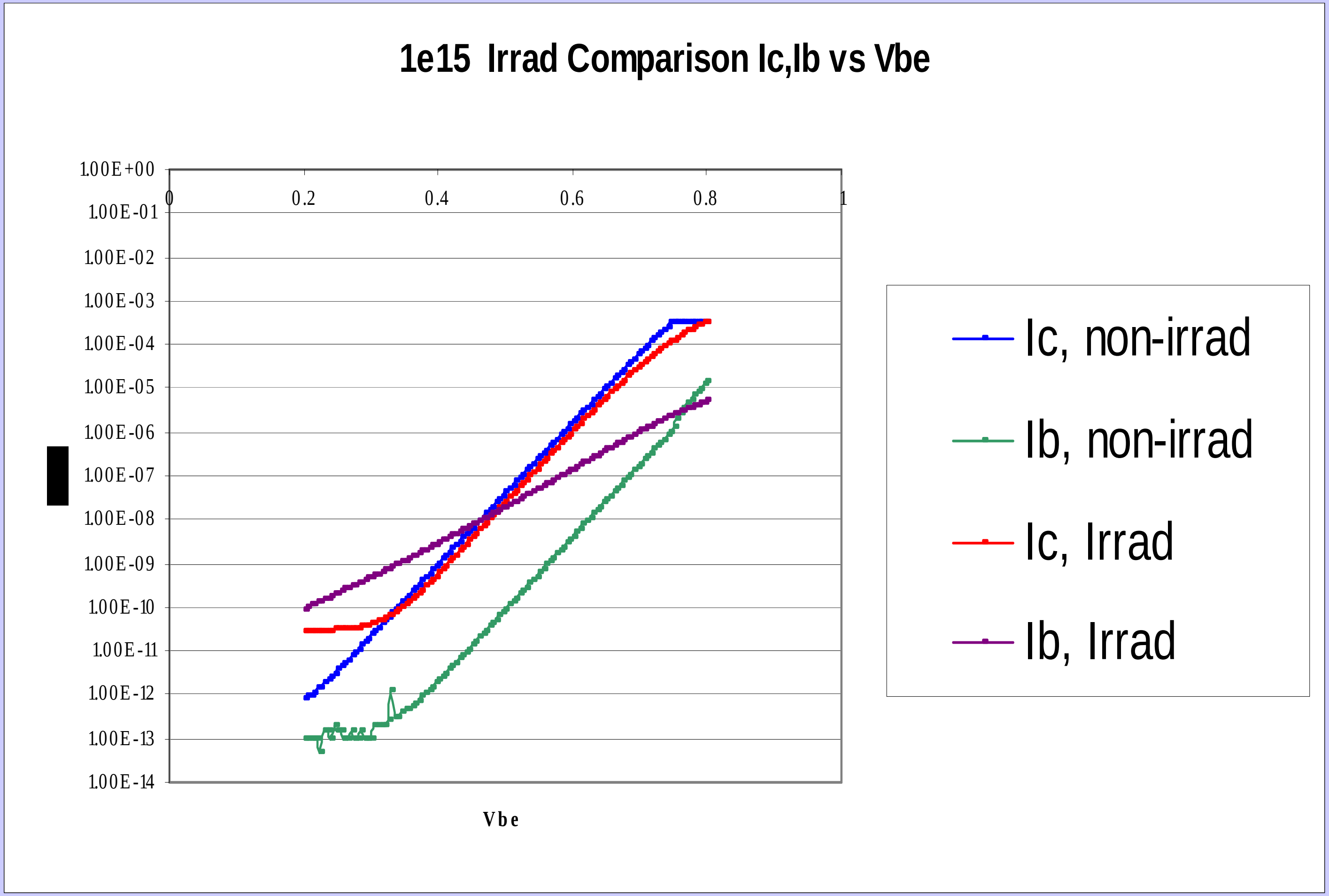


The following fluences (p/cm^2) were reached:

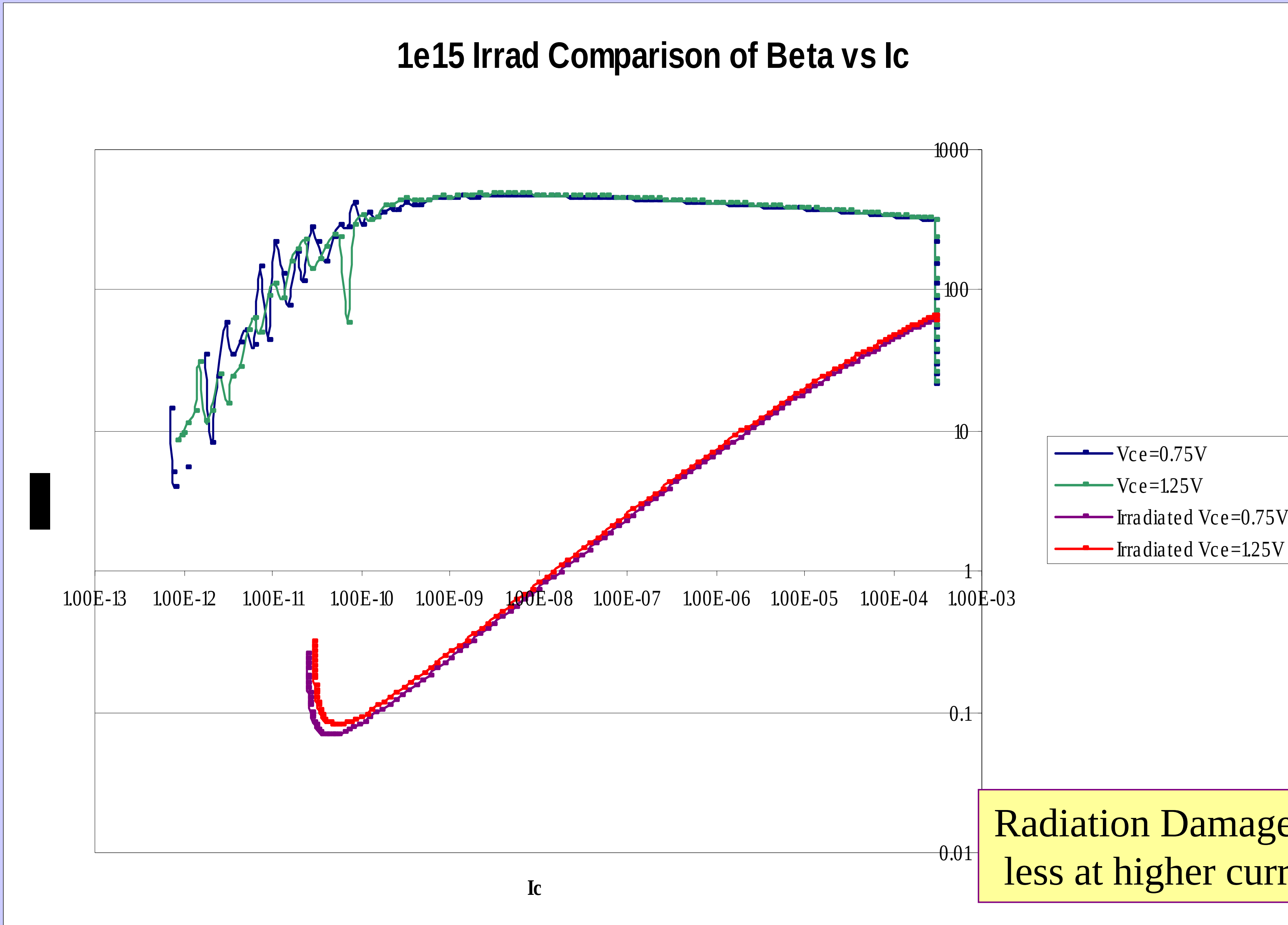
4.15×10^{13} 1.15×10^{14} 3.50×10^{14} 1.34×10^{15} 3.58×10^{15} 1.05×10^{16}

The discoloration highlights the damage caused by the proton beam.

Gummel Plot for 0,5 x 2.5 pre and post-rad 1.3×10^{15} p/cm.
(The ratio of I_c / I_b is the current gain β)

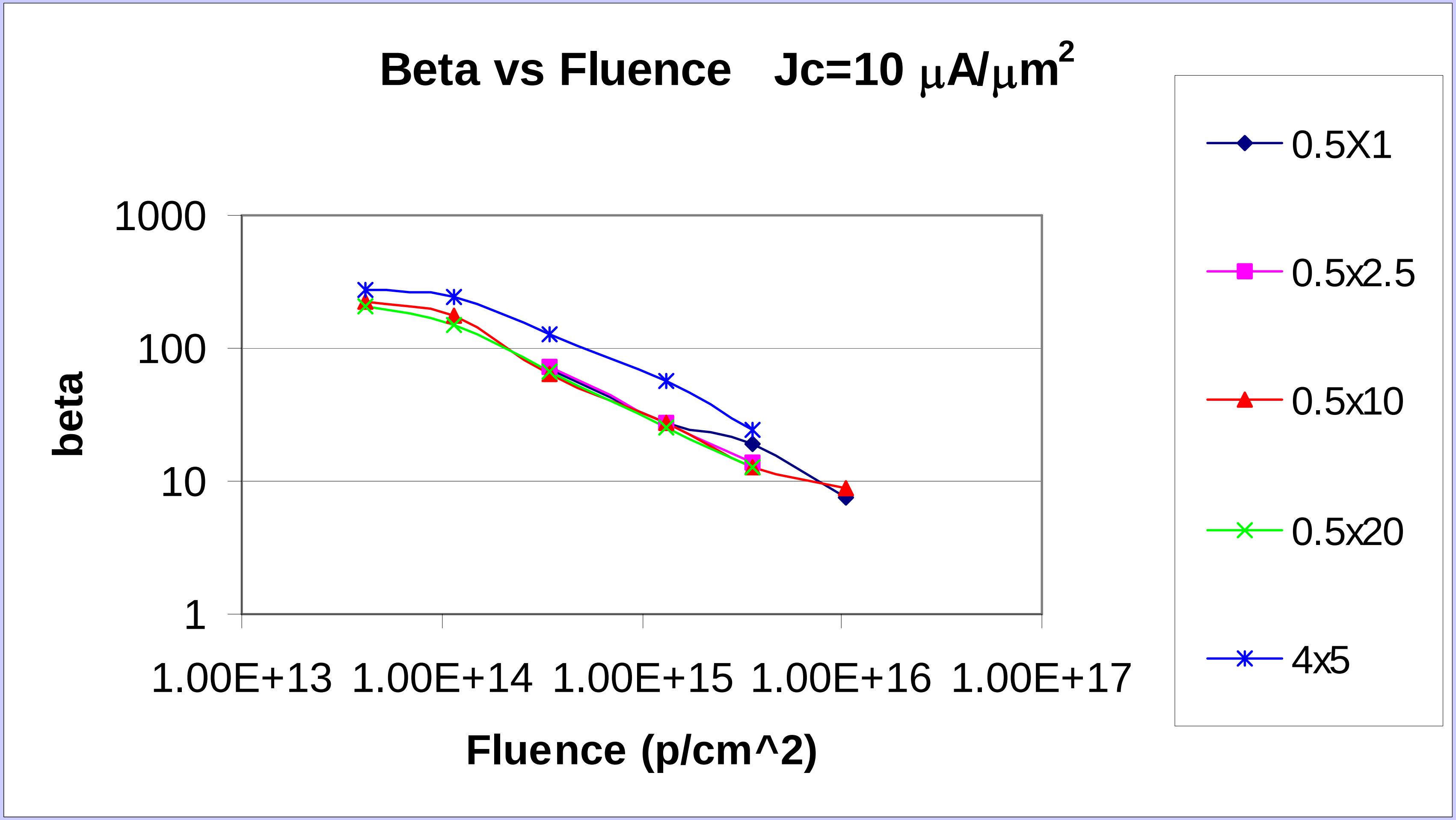


Radiation effects mainly the base leakage current



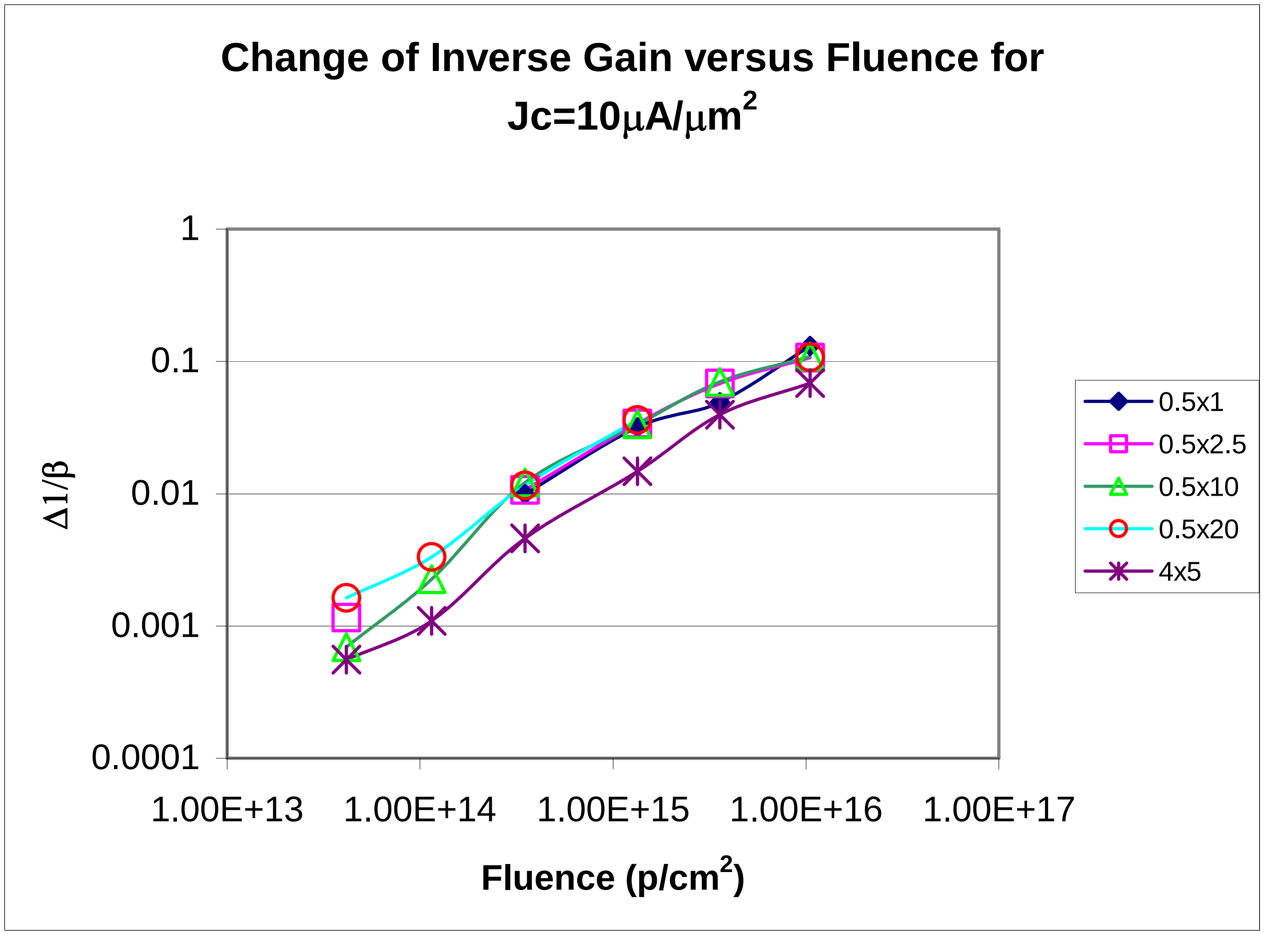
Radiation Damage
less at higher currents

Radiation Effects are geometry dependent at fixed I_c,
But are universal for fixed collector current density J_c,

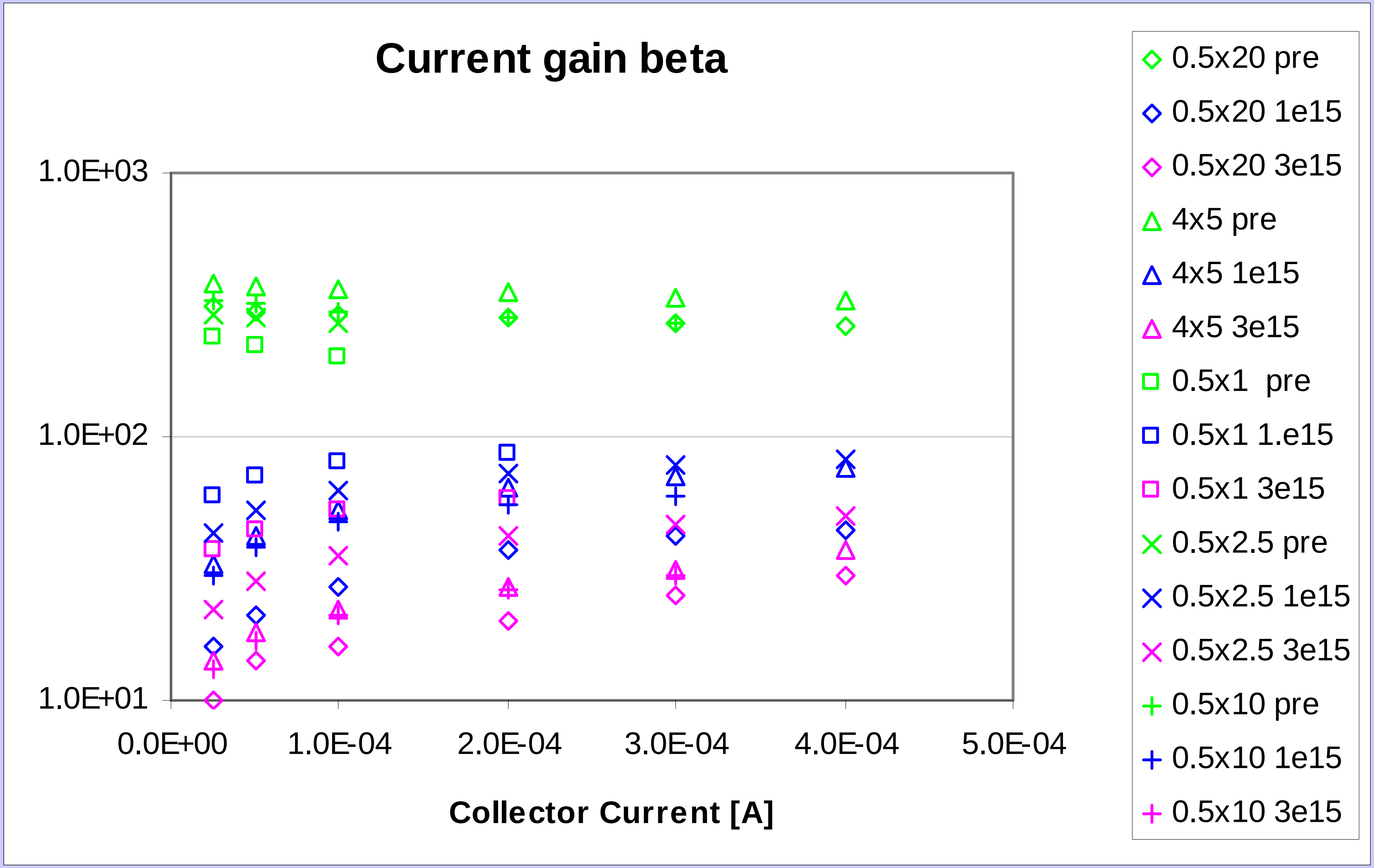


$\Delta(1/\beta)$ = Difference of $1/\beta$ post-rad and pre-rad vs. fluence at a fixed collector current density J_c, before annealing:

$$\Delta(1/\beta) \propto \text{Fluence}$$

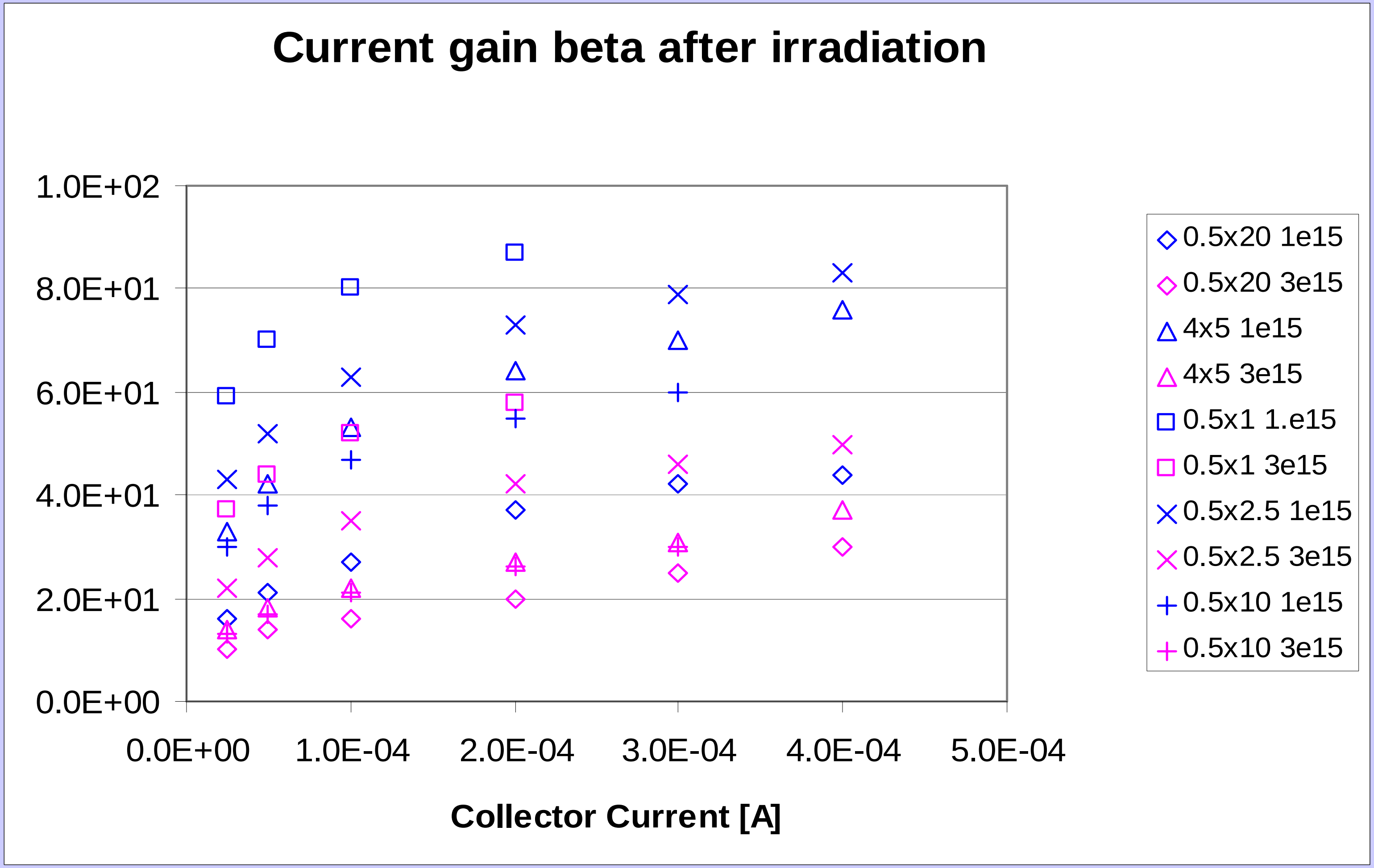


Current gain β post-rad and pre-rad vs. collector current, (before annealing)



Current gain β post-rad vs. collector current (before annealing)

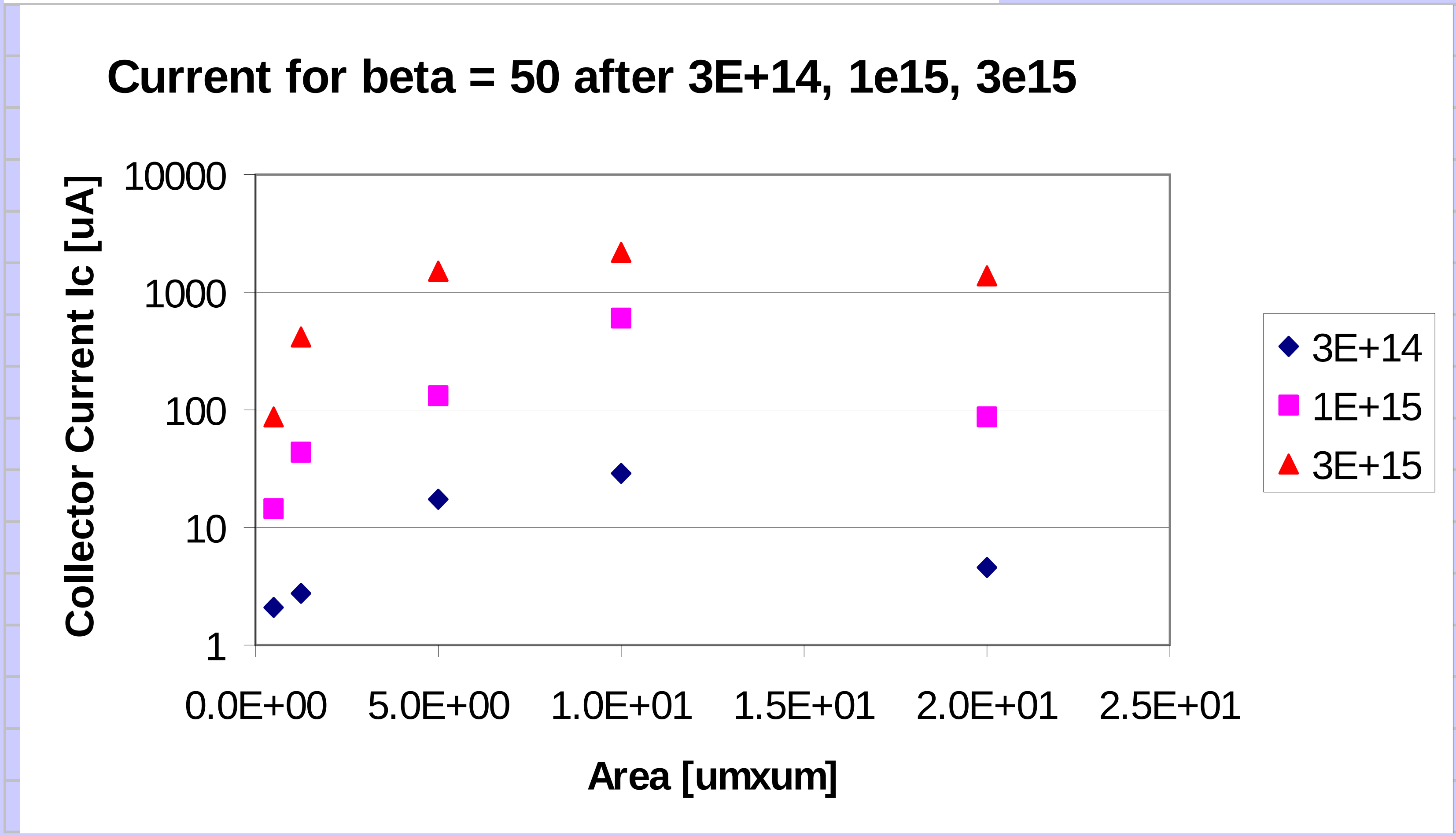
Large erosion of β observed, (annealing ≈ 50 – 100 % of post-rad value)

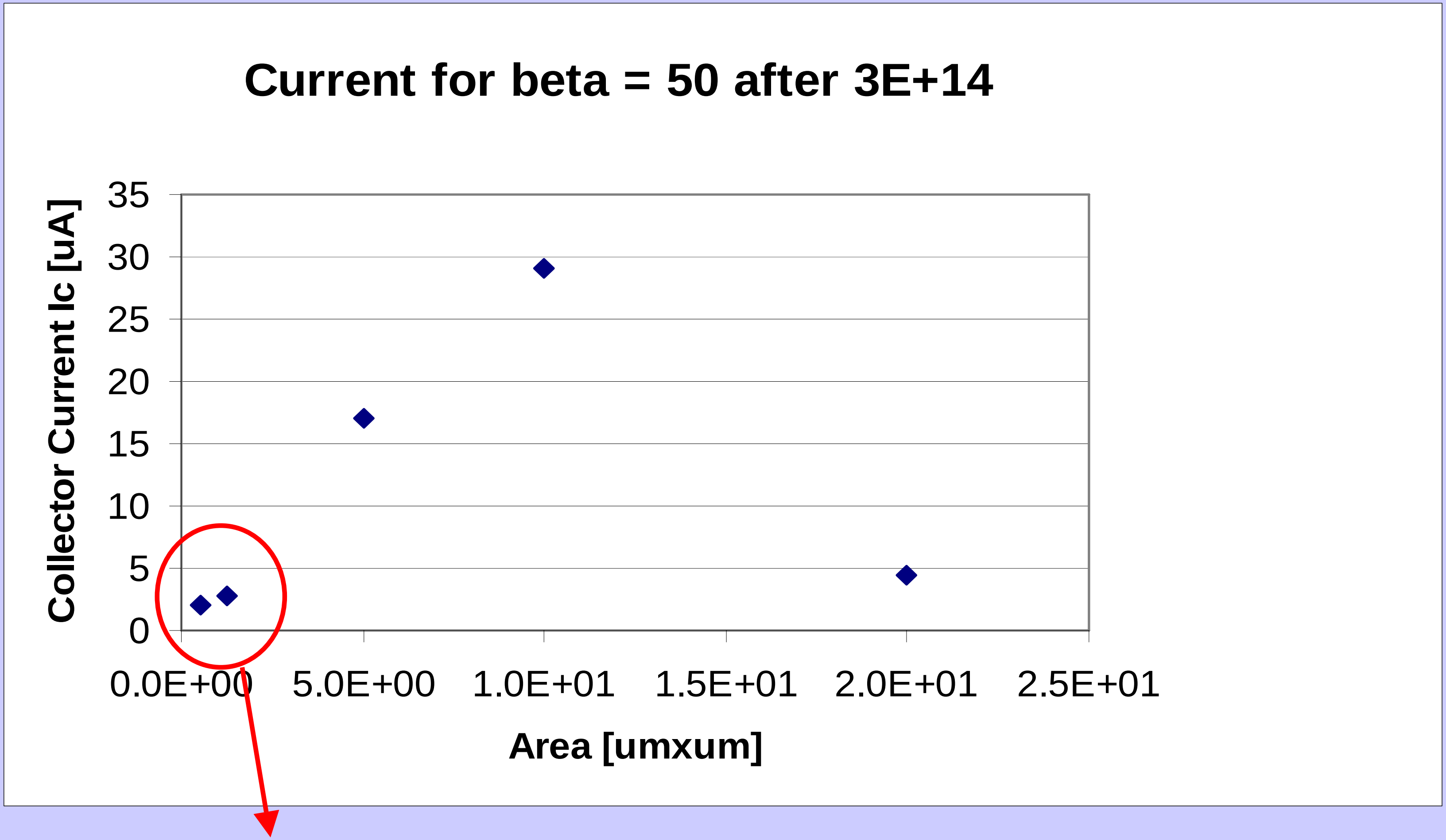


Power Consideration post-rad:

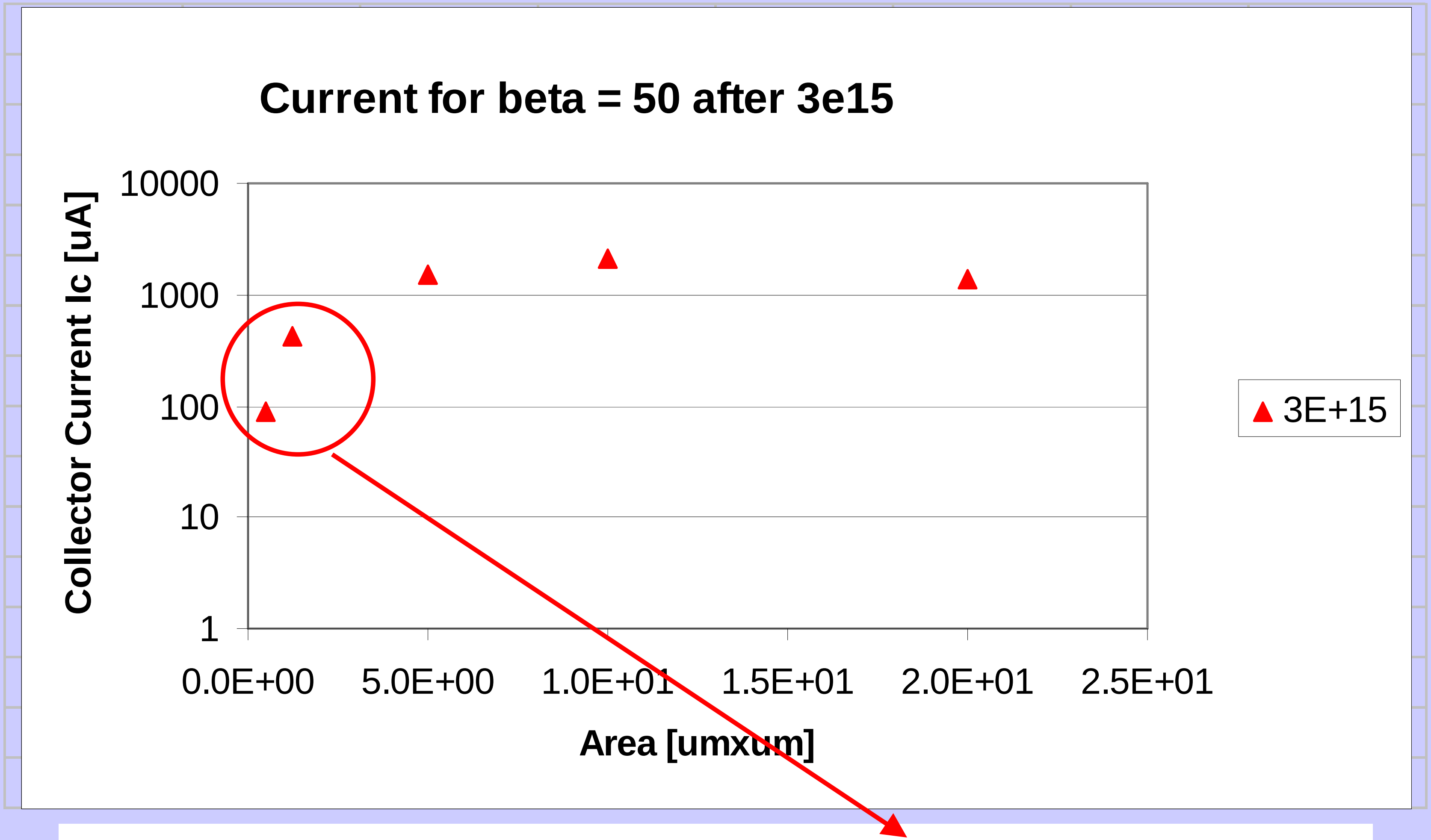
An acceptable current gain β is 50.

what is the current needed to achieve this post-rad?





In the outer tracker region, the entire front-end (amplifer-shaper-comparator) can be built with SiGe bipolar transistors resulting in huge power savings!



In the middle (short strip) region, only the front transistor can be built with SiGe bipolar transistors, others need to large a current!

First Look at Power Savings based on our Transistor Measurements (no anneal)

CHIP TECHNOLOGY FEATURE	0.25 μm CMOS ABCDS/FE		IBM 5HP SiGe	
Power: Bias for all but front transistor	330 μA	0.8 mW	20 μA	0.05 mW
Power: Front bias for 25 pF load	300 μA	0.75 mW	150 μA	0.375 mW
Power: Front bias for 7 pF load	120 μA	0.3 mW	50 μA	0.13 mW
Total Power (7 pF) 3×10^{14} 3×10^{15}	1.1 mW		0.18mW 0.9 mW	
Total Power (25 pF) 3×10^{14}	1.5 mW		0.43 mW	

Large Power Savings for large part of the tracking system with SiGe Frontend
Needs detailed simulation including matching

Noise in Bipolar Transistors (H. G. Spieler):

$$Q_n^2 = i_n^2 F_i T_s + e_n^2 C_{tot}^2 \frac{F_v}{T_s}$$

$$C_{tot} = C_{\det} + C_{in}$$

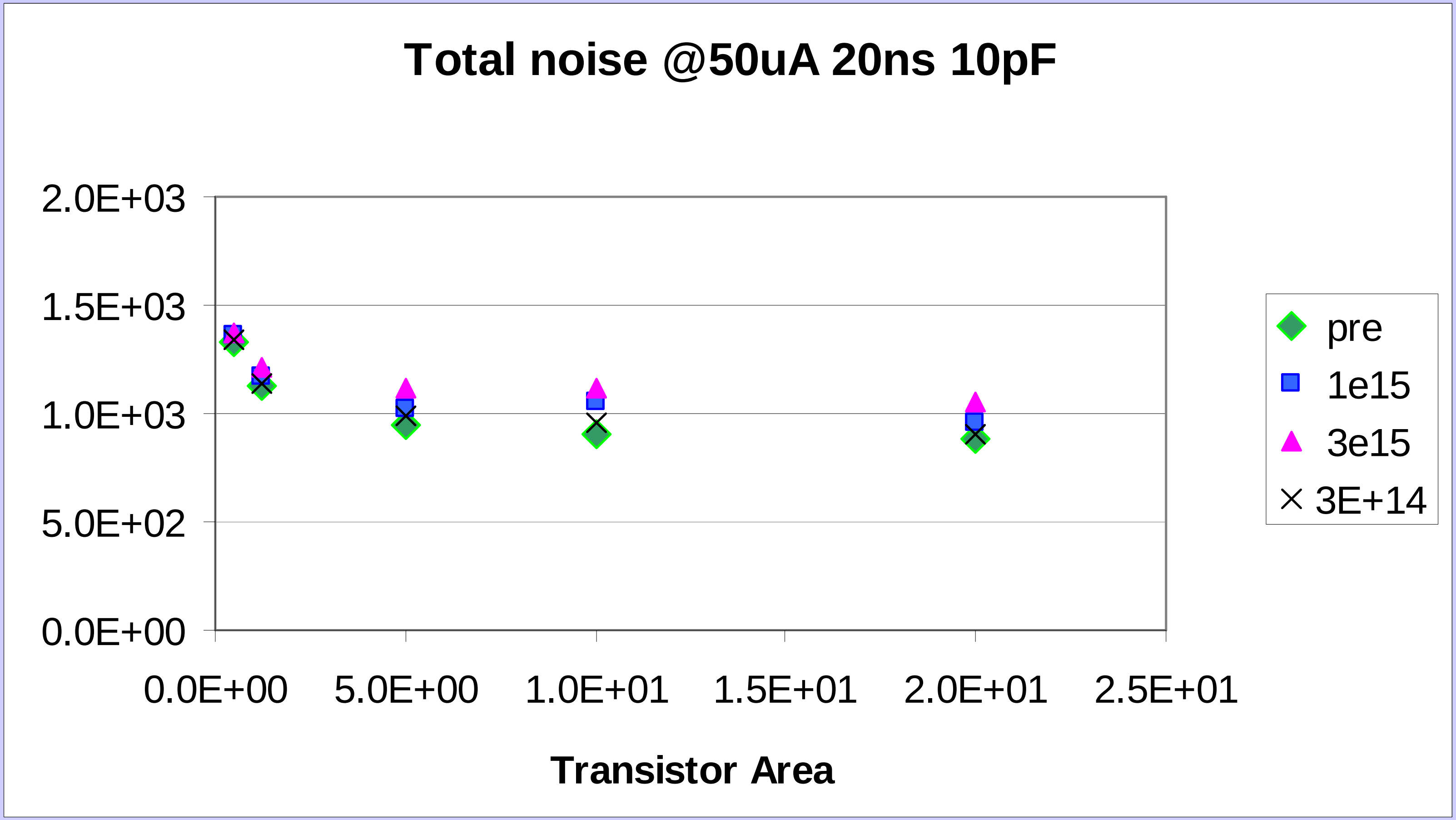
$$i_n^2 = 2q_e\left(\frac{I_c}{\beta} + I_{bias}\right) \qquad e_n^2 = \frac{2\,(k_B T)^2}{q_e\, I_e} + 4kTr_{bb}$$

Noise (scaled version)

$$Q_n^2 = (500e^-)^2 (I_c/100\mu A)(50/\beta)(T_s/20ns)$$

$$+ (600e^-)^2 (C_{tot}/10\,pF)^2 \left(\frac{20ns}{T_s}\right)(100\mu A/I_c + 0.87 r_{bb}/100\Omega)$$

$$C_{tot} = C_{\det} + C_{in}$$


Total noise @50uA 20ns 10pF
2.0E+03
1.5E+03
1.0E+03
5.0E+02
0.0E+00
0.0E+00
5.0E+00
1.0E+01
1.5E+01
2.0E+01
2.5E+01
Transistor Area
pre
1e15
3e15
3E+14

Conclusions:

- We extended the radiation testing of SiGe Bipolar transistors
  by a factor 100 in fluence thanks to the RD50 radiation program
- Modern high-speed technologies permit to extend
  the range of useful application of bipolar transistors (LHC ->sLHC)
- With the SiGe transistors (soon?) commercially available now, we can predict
  good noise behavior for short & long strips
  power savings in the entire analog front-end
  in the outer tracker ("long strips")
  power savings in the front-end transistor only
  in the mid-region tracker ("short strips")
- We started to investigate more advanced SiGe technologies (higher β),
  and are interested to irradiate the structures asap:
  - + CNM Barcelona (Miguel Ullan) started a collaboration with IHP
  - + We made contacts with STm through CERN (P.Jarron)
    and will receive test structures in the Fall
  - + Expect test structures from IBM in 8 HP with very large beta's (1000?)
    (Does post-rad current gain depend on pre-rad gain?)