P-spray implant optimization for p-type microstrip detectors

-Status of the RD50 calibration run-

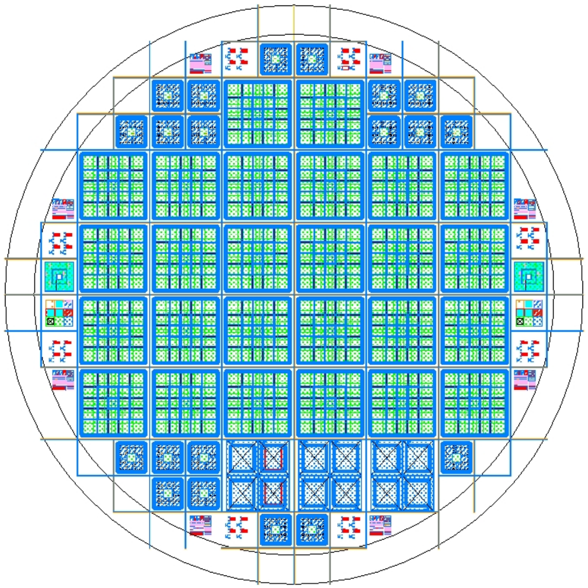
C. Fleta, M. Lozano, G. Pellegrini, K. Vatter, F. Campabadal, J. M. Rafí and M. Ullán

Instituto de Microelectrónica de Barcelona
IMB-CNM (CSIC)
Spain

3th June 2005

Background

- IMB-CNM to process wafers for the Collaboration
- P-in-N and N-in-P
- Mask set designed by RD50
- Insulation between strips provided only by p-spray (no p-stops)



- Optimize the p-spray parameters before processing the RD50 wafers
  - Complete simulation process (ISE-TCAD)
    - ➡ Test run to check simulation results

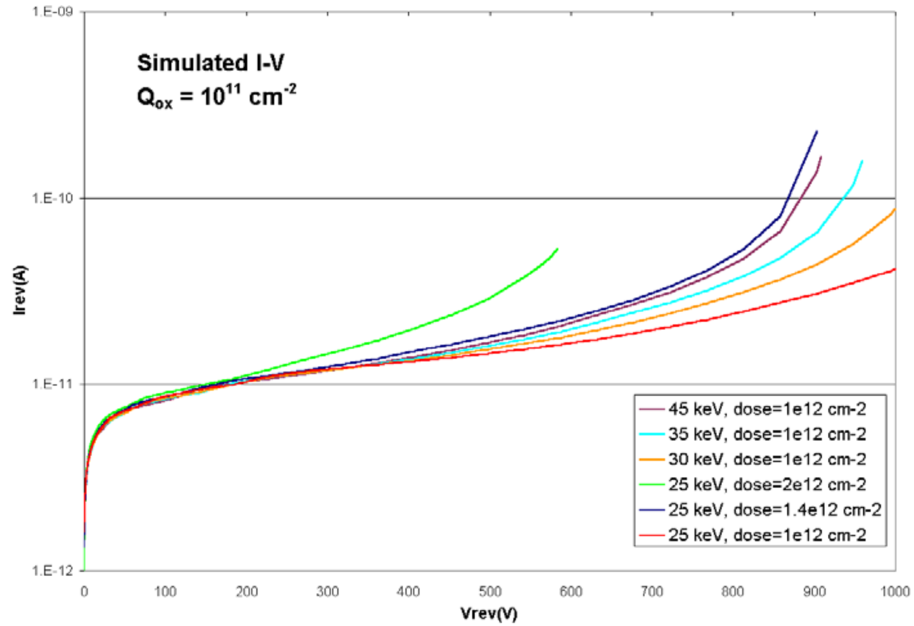
Wafer 1: 25 keV, 10^{12} cm^{-2}
Wafer 2: 25 keV, 1.4×10^{12} cm^{-2}
Wafer 3: 25 keV, 2×10^{12} cm^{-2}
Wafer 4: 30 keV, 10^{12} cm^{-2}
Wafer 5: 35 keV, 10^{12} cm^{-2}
Wafer 6: 45 keV, 10^{12} cm^{-2}

P-spray implant oxide thickness = 150 nm

Simulations: I-V

	P-spray	B peak (cm^{-3})	B total (cm^{-2})	V_{BD} (V)
Wafer 1	25 kev, 10^{12} cm^{-2}	3.80×10^{15}	3.01×10^{11}	> 1000
Wafer 2	25 kev, 1.4×10^{12} cm^{-2}	5.32×10^{15}	4.22×10^{11}	900
Wafer 3	25 kev, 2×10^{12} cm^{-2}	7.59×10^{15}	6.02×10^{11}	580
Wafer 4	30 kev, 10^{12} cm^{-2}	4.13×10^{15}	3.56×10^{11}	> 1000
Wafer 5	35 kev, 10^{12} cm^{-2}	4.30×10^{15}	3.85×10^{11}	960
Wafer 6	45 kev, 10^{12} cm^{-2}	4.44×10^{15}	4.09×10^{11}	910

- V_{BD} decreases as implanted dose increases



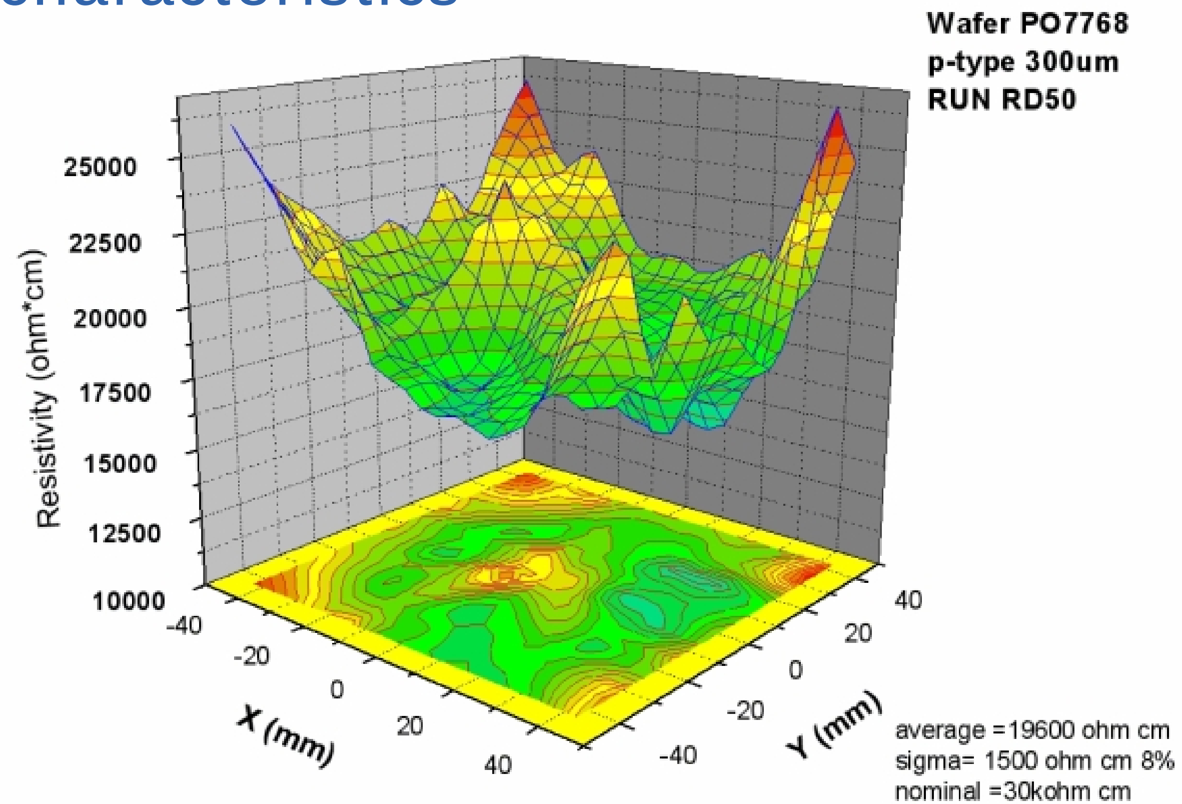
Simulations: strip insulation

- Inversion layer at full depletion?

		Q_{ox} (cm^{-2})	
		10^{11}	10^{12}
wafer	1	NO	YES
	2	NO	YES
	3	NO	YES
	4	NO	YES
	5	NO	YES
	6	NO	YES

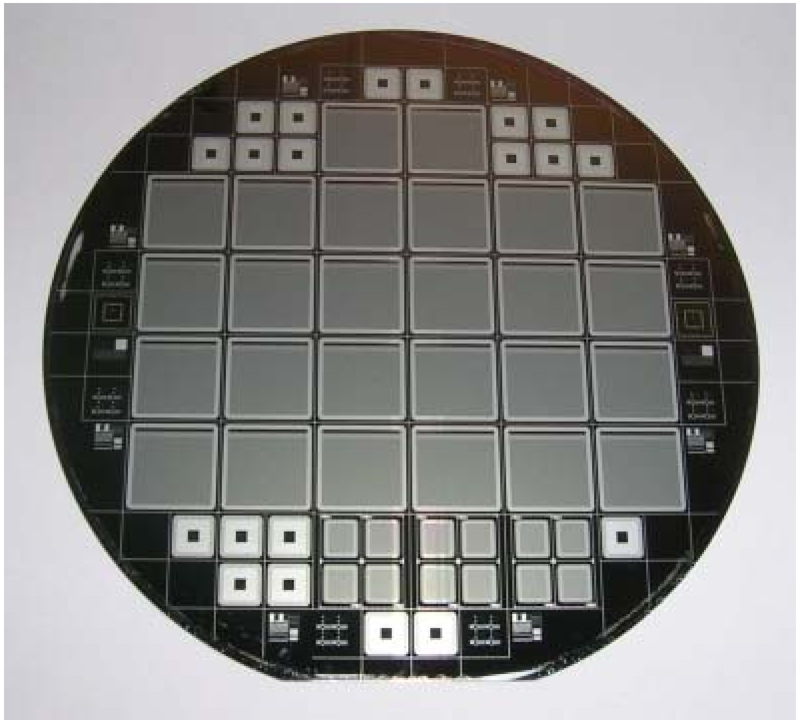
- Higher p-spray doses to avoid surface inversion on heavily irradiated devices, but V_{BD} decreases
  - Compromise solution
  - Strip insulation is not the major concern in irradiated detectors
    - More complete simulations needed

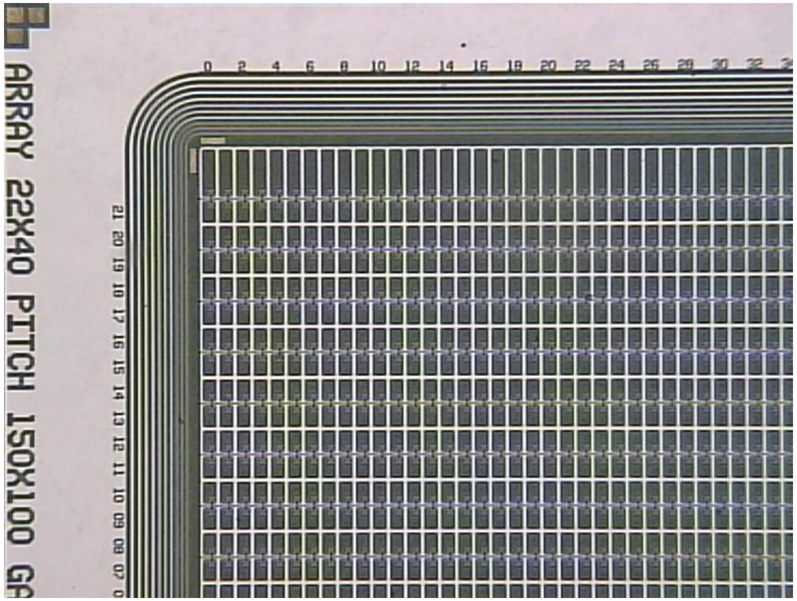
Wafer characteristics

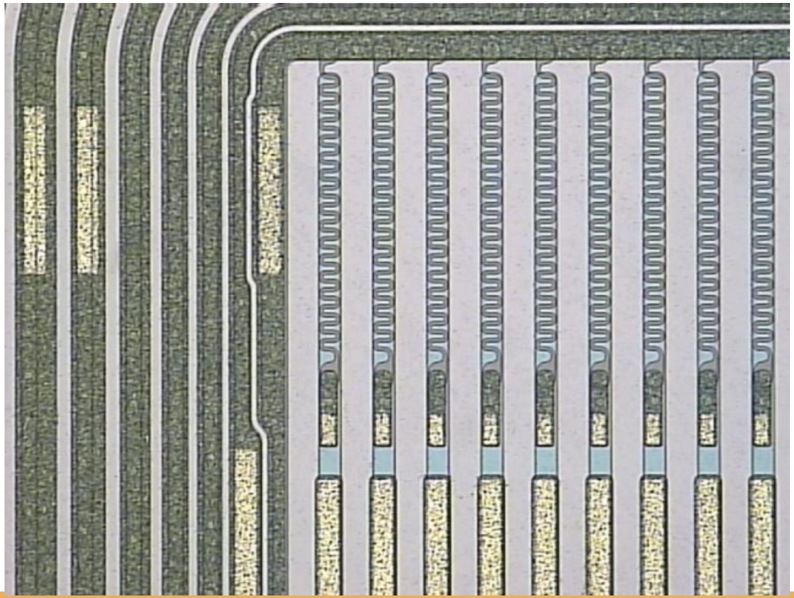


- New wafers from Siltronic
- <100>, p-type, 300 ± 15 μm
- ρ (nominal)= 30 kΩ.cm, ρ (measured)= 20 kΩ.cm

Fabricated devices

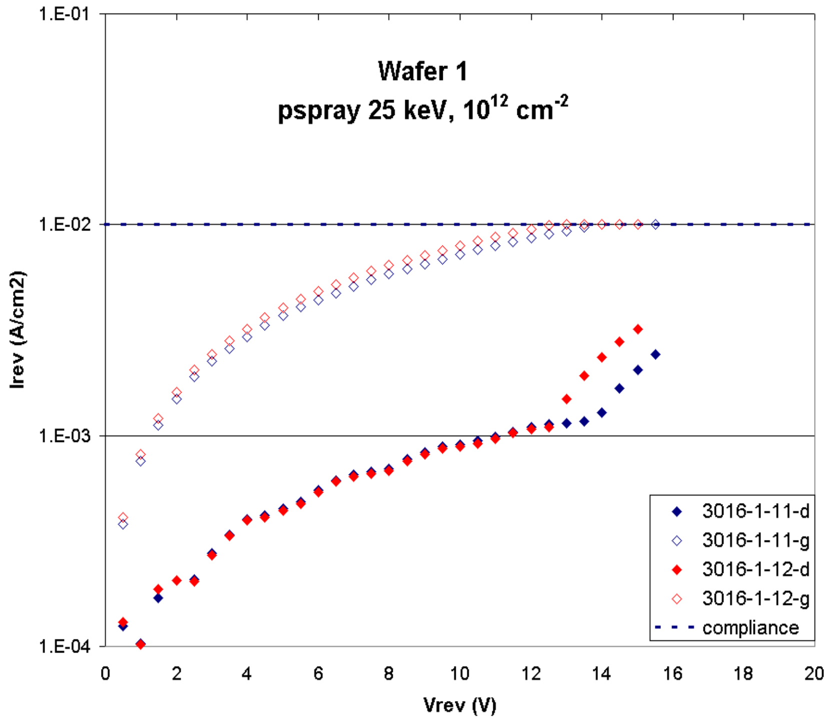


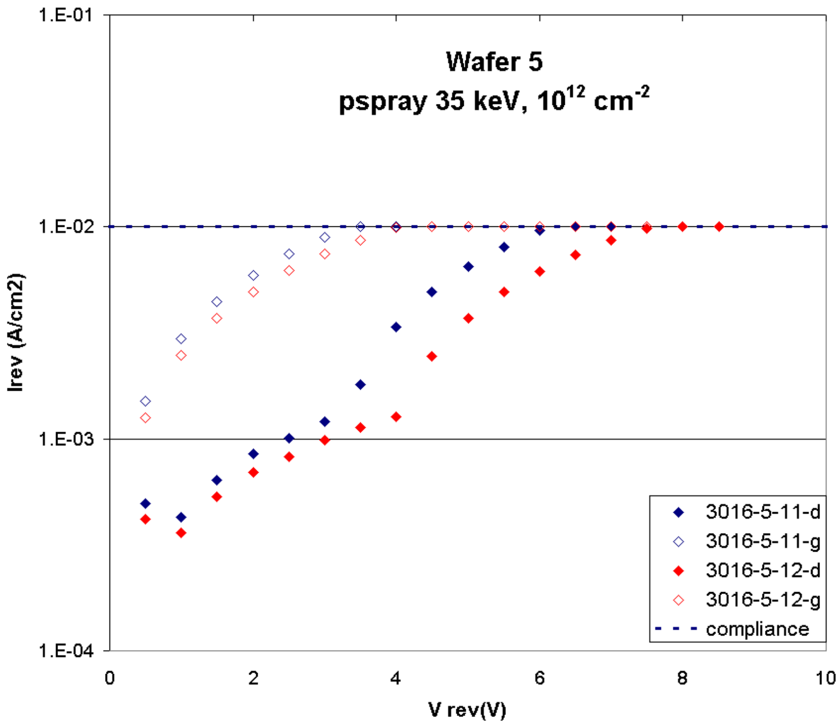




Electrical characterization

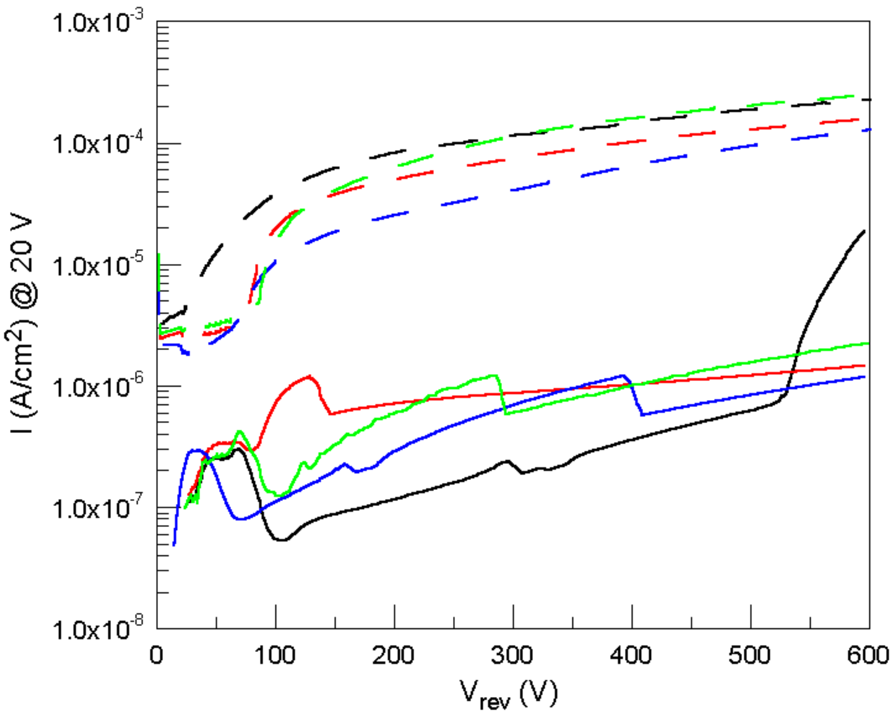
- Microstrips of wafers 1 to 5:
  - Very high leakage currents (mA/cm^2 @ 10 V)
  - Do not fulfill the requirements for radiation detectors

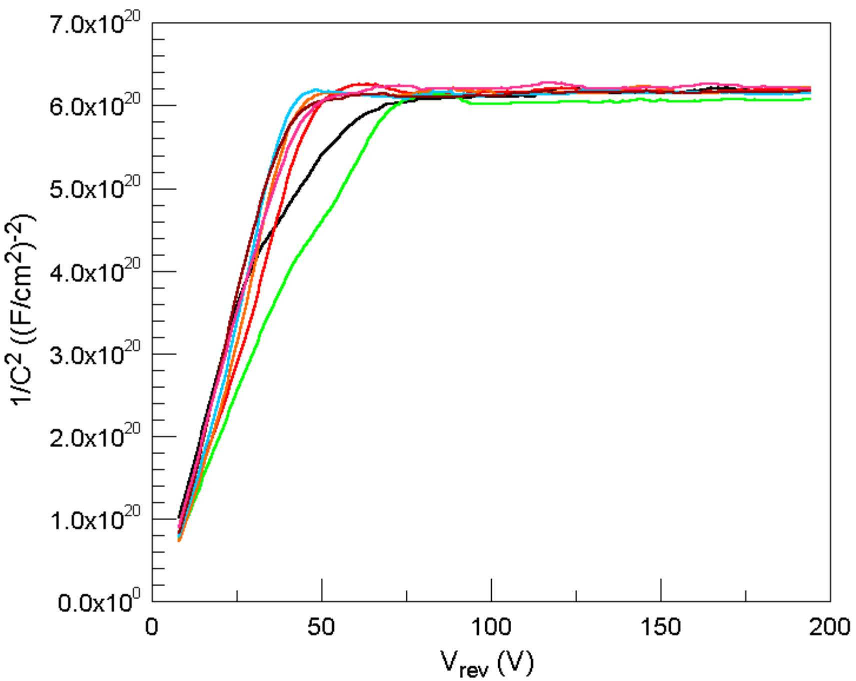




Electrical characterization

- Wafer 6
  - Leakage current ~ $\mu A/cm^2$
  - V_{BD} > 600 V
  - V_{FD} = 46 ± 5 V --> ρ = 17 ± 2 kΩ.cm

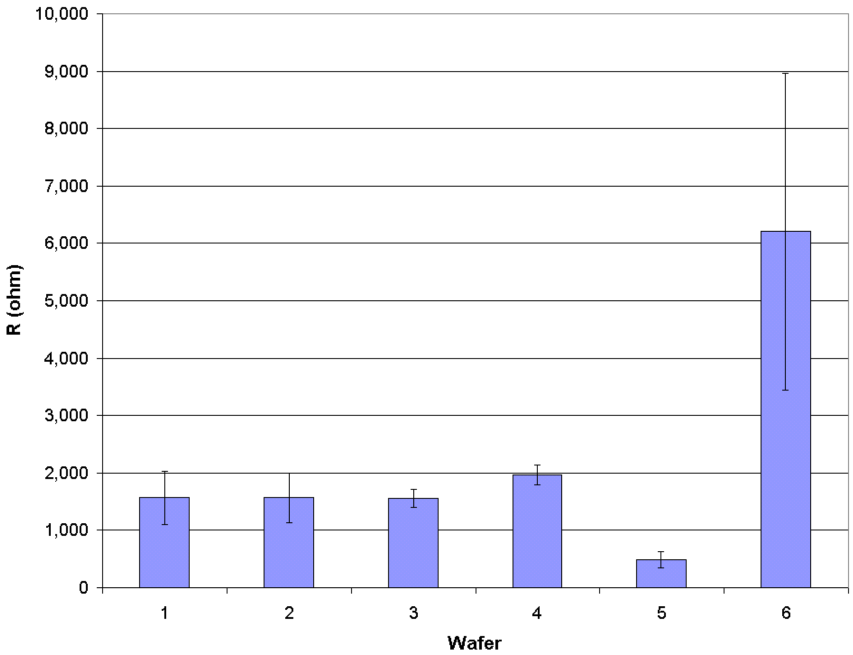




Electrical characterization

- Verify strip insulation
  - Measurement of the resistance between two consecutive microstrips

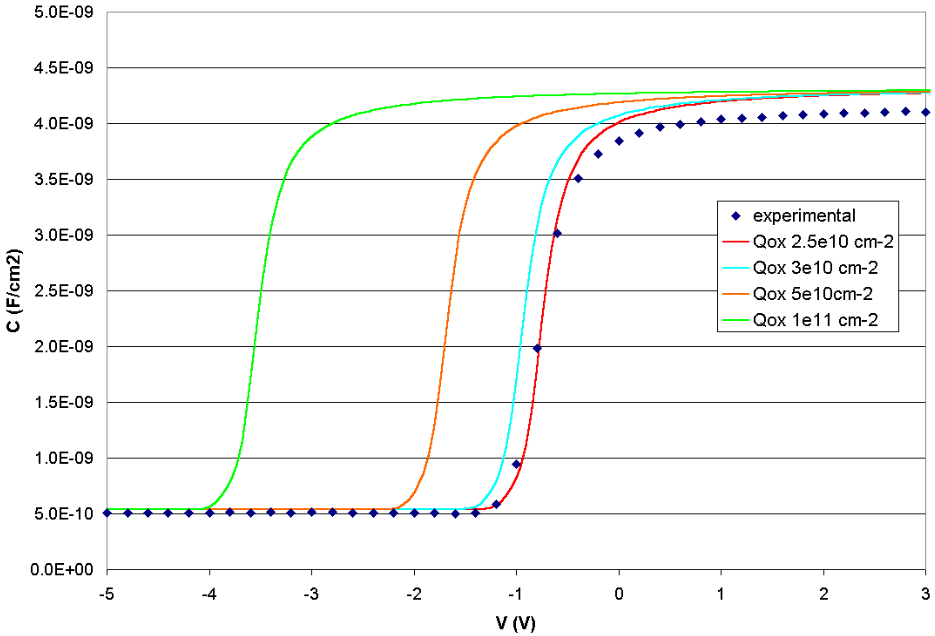
Surface is clearly inverted



~250 MΩ for a N-in-P with P-stops

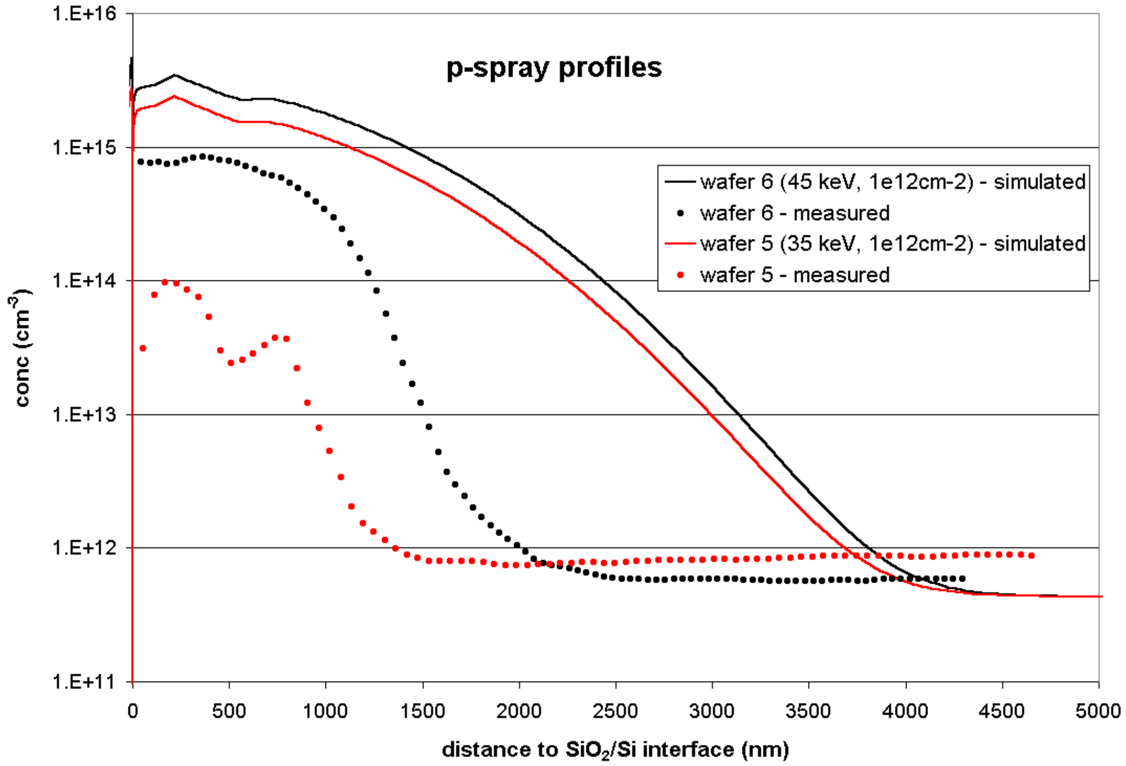
Oxide charge measurement

- Simulated devices: $Q_{ox} = 10^{11}$ cm^{-2}. Overestimated oxide quality?



- C-V measured in test structure (MOS capacitor)
  - Agreement with the simulated curve for $Q_{ox} = 2.5 \times 10^{10}$ cm^{-2}
  - Another reason for the bad electrical performance

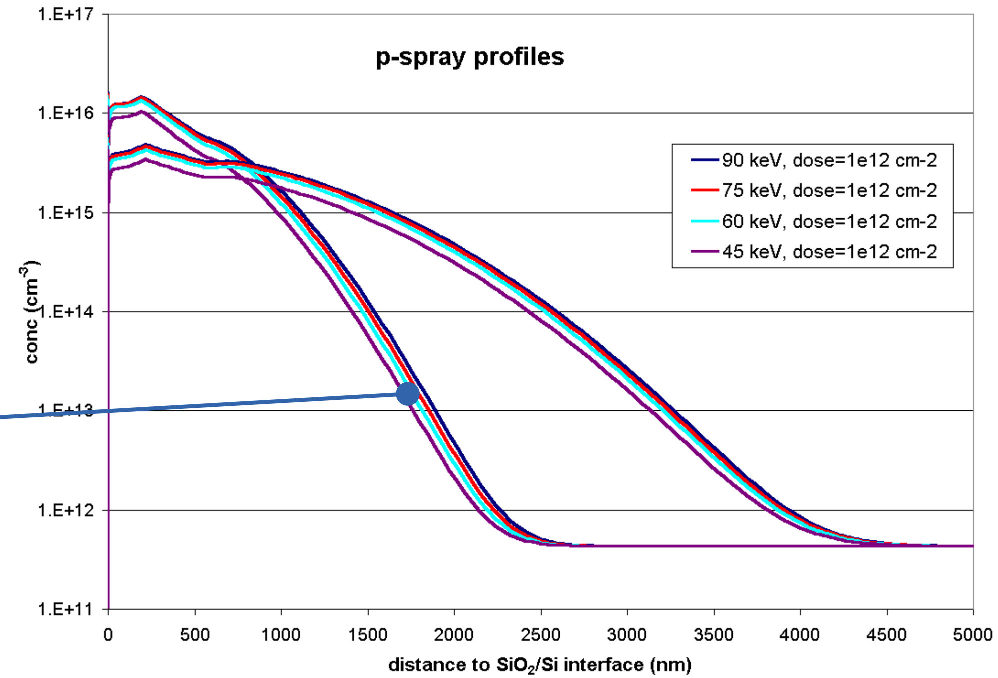
Spreading resistance measurements



- Total implanted dose lower than the predicted by simulations
  - Wafer 6: 70% of the expected dose
  - Wafer 5: 9%

Second calibration run

- Higher implant energies with the lowest dose (10^{12} cm^{-2})
  - 45 keV (= wafer 6)
  - 60 keV
  - 75 keV
  - 90 keV
- 4 more wafers: same p-spray parameters, less thermal stress
  - Field oxide low-T deposited



Second calibration run

- Defective wafers from Siltronic
  - P-spray implant oxide thicker in some areas (irregular wafer surface)
  - Will affect the implant profile

- Could this be the reason for the bad results of the previous run?
  - Wafers from the same provider but a different batch
  - Did not detect anything unusual during the first process

Conclusions

- Calibration runs to optimize the p-spray implant parameters in N-in-P detectors
  - First run: p-spray profiles lower than expected
    - Implantation doses near the technical limit of the ion implanter. Calibration error?
    - Wrong predictions by process simulator?
    - Defective wafers?
    - ...?
  - Second run:
    - Oxide thickness not uniform due to irregular wafer surface
    - Still not finished
- What we have learnt so far...
  - Not sure of the suitability of the p-spray for heavily irradiated devices
    - Compromise between reasonable V_{BD} and good strip insulation
    - More complete studies needed
  - P-spray seems to be very sensitive to fabrication details
    - Alternative technologies?