Powering Interlocks

A common task shared between AB-CO, AB-PO and AT-MEL

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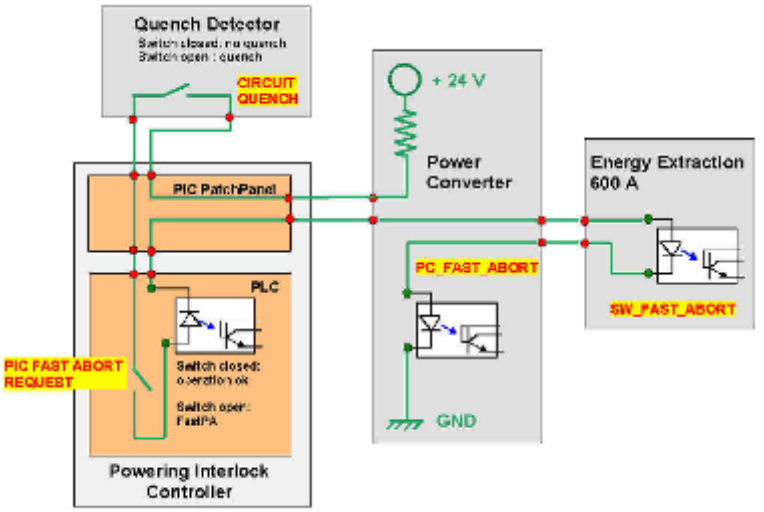
Powering interlocks - outline

- Hardwired interlocks
- Software links & interlocks



Example from LHC-D-ES-0003 rev 1.1: Hardware interface for 600 A corrector circuits.

RCD.A56B1:ST_PWR_PERM **=**
DQQDC.UA63.RCD.A56B1.LD1:ST_PWR_PERM **&&**
DQQDC.UA63.RCD.A56B1.LD2:ST_PWR_PERM **&&**
DFLBS.5L6.RCD.A56B1.LD1:ST_PWR_PERM **&&**
DFLBS.5L6.RCD.A56B1.LD2:ST_PWR_PERM **&&**
DQQDG.UA63.RCD.A56B1:ST_PWR_PERM **&&**
DQAMG.UA63.RCD.A56B1:ST_PWR_PERM

Example: QPS POWER PERMIT condition for a 600 A corrector circuit.

Hardwired interlocks I

- Current loops linking the power converter, the powering interlock controller and the quench protection system
  - Powering Permit Loop, Powering Failure Loop, Circuit Quench Loop, Discharge Loop
- Long current loops internal to the quench protection system for the main circuits (linking the odd and even points)
- Hardware design based on experience gained during the exploitation of the STRING II experiment
- Development finished and most devices in production
- First tests successfully performed on power converter test benches
  - Equipment designed & produced by different groups conform to the common specification (LHC-D-ES-0003 rev. 1.1)
  - First type tests on EMC performed
- **Powering interlocks are critical for safety and absolutely vital for LHC operation**

Hardwired interlocks II

- Testing of the hardwired interlocks (see LHC-D-HCP-0002 rev 1.0) requires:
  - Availability of concerned hardware: power converter, PIC, quench detection system, energy extraction system (if applicable)
  - Supervision applications for PC, PIC and QPS
  - Post mortem database and data retrieval tools & LHC timing
  - Logging & alarms
- Interlock hardware required for the short circuit tests of the power converters
- Test and commissioning of the powering interlocks will start with LSSL8 beginning of January 2006
- During commissioning of LSSL8 and sector 8/1 a few additional type tests have to be performed
  - EMC, timing of abort sequences …
- It is foreseen to test the powering interlocks to a very wide extent with the help of automatic procedures (see LHC-D-HCP-0005 rev.1.0)

Software links & interlocks I

- Despite hardwired links a few software protection signals are exchanged between the PIC supervision and the supervision of the corresponding systems
  - “Cryo OK”
  - QPS power permit signal: <Circuit_name:ST_PWR_PERMIT>
- Purpose of the ST_PWR_PERMIT signal is to ensure the 100% functionality of the QPS prior to the powering up a superconducting circuit
  - Signal to be calculated per circuit by the QPS supervision application based on the information delivered by the QPS controllers
  - The power permit condition is verified by each controller permanently with respect to its associated equipment
  - Each controller transfers this information to the corresponding gateway, from where it is accessible for the QPS supervision application

Software links & interlocks II

- QPS supervision sends the result on request to the PIC supervision application
  - ST_PWR_PERMIT signal required for starting a powering run but not interlocking
  - Alarms are generated in case the signal changes its state
  - ST_PWR_PERMIT signal to be refreshed in case of consecutive powering cycles
    - Procedure to be defined
- Engineering specification for the transmission protocol and its implementation into the supervision applications currently in preparation
  - 1st proposal to be discussed in MPWG
- Test of all software links already defined in LHC-D-HCP-0002 rev 1.0

Conclusions

- Development of hardwired interlocks finished and a significant part of the equipment already available at CERN
- Definition of the generation and transmission of software protection signals to be completed and approved in the near future
- Interlock testing and commissioning to be started with LSSL8 beginning of January 2006
  - Sufficient resources (time and manpower) have to be provided
  - Shortcuts during commissioning of these systems are not an option
- Tests have to be repeated on a regular basis during LHC exploitation