# N-in-n and n-in-p Pixel Sensor Production at CiS

Anna Macchiolo - MPP Munich

- Investigation of the fluence range at which the planar pixel sensors can be used to instruments the trackers at SLHC
- Application of the results of many studies on n-side readout (mainly performed with micro-strip sensors within RD50) to pixel geometries and read-out
- Optmization of the planar pixel structures to obtain slimmer edges

- **Proposal to transform this submission into a common RD50 project**

# R&D for a novel pixel detector for SLHC

➢ Production started as a joint effort of ATLAS groups participating in the Planar Pixel Sensor Project (coordinator C. Goessling, TU Dortmund) in view of the Insertable B-Layer upgrade and SLHC

| Country | Institution | |
|---|---|---|
| Czech Rep. | AS CR Prague | RD50 member |
| CERN | ATLAS Pixel group | RD50 member |
| France | Lal Orsay | |
| | LPHNE / Paris VI | |
| Germany | MPP | RD50 member |
| | TU Dortmund | RD50 member |
| Spain | IFAE-CNM | RD50 member |
| USA | UCSC | RD50 member |

➢ Parallel productions of n-on-p pixel sensors on 6” wafers within the ATLAS Planar Pixel Sensor Project :

- *HPK, organized by the KEK group*
- *MICRON, organized by the Liverpool group*

# Foreseen production parameters

- Production with CiS (Erfurt, Germany) on 4” wafers

- It combines the “known” → production of pixel sensors with a proven technology (n-in-n) with one of the two pixel sensor suppliers of the present system

  with the “unknown” → new bulk material for pixels (MCz and p-type) , new geometries to investigate active/slimmed edges

| | | | |
|---|---|---|---|
| n-in-n batch | ~ 10-15 Fz wafers | ~ 5-10 MCz wafers | Double sided process |
| n-in-p batch | ~ 15 Fz wafers | ~ 5 MCz wafers | Single sided process |

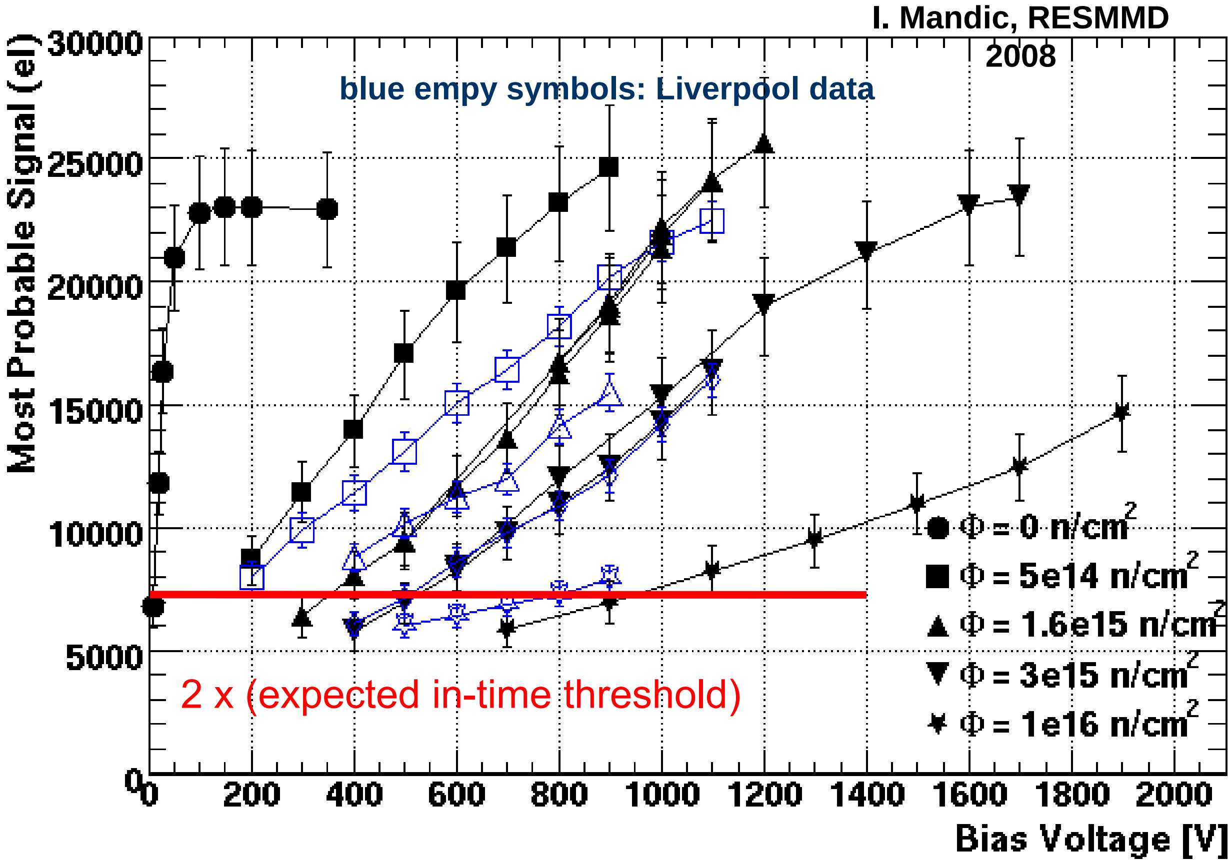
- Foreseen production times: - 4 weeks for the mask production
  - 4 months for n-in-p
  - 5 months for n-in-n

- Inter-pixel isolation methods: homogenous p-spray and moderated p-spray for both batches

# Why planar pixel sensors?

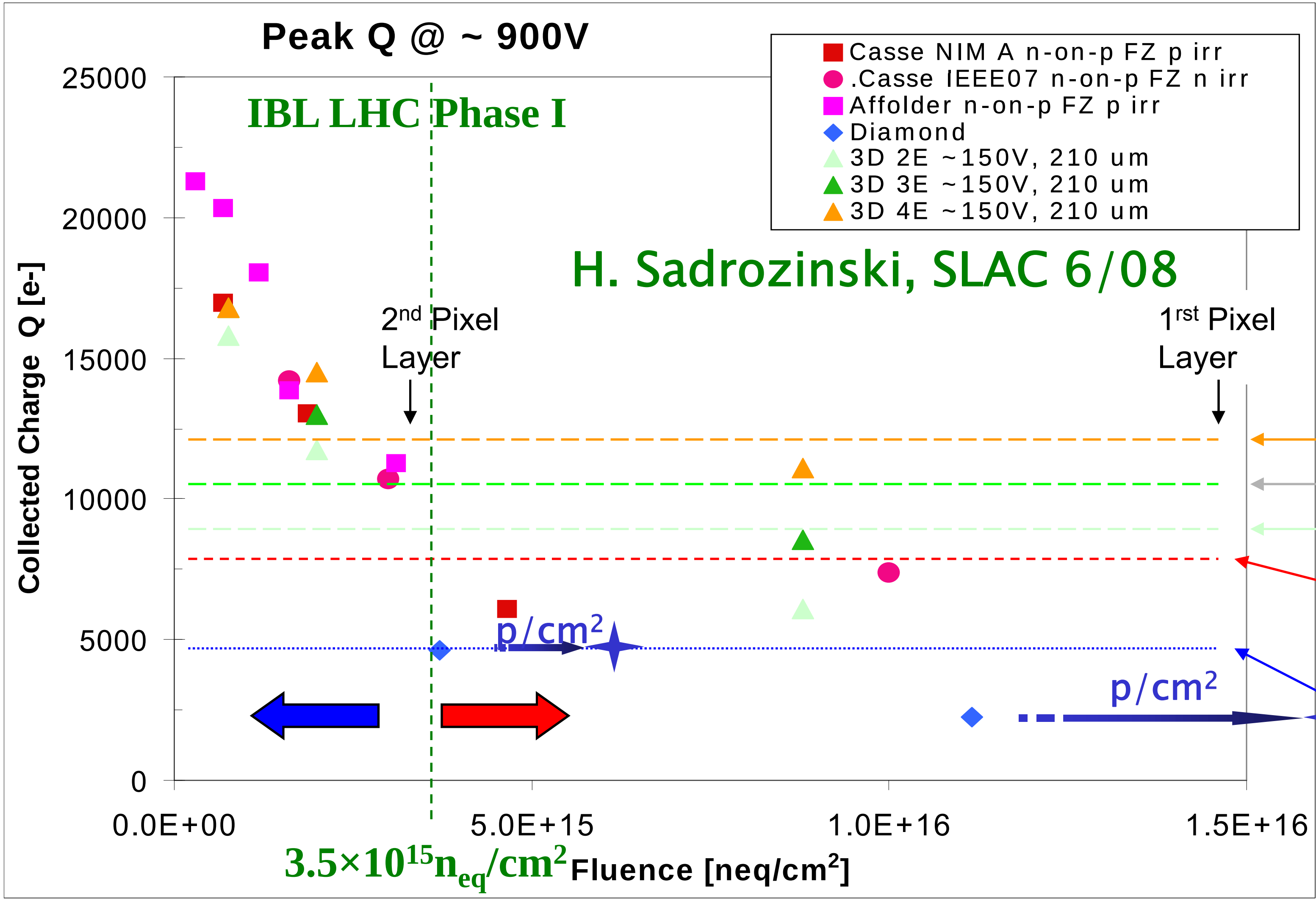
- We aim to investigate the maximum fluence at which planar pixel sensors can be operated, as a function of the bulk material, the production parameters, geometry, annealing scenarios, read-out electronics (threshold dependence)

## Signal (V) with 25ns microstrip R/O




- latest results from Liverpool and Ljubljana: CCE in strip devices after large fluences much higher than anticipated
- reasons not yet clear
- measurements to confirm this behaviour in n-in-n pixel sensors are underway

# Why planar pixel sensors?



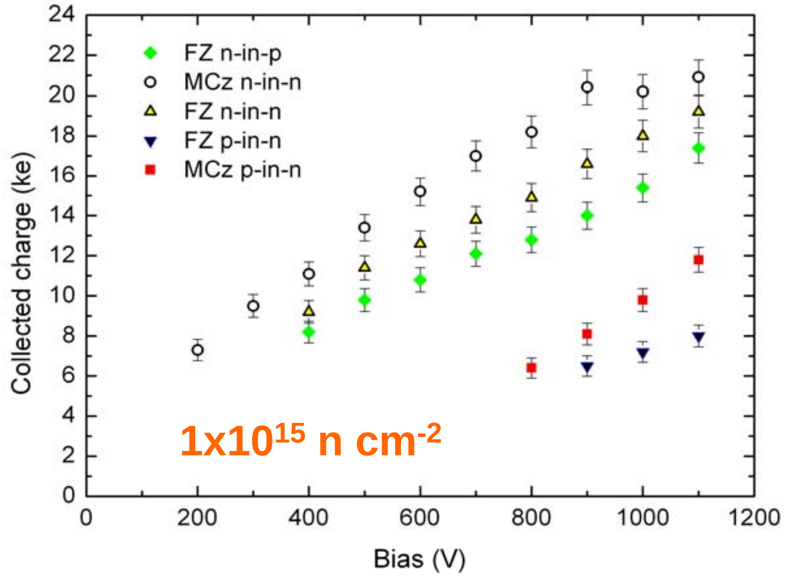

Signal required with present Pixel ASIC (= 2 x In-time threshold):

A. Macchiolo, 13th RD50 Workshop, CERN 11th November 2008

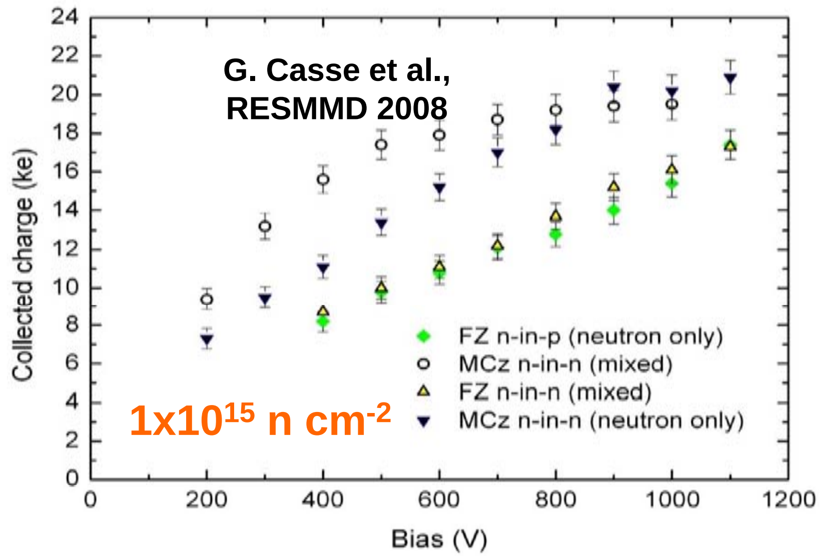
# Choice of bulk material

- Planar n-in-n sensors:
  - Proven technology – ATLAS / CMS present pixel sensor
- Planar n-in-p sensors:
  - Intensive studies within RD50 - designated material for the upgrade of the ATLAS SCT
  - Much less experience at the pixel level
  - Only one-sided processing required → less costly
  - HV present on pixel / FE-side – choice of insulation ?
- The goal of this production is to achieve best possible comparability between n-bulk and p-bulk sensors of different materials

# Choice of bulk material: Fz and MCZ




- Explore MCZ silicon as possible alternative to Fz for n-in-n pixels.
- MCz shows better performances than Fz after neutron ….




- … and mixed irradiations. n-type MCz looks like a good candidate to be used in the outer pixel layers where there are comparable levels of charged and neutral radiation → $N_{eff}$ compensation.

- Comparable behaviour of p-type Fz and MCz after neutron irradiation

# Areas of R&D: Active/Slim Edges

- coverage lost due to inactive gaps/edges must not exceed 1-3%
- need to increase the active area coverage especially in the inner layers where it's not possible (in ATLAS at least) to have double side structures to recover dead module regions
- therefore, inactive edges have to shrink from ~1100 μm to O(100 μm) on at least 2 sides of the sensor
- Ideas to reach this:

  - fewer and narrower guard rings?
  - pixels right up to the edge?
  - avoidance of crystal-damaging cutting methods (sawing)?
  - Interested groups: Dortmund<br>IFAE-CNM<br>Orsay- LPHNE<br>UCSC

# Active/Slim Edges: Current Activities (I)

- First designs with reduced guard-ring structures with respect to the present one – to be included in the n-in-n and n-in-p batches
- TCAD simulations ongoing to optmize a narrower version of the guard-ring structure and the dimensions of the cutting region
- Laser cutting tests using current sensors and test structures under preparation
- Insert structures to be cut by dry etching at CNM (low damage surface in comparison with laser drilling or diamond saw cut)

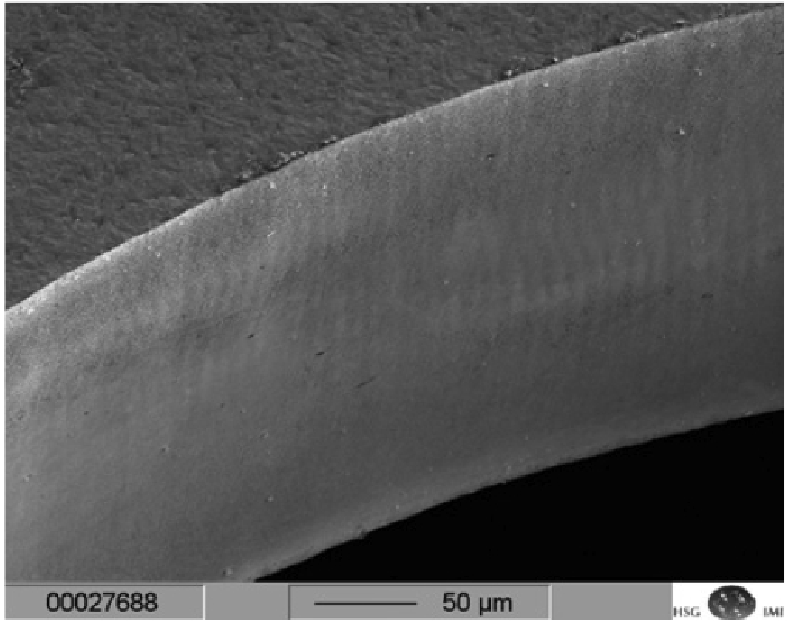
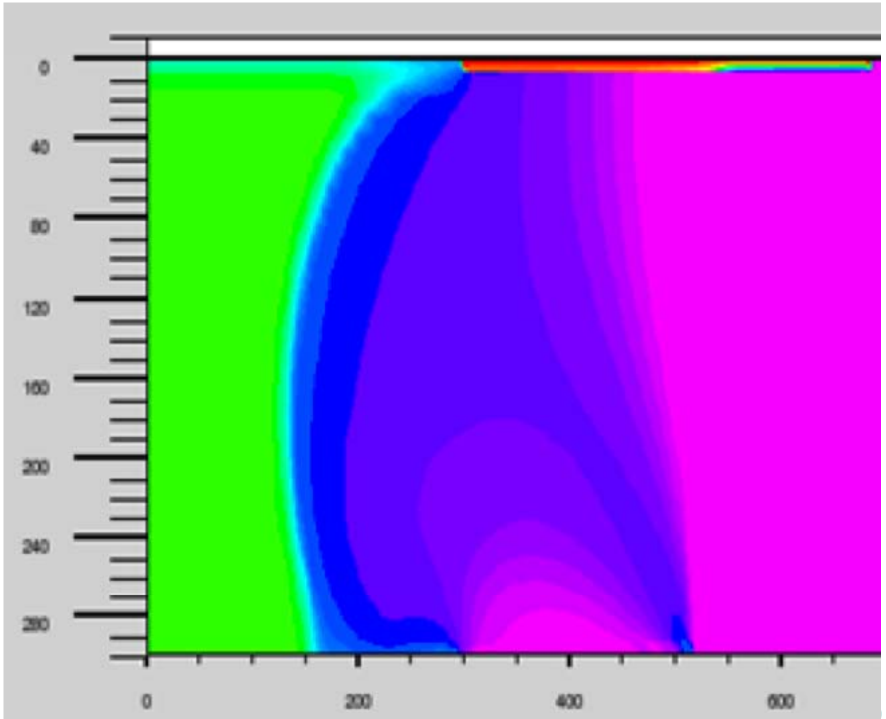


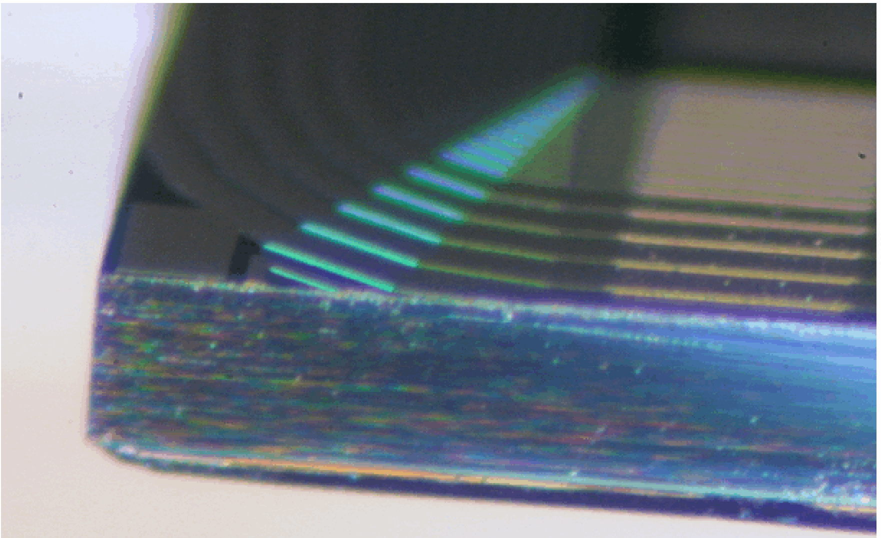

FIGURE 2: **Edge of a silicon wafer with a thickness of 300 µm cut with a high average power picosecond laser of the TruMicro Series 5000. No chipping and heat affected zone can be detected.**

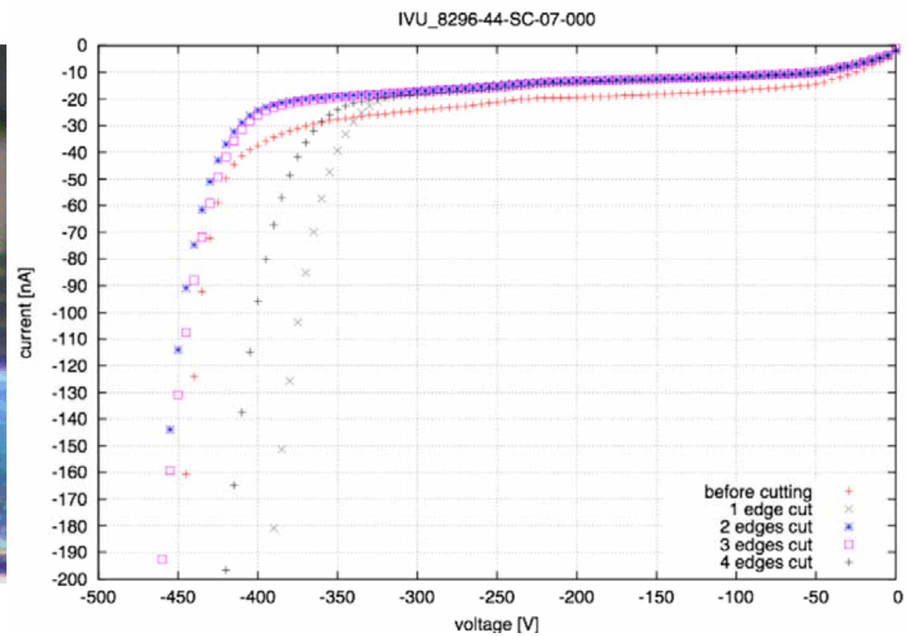



Depletion in n-in-n device

# Active/Slim Edges: Current Activities (II)

- first results from saw dicing trials amidst the guard rings encouraging
- investigation of breakdown behaviour of unirradiated SingleChips ongoing
- cutting of irradiated samples under preparation






Example of IV curves obtained on a unirradiated FE-I3 Single Chip Sensors cutting between the 15th and the 16th guard-ring

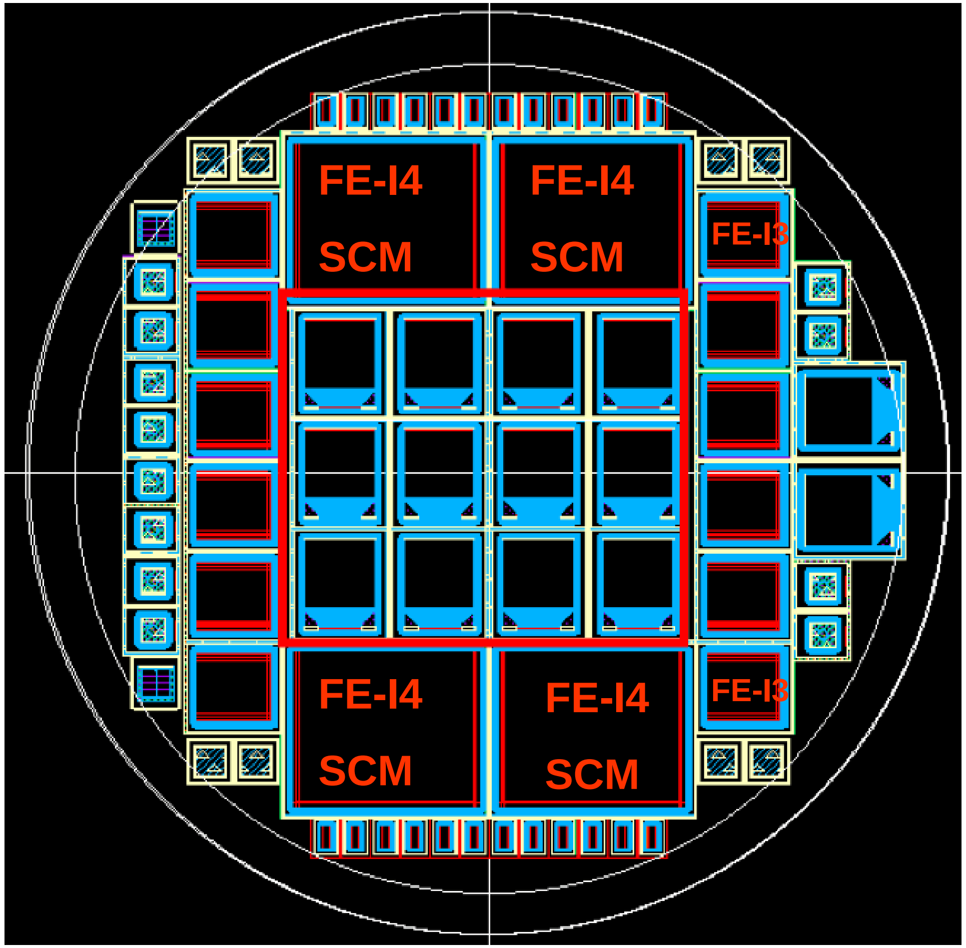
# Overview of sensor structures (I)

- Need two different masks for n-in-n (guard rings on the back side) and n-in-p (guard rings on the top side)

- n-in-p batch

- **FE-I4** (new ATLAS ASIC for IBL and SLHC outer layers, 336 rows x 80 columns, 22.5x19.1 mm$^2$) : only standard version of guard rings. p-spray and moderated p-spray
- **FE-I3** (10.4x9.8 mm$^2$): standard and slimmed edges versions. Design compatible with dry etching process
- **Microstrips** (RD50 design) to study with an easier read-out the performances of devices with a slimmed edges. Investigation of isolation methods

**NOT THE FINAL DESIGN- ONLY TO SHOW THE RELATIVE DIMENSIONS**



# Overview of sensor structures (II)



- n-in-n batch

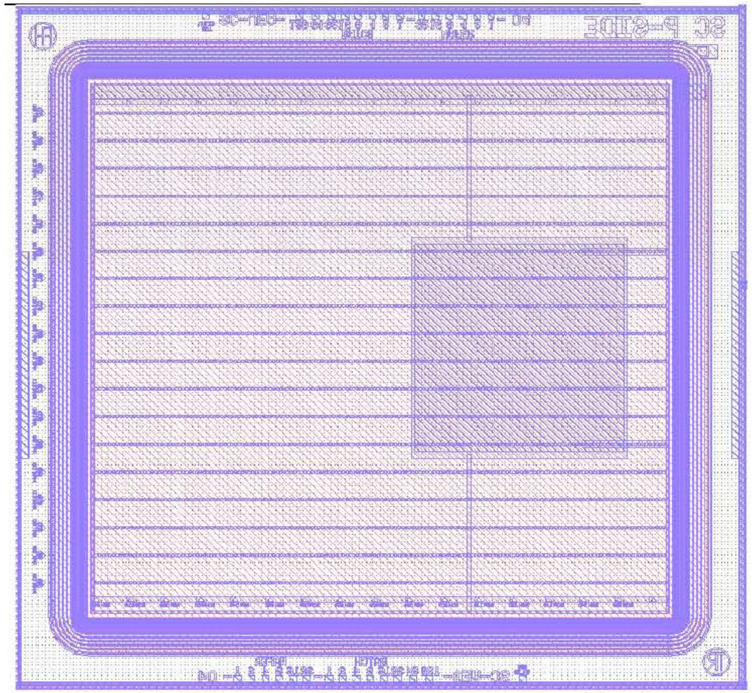
  - Single Chip Module FE-I4 sensor
  - FE-I3 Single Chip variants: Standard version

    Slim edge versions

    - Less guard rings (perhaps only one or even none at all, after irradiation they could be dispensable )
    - Pixel opposite guard rings
    - Both versions combined

    n-in-p design on n-bulk wafer

    - The sensor would only work after radiation induced type bulk inversion
    - Direct comparison with n-in-p sensors possible



# Common test-structures

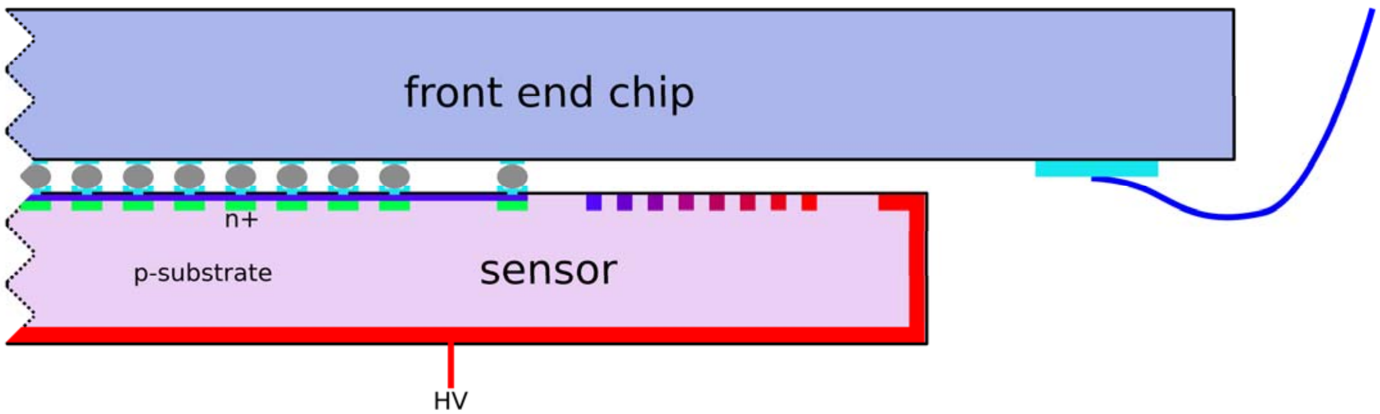
- Implementation of a common set of test-structure in the CiS , HPK and Micron productions

  - Diode
  - Mos
  - Micro-strip sensor (RD50 geometry)
  - FE-I3 Single Chip Module

- Choose homogenous p-spray as simplest isolation technique to compare. CiS and Micron production will not implement p-stop.

# P-type pixel modules

- Production on p-type material → need to isolate the FE chip from the HV present at the sensor edges on the front side
- A BCB layer as additional passivation on the sensor front side should provide the necessary isolation




- IZM can deposit BCB as a post-processing step on 4” wafers before the UBM step → additional mask needed
- Post-processing on full wafers

# Summary and Outlook

- Wafer submission in preparation to study the ultimate fluence limit at which planar sensors could be good candidates for the pixel systems at SLHC
- Parallel production of n-in-n and n-in-p pixel sensors on Fz and MCz silicon
- Application of RD50 results on n-side readout sensors to pixel geometries and read-out systems
- Optimization of the pixel geometries to achieve slimmed / active edges

- Open to insert devices / test structures in the two batches proposed by RD50 groups interested to join this submission

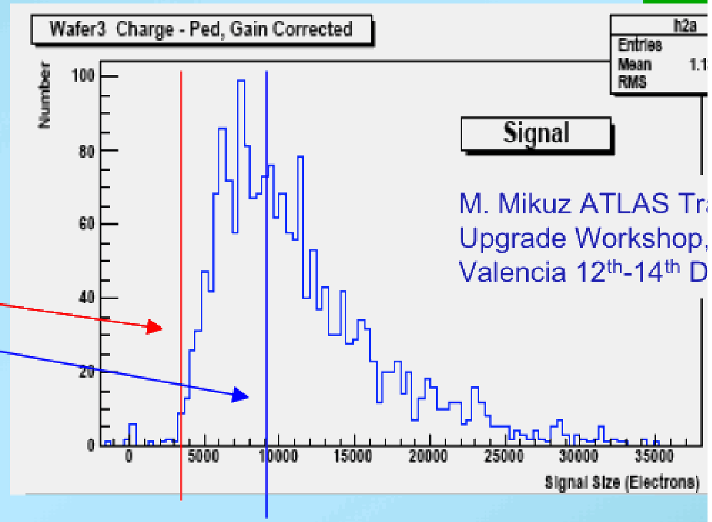
- PSI (T. Rohe) already interested in joining the submission (discussion under way on the structures to insert) for R&D on p-type pixel modules

# Back-up slides

# Pixel Sensor Efficiency: Signal/Threshold

**Signal is Landau (here Diamond):**

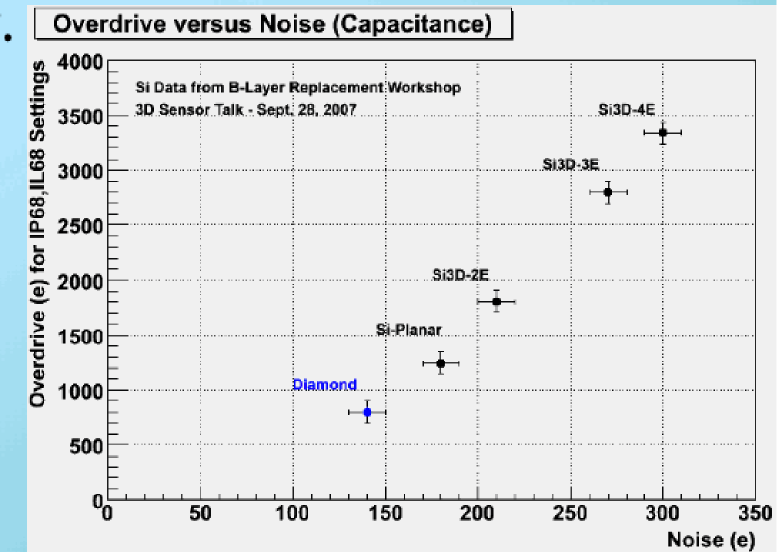
**Efficiency requires**
**Signal/Threshold > 2**




**Threshold**
**"bare" threshold is set as low as the system permits**
**Bare Threshold ~ 1500e for Diamond**
**~ 2500e for Silicon**
**(why does it not scale with noise?)**

**In order to fit the hit into the beam crossing of 20 ns, the signal has to exceed the threshold by the "overdrive".**
**In-time Threshold = bare threshold + overdrive**

**Overdrive scales with noise**




**Signal needs to be > 2x In-time Threshold:**

| Sensor | Threshold [e] | | | Required Signal [e] |
|---|---|---|---|---|
| | Bare | Overdrive | In-time | |
| Si planar | 2500 | 1300 | 3800 | 7600 |
| Si 3D 2E | 2500 (?) | 1800 | 4300 | 8600 |
| Si 3D 3E | 2500 (?) | 2800 | 5300 | 10600 |
| Si 3D 4E | 2500 (?) | 3400 | 5900 | 11800 |
| Diamond | 1500 | 800 | 2300 | 4600 |

C. daVia ATLAS B-Layer Workshop, CERN Sep. 28-30. 2(
O. Roehne ATLAS Tracker Upgrade Workshop, Valencia 12th-14th De