LHC Beam Loss Monitor

Realisation

LHC Machine Protection System Review

LHC Beam Loss Monitor

- BLM Overview
- Tunnel
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  - Frameword for Transmission
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- Surface
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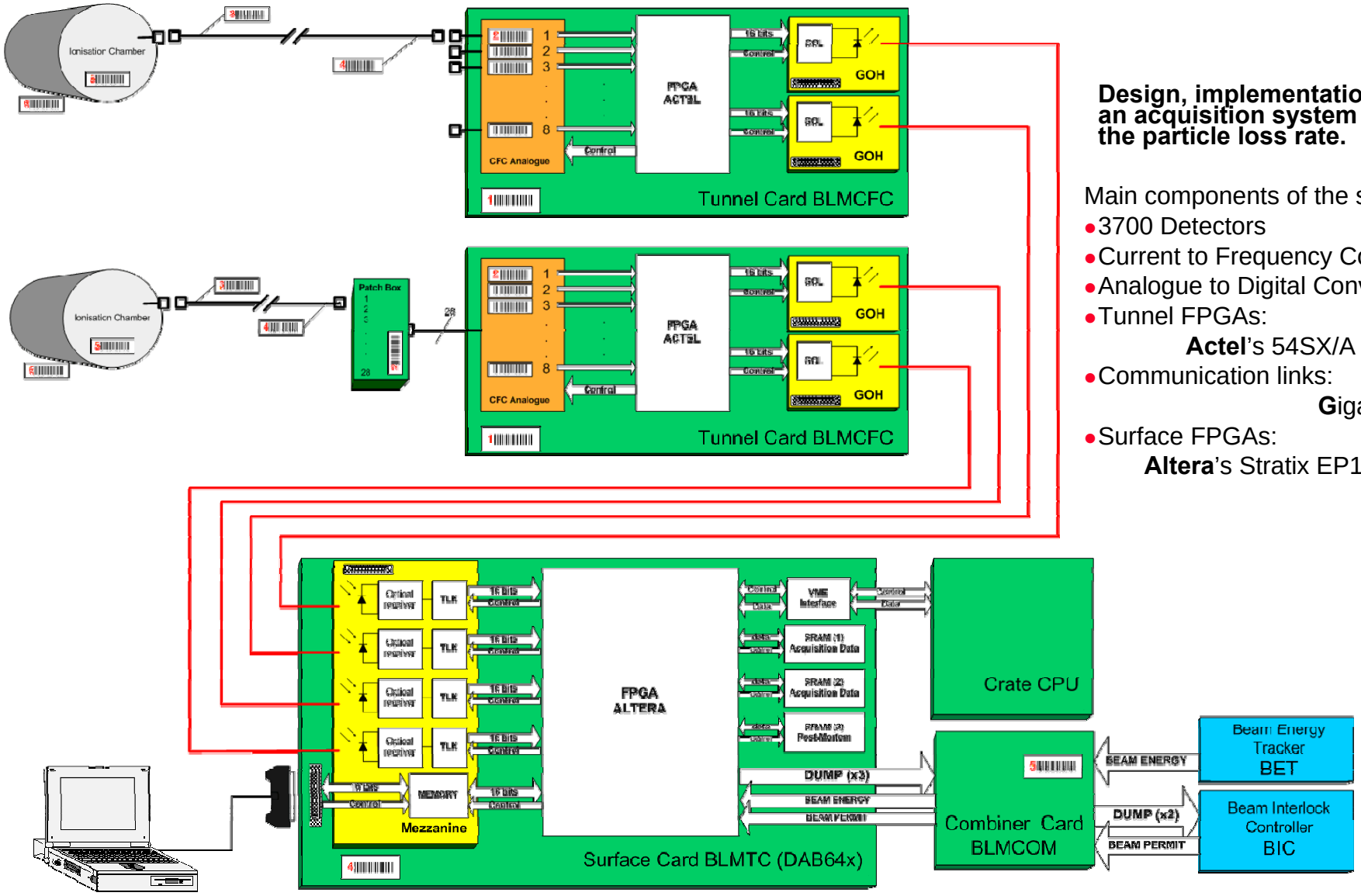
  - Real-Time Analysis of Data
  - Combiner Card (BLMCOM)
  - Failsafe Surface System
- Reliability Study

BLM Overview



Design, implementation and testing of an acquisition system that measures the particle loss rate.

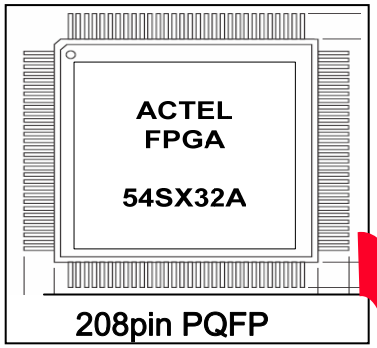
Main components of the system:

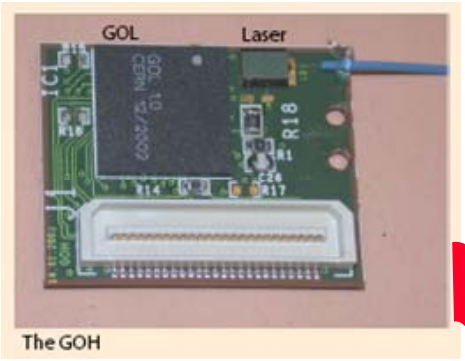
- 3700 Detectors
- Current to Frequency Converters (CFCs)
- Analogue to Digital Converters (ADCs)
- Tunnel FPGAs:
  Actel's 54SX/A radiation tolerant.
- Communication links:
  Gigabit **O**ptical **L**inks.
- Surface FPGAs:
  Altera's Stratix EP1S40 with 780 pin.

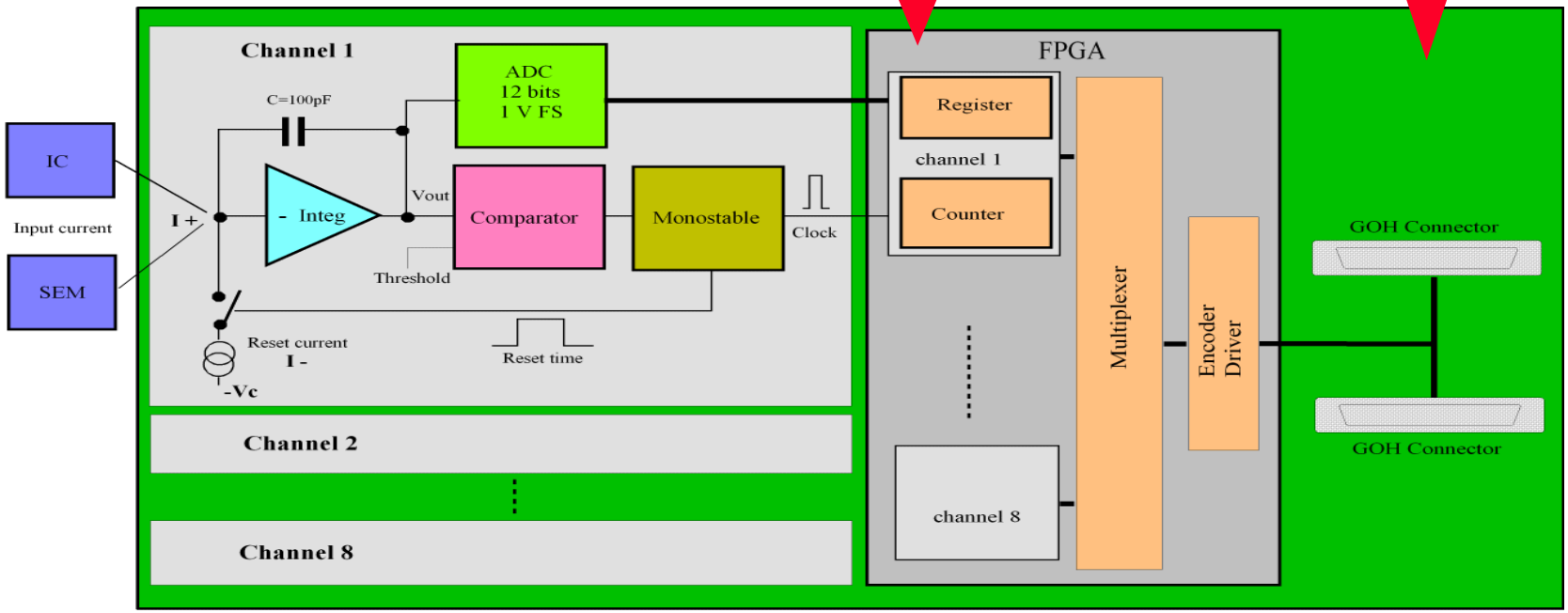
Tunnel Card (BLMCFC)

Design Criteria Keypoints:

- **Radiation Environment**
  - **Radiation Tolerant Devices available**
  - **Actel SX/A family (54SX32A)**
  - **Qualification/Irradiation tests**
- **Not very complicated digital part design but**
  - **Triple modular redundancy (TMR)**
  - **8 channels**
- **Large Dynamic Range**
  - **Current-to-Frequency Converter**
  - **Analogue-to-Digital Converter**







Tunnel Card's Design Choices

Basic components used:

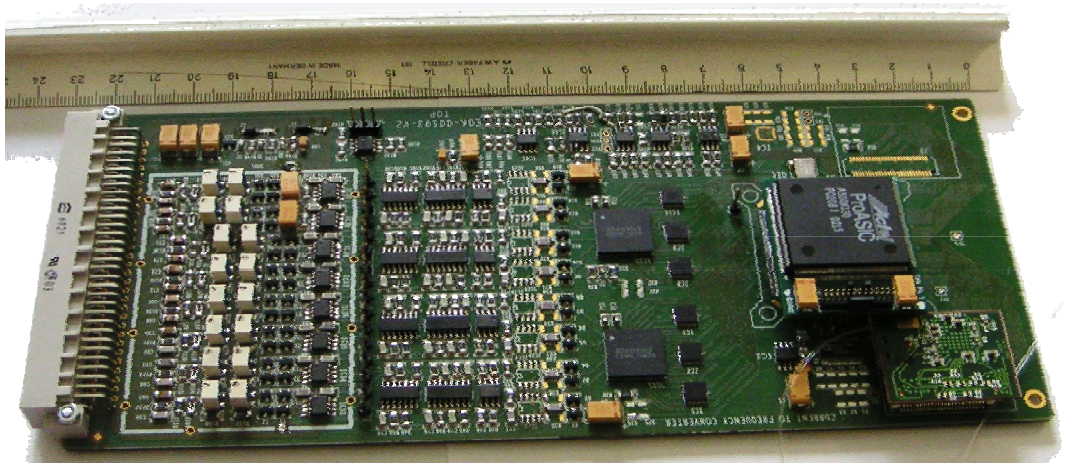
Off-the-shelves

- **Current-to-Frequency Converter** (x8)
  - Irradiation tests at cyclotrons of Lauvain and PSI
- **Actel FPGA (54SX32A)** (x1)
  - 208 pin
  - 32,000 LE
  - One-time-programmable
  - Redundant Inputs
    - Triple counter inputs
  - Redundant outputs
    - Double 16bit data bus
    - Double 4bit control bus

CERN Custom ASICs

- **A/D Converter AD74240 CMOS** (x2)
  - Quad 12bit
  - 40Ms/s
  - Parallel output
- **Line Driver LVDS_RX CMOS** (x6)
  - 8 LVDS to CMOS line receivers
- **Temperature Sensor DCU2** (x1)
  - 12 bit output
- **GOL (Gigabit Optical Link)** (x2)
  - Analogue parts needed to drive the laser.
  - Algorithm running that corrects SEU.
  - 8b/10b encoding.
  - 16 or 32 bit input.
  - Error reporting (SEU, loss of synchronisation,..)

Figure: CFC card top view.



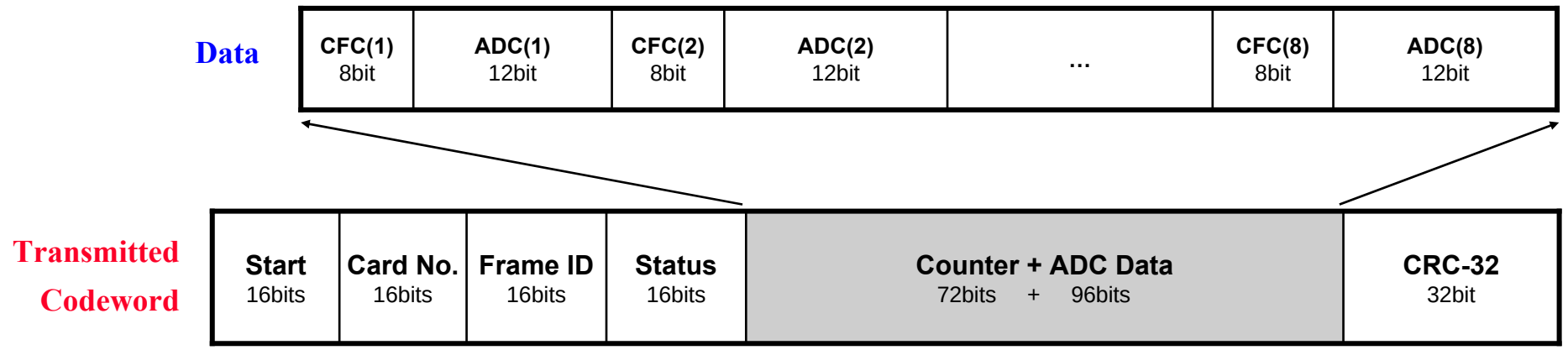
Part Name	Integral Dose (KGy)*
C/F Converter	0.5
ACTEL	3.2
AD41240	10
LVDS_RX	10
DCU2	10
GOH	3.14

Table: Radiation dose withstood by component without error.

*** For 20 years of nominal operation it is expected to receive around 200 Gy.**

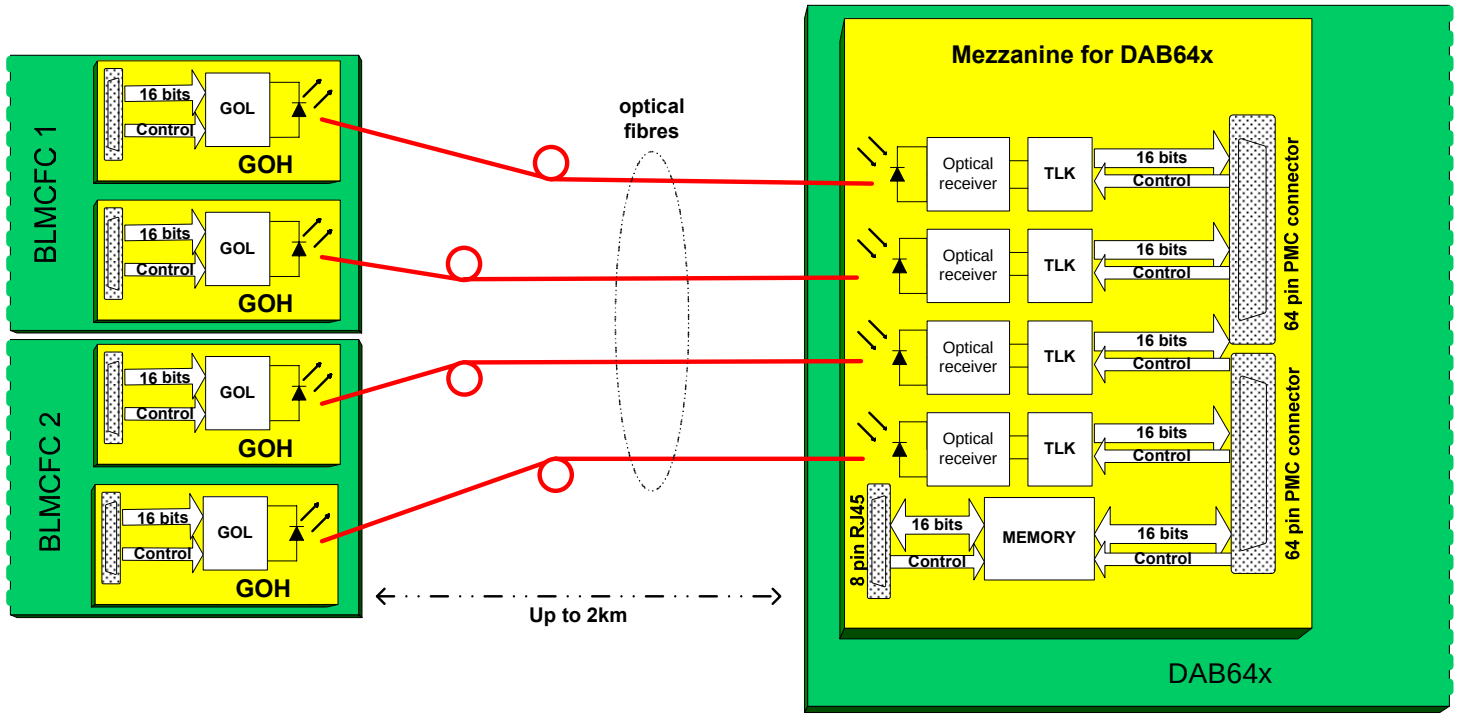
Frameword for Transmission

- **Formatting of the frameword for transmission (256 bits)**



- **Transmission of frameword every 40μs.**
  - **The data rate must be high enough to minimise the total latency of the system .**
- **Redundant optical link**
  - **In order to increase the reliability and the availability of the system.**

Mezzanine Cards



- Redundant transmission
- High radiation tolerance
  - > 3 KGy
- 800 Mbps
  - Data 640 Mbps
- 8bit/10bit encoding

- 4 optical diodes
- 4 TLK (Texas Instruments) transceivers
  - 8bit/10bit decoding
  - Synchronisation
  - Clock extraction
- 1MB non-volatile RAM
  - Programmable either via FPGA or RJ45

Steps taken for a Failsafe Tunnel System

To ensure Ionisation Chamber connection:

- **Modulation Tests**
  - Tests initiated when no beam present.
  - Sine wave checks the connection and the ADC.
  - Rectangular wave checks the connection and the CFC.

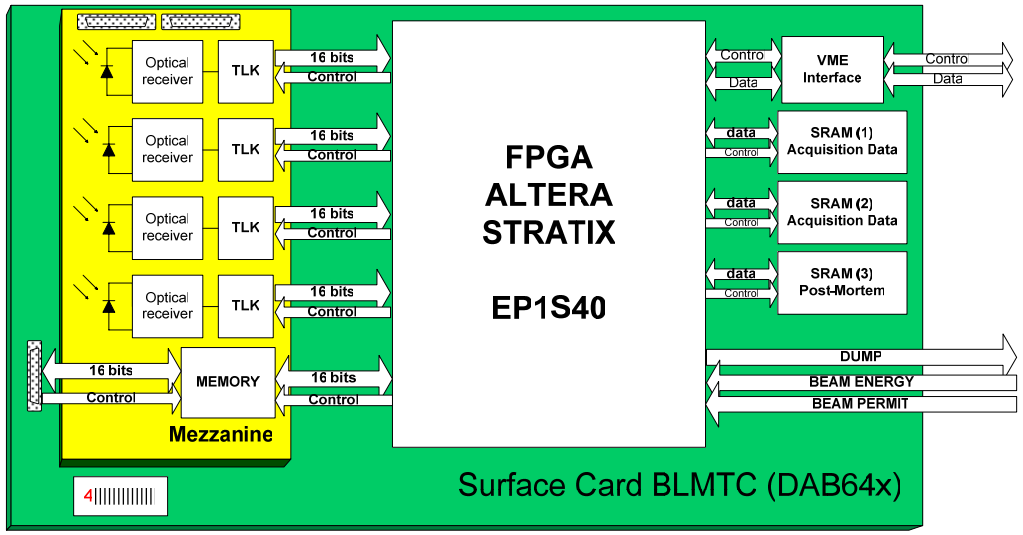
To ensure CFC card correct operation:

- **Constant Current**
  - A current (~10pA) is applied constantly.
- **Status monitor**
  - High tension check.
  - Temperature

To minimise SEU:

- **Radiation Tolerant Components**
  - Custom ASICs,
  - No Configuration Data,
  - Radiation Qualification.
- **TMR (triple modular redundancy)**
  - FPGA design tripled and added voting.
- **Doubled/Tripled I/Os**
  - Tripled Counter inputs.
  - Doubled Data and Control outputs.

Surface Card (BLMTC)

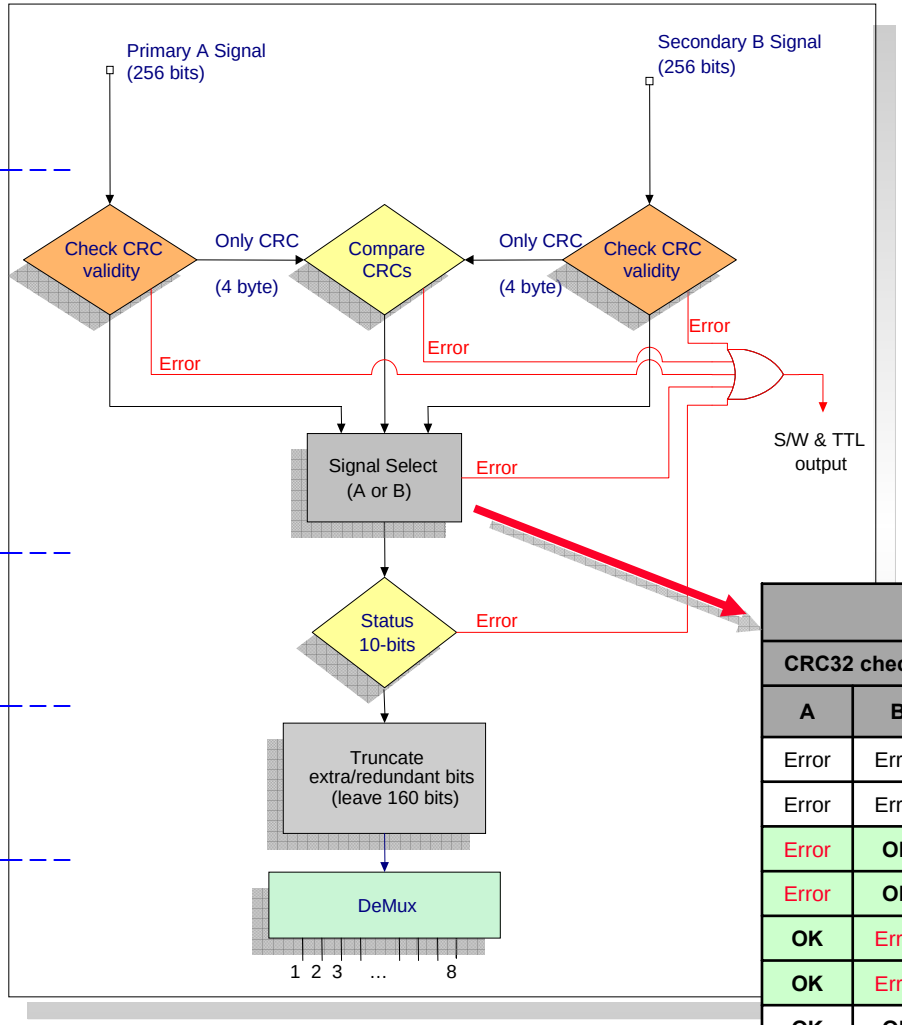


Stratix Device Features	
Feature	**EP1S40**
LEs	41,250
M512 RAM blocks (32 ×18 bits)	384
M4K RAM blocks (128 ×36 bits)	183
M-RAM blocks (4K ×144 bits)	4
Total RAM bits	3,423,744
DSP blocks	14
Embedded multipliers	112
PLLs	12
Maximum user I/O pins	615

DAB64x specifications

- **Stratix FPGA**
  - **Vertical Migration to EP1S40**
- **SRAM memories**
  - **512K x 32bit**
- **Connectors for Mezzanine**
  - **2 x 64pin PMC connectors**
  - **Provide 3.3V, 5V, GND, and**
  - **Connection to 114 FPGA I/O pins.**
- **Card bus**
  - **VME64x**

Transmission Check & Tunnel Status



At the Surface FPGA:

- **CRC-32**
  - Error check / detection algorithm for each of the signals received.
  - Comparison of the pair of signals.
- **Signal Select block**
  - Logic that chooses signal to be used
  - Identifies problematic areas.
- **Tunnel's Status Check block**
  - HT, Power supplies
  - FPGA errors
  - Temperature

Signal Select Table

CRC32 check		Comparison of 4Byte CRCs	Output	Remarks
A	B			
Error	Error	Error	Dump	Both signals have error
Error	Error	OK	Dump	S/W trigger (CRCgenerate or check wrong)
Error	OK	Error	Signal B	S/W trigger (error at CRC detected)
Error	OK	OK	Signal B	S/W trigger (error at data part)
OK	Error	Error	Signal A	S/W trigger (error at CRC detected)
OK	Error	OK	Signal A	S/W trigger (error at data part)
OK	OK	Error	Dump	S/W trigger (one of the counters has error)
OK	OK	OK	Signal A	By default (both signals are correct)

Quench Level Thresholds

Threshold values depend on

- **Beam Energy and**
- **Integration Time (Loss Duration)**

The acquisition card transmits a value which corresponds to the particles seen over the integration time of 40μs.

- **Using this values the surface FPGA calculates and keeps 11 more running sums per detector.**
- **The max integration time needed to be observed is 100s.**
- **The intermediate observation points are found by identifying the places where the approximation introduces the minimum fitting error.**

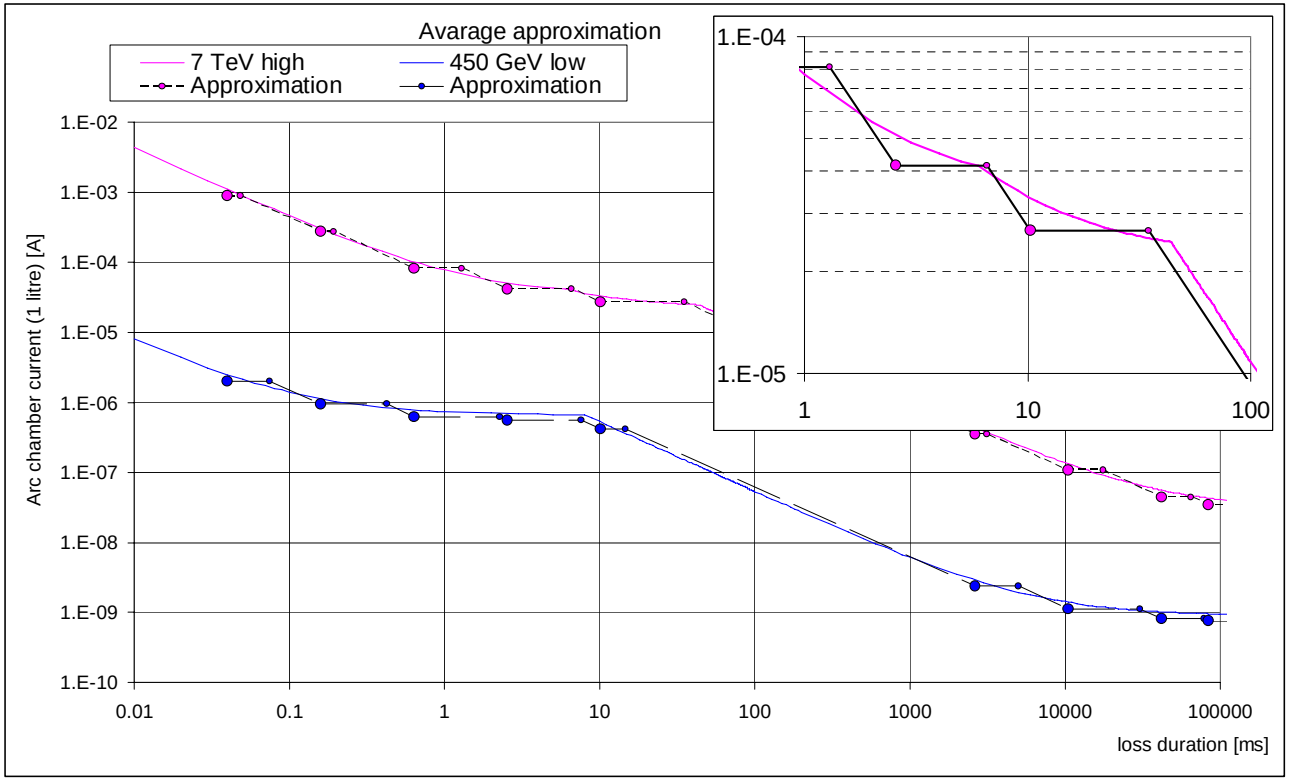
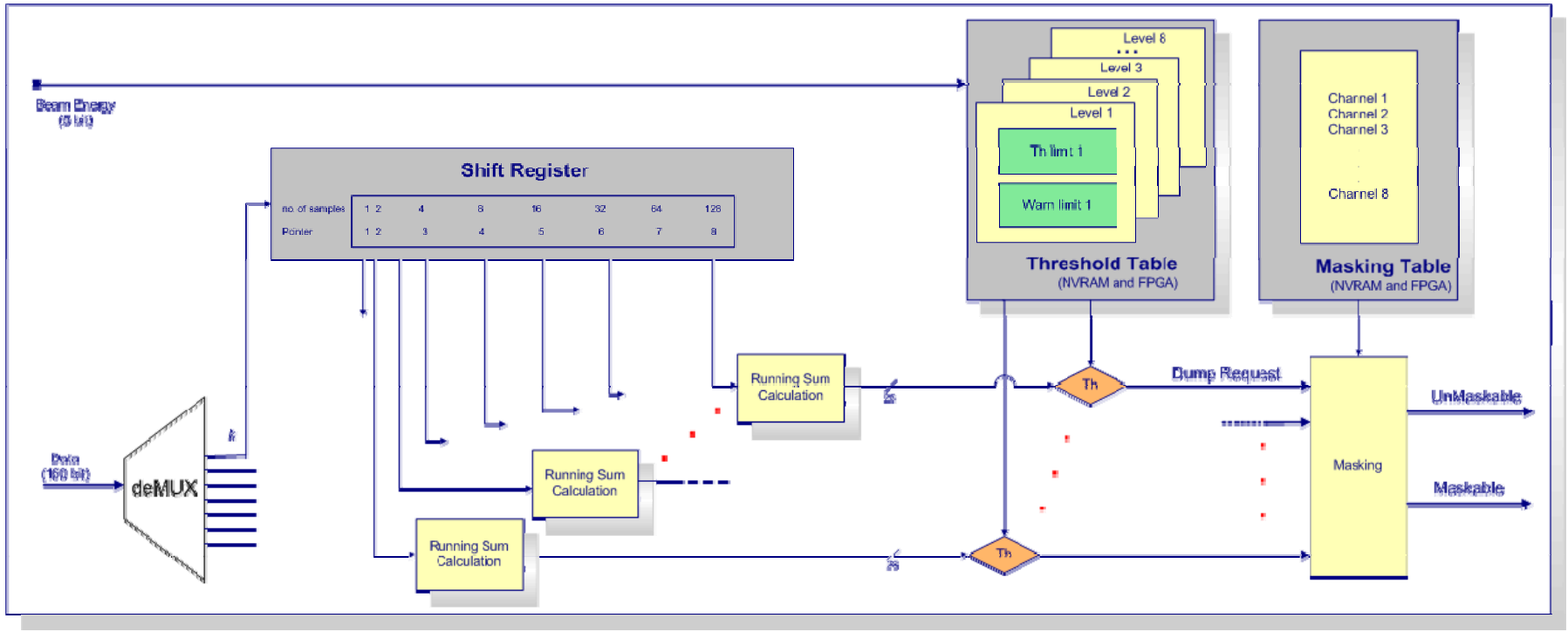


Figure and error calculations by G. Guaglio

Real-Time Analysis of Data



Running Sums

- Multi-point Shift Registers holds data
- Successive calculation
- 100μs-10ms (System A)
  - 5 Running Sums
  - Max. values of the last second
- 10ms-100s (System B)
  - 6 Running Sums

Threshold Table

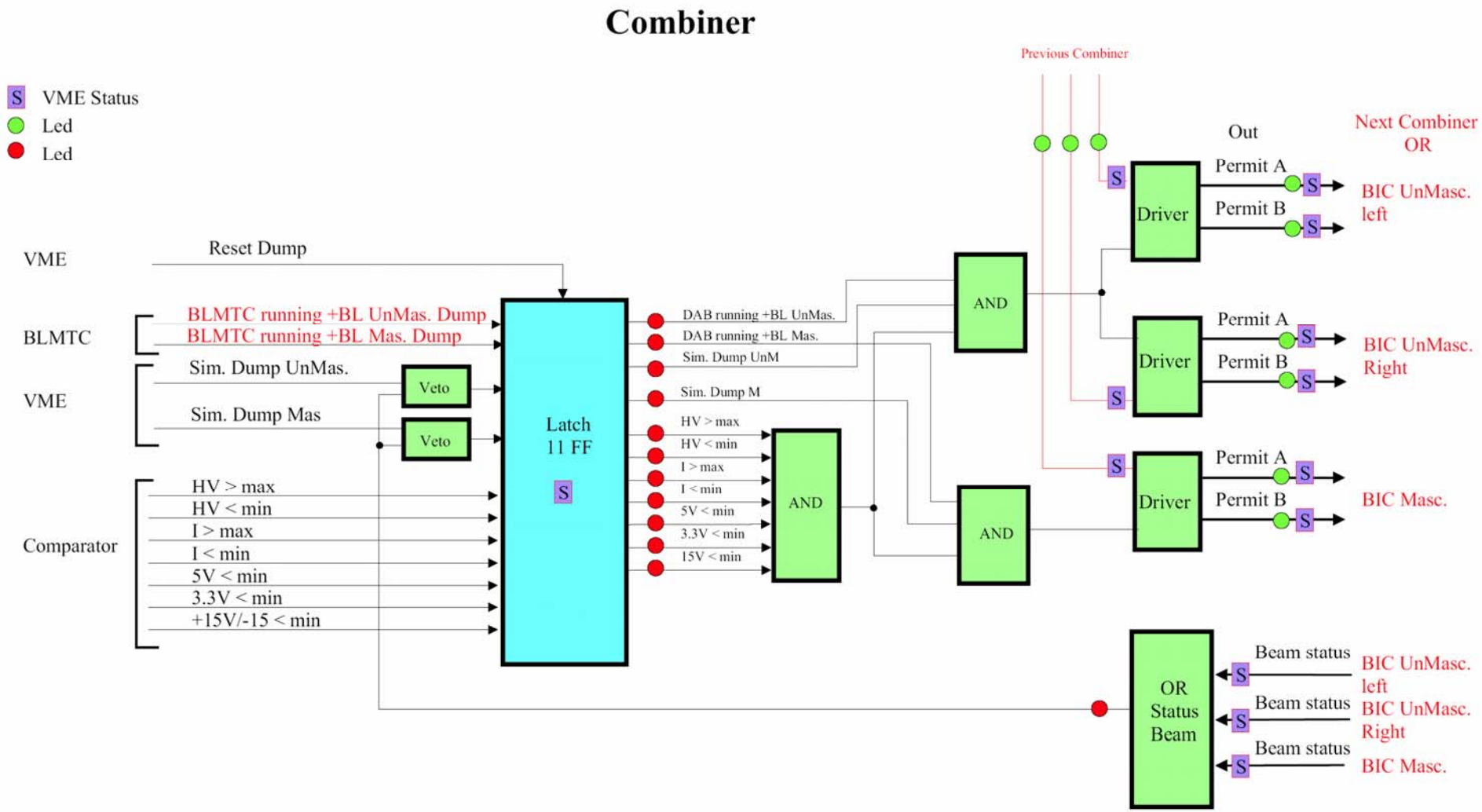
- Threshold depends on energy and a acquisition time.
- Unique thresholds for each detector.
- Read at system power-on from an external Non-Volatile RAM.

Masking Table

- Masking of channels is allowed only when safe.
- Unique masking table for each card.
- Read at system power-on from an external Non-Volatile RAM.

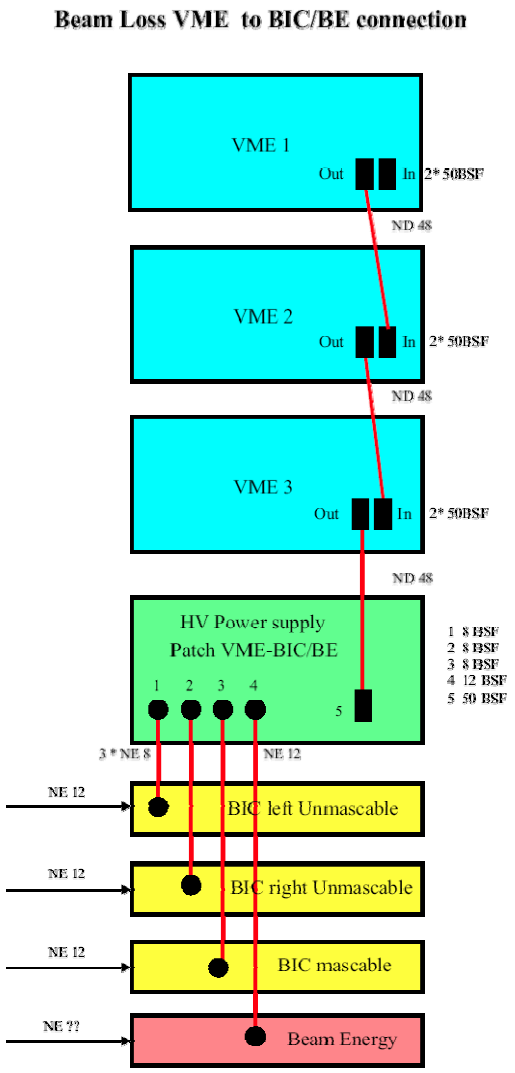
Combiner Card's Beam Permit Logic

Gianfranco Ferioli



Combiner Card Arrangement

Gianfranco Ferioli



- One combiner card per crate
- Daisy-chained
- Distributes to all BLMTC cards
  - Beam Energy
  - Beam Status
- Collects from all BLMTC cards
  - Card running
  - Maskable Dump
  - Unmaskable Dump
- Checks status of all power supplies
- High Tension Modulation Tests

Steps taken for a Failsafe Surface System

To ensure a reliable communication link:

- **Double (redundant) optical link**
- **CRC-32 error check algorithm**
  - All single-bit errors.
  - All double-bit errors.
  - Error detection – four times more characters.
  - Any odd number of errors.
  - Any burst error with a length less than the length of CRC.
  - For longer bursts $Pr = 1.16415*10^{-10}$ probability of undetected error.
    - 224 bits of data + 32 bits of CRC remainder = 256 bits.
- **8b/10b encoding**
  - Clock data recovery (CDR) - guarantees transition density.
  - DC-balanced serial stream - ones and zeros are equal/DC is zero.
  - Special characters used for control – sync, frame.
    - 256 bits of data are encoded in 320 bits = 64 extra bits.

To avoid misplacement of threshold and/or masking table

- **Card ID**
  - Each tunnel card holds a unique 16bit number
  - Included with every transmitted frame
  - Compared with the one loaded together with the tables

To avoid loss of data

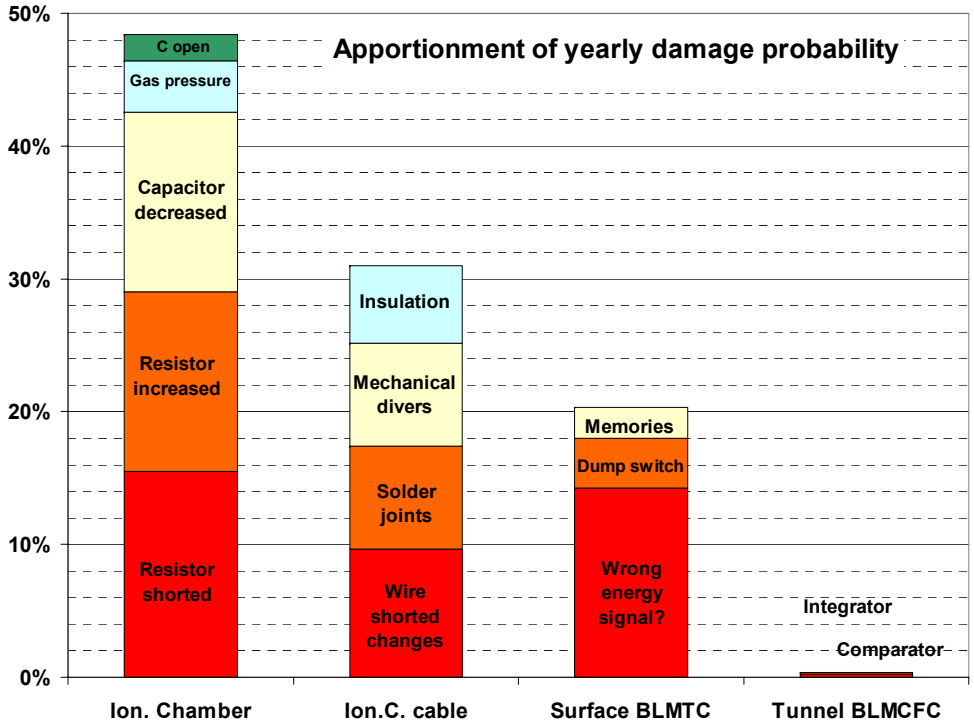
- **Frame ID**
  - Surface FPGA checks for missing frames
  - 16bit Frame ID number increments by one and is included at every transmission

To ensure recognition of system failures and dump requests

- **Outputs (Dump signals) from the FPGA as frequency**
  - At a dump request, reset, or failure the transmitted frequency will be altered.
- **Outputs (Dump signals) from the surface cards are daisy chained**
  - Using the VME backplane as interconnection
  - Card disconnection and/or failure is immediately recognisable by the Combiner card.

Reliability Study

by G. Guaglio



Relative probability of a system component being responsible for a damage to an LHC magnet in the case of a loss

- More than 80% from the Ionisation Chamber

Relative probability of a BLM component generating a false dump.

- ~98% from components that are in the tunnel