Feedback Control of E-Cloud Instabilities

Ideas from Instability Control in Lepton Colliders

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November 2008

LARP Ecloud Contributors

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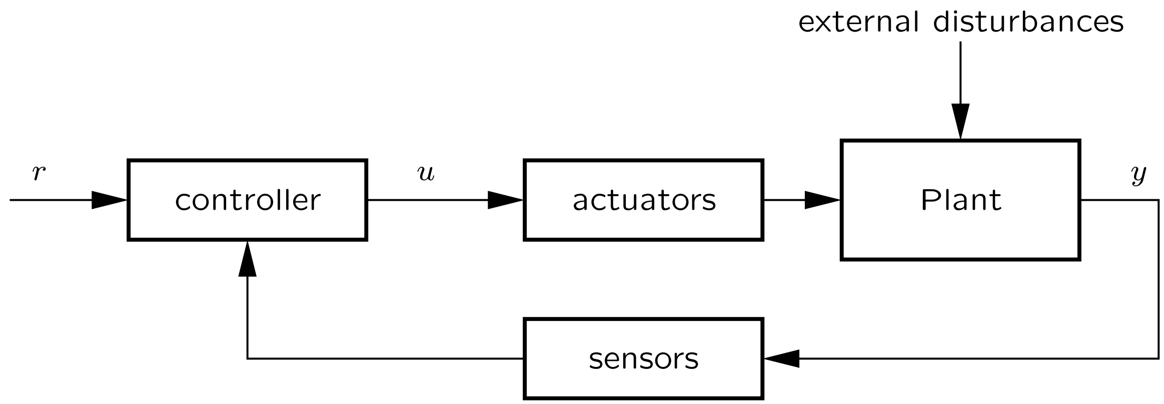
Feedback basics

The objective is to make the output *y* of a dynamic system (plant) behave in a desired way by manipulating input or inputs of the plant.



Regulator problem - keep *y* small or constant

Servomechanism problem - make *y* follow a reference signal *r*

Feedback controller acts to reject the external disturbances.

The error between *y* and the desired value is the measure of feedback system performance. There are many ways to define the numerical performance metric

- RMS or maximum errors in steady-state operation
- Step response performance such as rise time, settling time, overshoot.

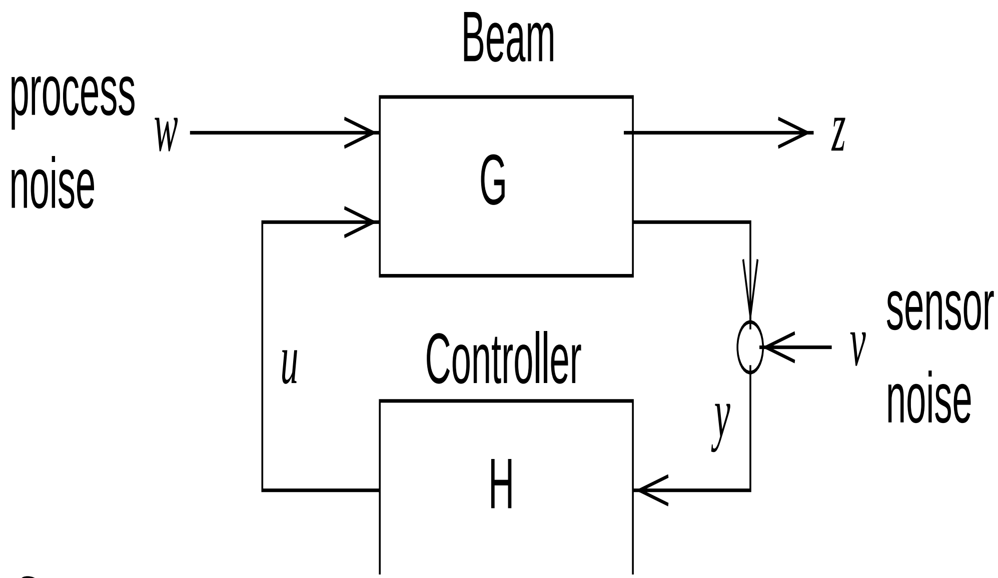
An additional measure of feedback performance is the average or peak actuator effort. Peak actuator effort is almost always important due to the finite actuator range.

Feedback system robustness - how does the performance change if the plant parameters or dynamics change? How do the changes in sensors and actuators affect the system?

Beam Dynamics Feedback Principles - General Overview

Principle of Operation-Feedback can be used to change the dynamics of a system

Transverse - measure(δX, δY) - kick in X', Y'



Longitudinal - measure $\delta\phi$ - correct E

Technical issues

Loop Stability? Bandwidth? Noise? Emittance blow-up?

Pickup, Kicker technologies? Required output power?

Processing filter? DC removal? Saturation effects? Diagnostics (system and beam)?

Overview of Feedback Options for E cloud control

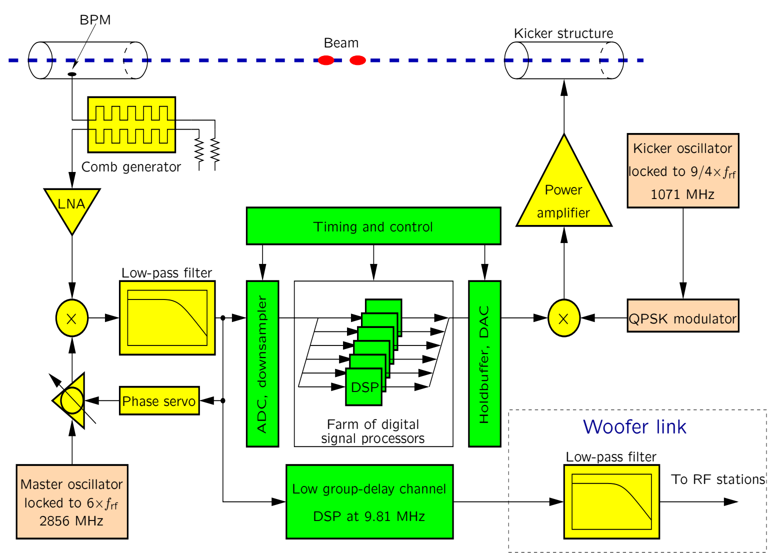
example/existing centroid systems 2 ns sampling (PEP-II, KEKB, ALS, Elettra, SLS, etc.)

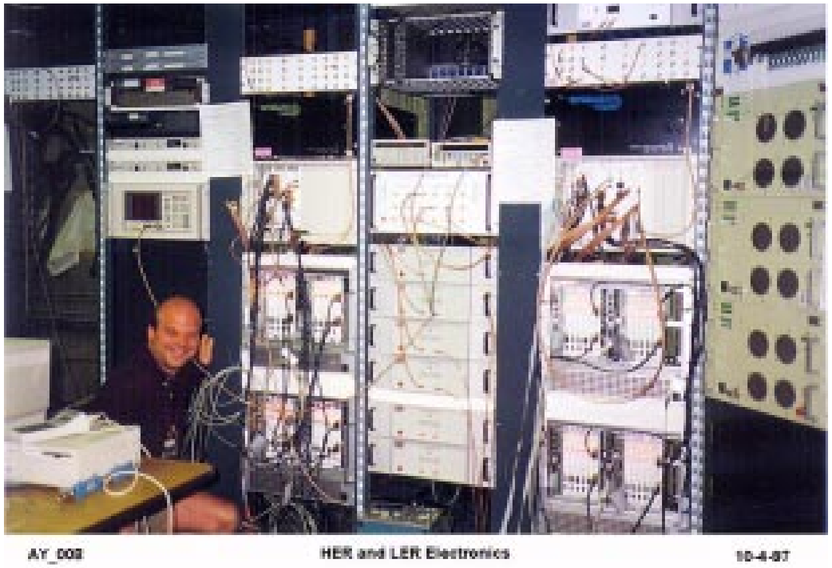
- Diagonal controller formalism treats each bunch as rigid object
- Maximum loop gain from loop stability and group delay limits - 1 turn delay minimum
- Maximum achievable instability damping from receiver noise floor limits

Electron-cloud effects act within a bunch (effectively a single-bunch instability) and also along a bunch train (coupling near neighbor bunches)

SPS and LHC needs may drive new processing schemes and architectures

Existing Bunch-by-bunch (e/g diagonal controller) approaches may not be appropriate





Processing Requirements

For instability control, the processing channel must

- extract (filter) information at the appropriate betatron or synchrotron frequency,
- amplify it (a net loop gain must be generated, large enough to cause net damping for a given impedance)
- generate an output signal at an appropriate phase (nominally 90 degrees, but arbitrary if the system and cable delays, pickup and kicker locations are considered)

Some technical issues

- Bandwidth/sampling rate (2500 - 4000 MHz?)
- DC offset removal from the processing channel (e.g. from DC synchronous phase position, or static orbit offset)
- Saturation on large input errors
- Noise in the input channel (e.g. bandwidth reduction via processing filter)
- Maximum supportable gain - limits from noise as well as loop stability
- Diagnostics (processing system and beam dynamics)
- Wideband pickups and kicker systems

Filter Implementation Options

Terminology

- Time domain - bandpass bunch by bunch filters
- frequency domain - modal selection, notch at Frev

Sampling process suggests discrete time filter (filter generates correct output phase, limits noise, controls saturation)

General form of IIR filter (infinite impulse response)

$$y_n = \sum_{k=1}^{N} a_k y_{n-k} + \sum_{k=0}^{M} b_k x_{n-k}$$

General form of FIR filter (finite impulse response)

$$y_n = \sum_{k=0}^{M} b_k x_{n-k}$$

wide bandwidth filter - insensitive to variations in machine tune

narrow bandwidth filter - helps reject detector noise

Maximum gain - when noise in front-end saturates DSP processing

New directions -possible technical options

Matrix (modal) controller (corrections from off-diagonal signals)

Wideband single-bunch (slice) correction (Ghz bandwidth, DSP or electro-optic processing)

- 4 - 8 GS/sec. bunch coordinate sampling (take advantage of 25 ns bunch spacing)
- Adaptive control filters
- time varying filters? time varying gain?

Multiple pickups (M pickups, spaced at various betatron phases)

Multiple kickers

Hybrid Fast Feedforward (< 1 turn) in combination with multi-turn Feedback?

(feed forward lowers growth rates to scale where feedback over several turns is feasible)

Less than 1 turn group delay needed?

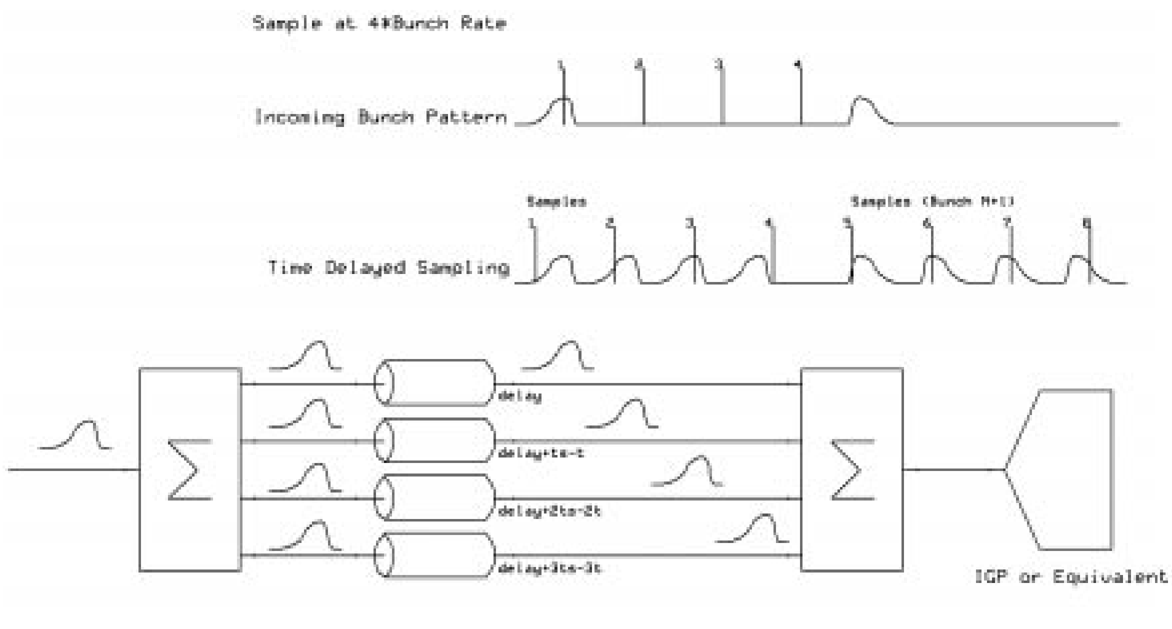
- via matrix correction algorithm
- via signal transmission across the ring

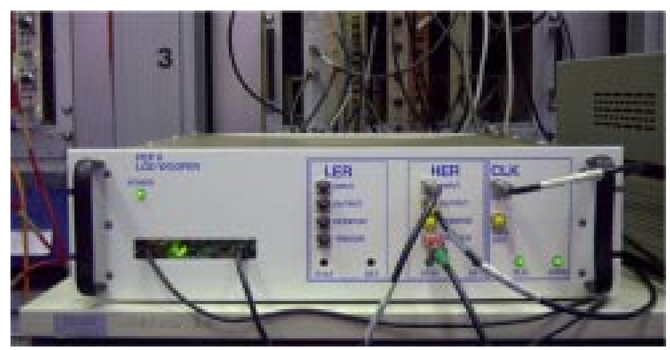
New directions -possible technical options, II

4 - 8 GS/sec. bunch coordinate sampling (take advantage of 25 ns bunch spacing)

Instrumentation for SPS measurements - use existing iGp

- iGp - 500 MS/sec. platform in use at Frascati, KEK (transverse coupled-bunch feedback)
- Gboard - 1.5 Gs/sec. proof of principle lab study





- 1200 MHz Sampler bandwidth resolves high frequency structure on beam (pickups?)

LARP Fundamental feedback technology R&D

Low-noise transverse coordinate receivers and pickup techniques - 2008/2009

(Joint SLAC/KEK study with M. Tobiyama -noise floor sets damped beam motion and influences equilibrium emittance)

4 - 8 GS/sec. bunch coordinate sampling and output kick

(necessary to resolve modes within the 1 - 2 ns bunch length)

Lab effort - prototype 4 GS/sec. back end (2008/2009 Joint SLAC-KEK study)

High-Speed Matrix computation channels (existing 1.5 GS/sec. design - expand?)

(digital signal processing architectures)

Low latency computation/processing/physical implementation approaches

(necessary for <1 turn correction group delay)

Wideband Pickups, Wideband Kickers (2009/2010)

Biggest Issue to resolve - time scale of instability growth (simulations, beam measurements)

E+ ring DAFNE E Cloud study in the horizontal plane

Horizontal plane growth rate measurements vs. bunch spacing. The fastest growing modes are low frequency (typically mode -1)

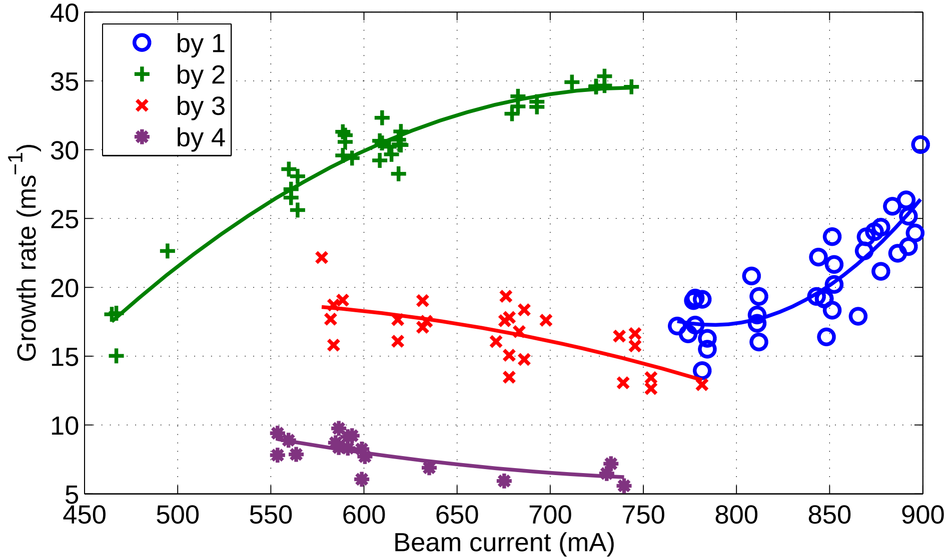
- non-linear current dependence of growth rate,
- oscillation frequency
- variation with bunch spacing

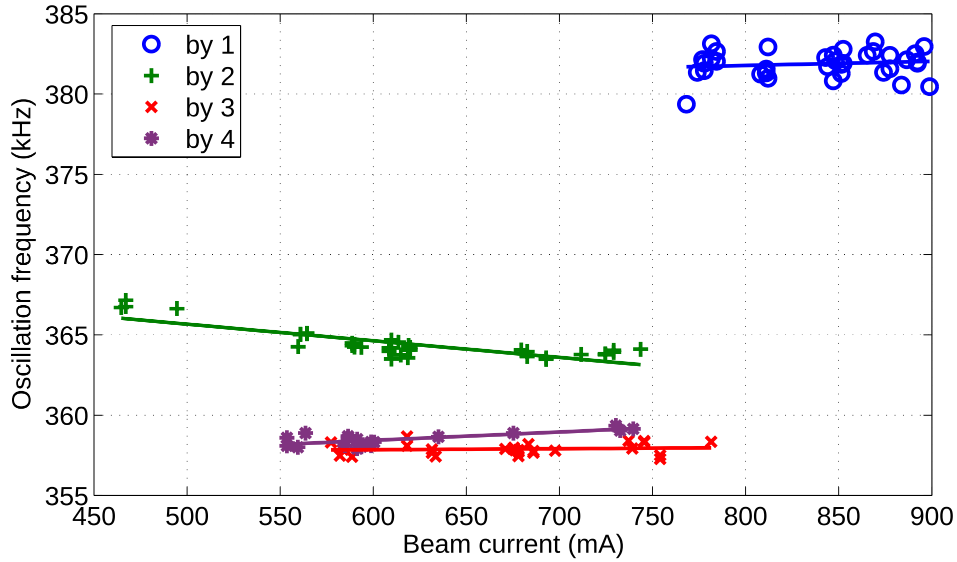
are suggestive of an electron cloud effect (inconsistent with a simple resistive wall instability)

The data are taken using a digital Gproto system via transient-domain (grow-damp) excitations

(From D. Teytelman, et al)

Figures from “Design and Testing of Gproto Bunch-by-bunch Signal Processor.” D. Teytelman, C. Rivetta, D. Van Winkle, R. Akre, J. Fox, A. Krasnykh (SLAC), A. Drago (Frascati). SLAC-PUB-11943, Jul. 18, 2006. 4pp.Contributed to European Particle Accelerator Conference (EPAC 06)





Summary and LARP SPS and LHC Ecloud FY2009 proposal

Based on the FY2008 results, LARP plans a more detailed effort in 2009

- develop a beam dynamics/feedback dynamics simulation model
- develop the detailed requirements for a new wideband feedback system architecture
- Proof-of-principal technology R&D on GHz bandwidth (e.g. 2 - 4 GS/sec.) processing, backend

SPS Machine Physics studies, development of transient-domain instrumentation

Modelling, estimation of E-Cloud effects

Modelling of closed-loop system dynamics, estimation of feedback system specifications

Evaluation of possible control architectures, possible implementations

Technology R&D - Specification of wideband feedback system technical components

- wideband RF instrumentation, high-speed digital signal processing
- SLAC/LBL have extensive collaboration associated with instability control, feedback signal processing and high-power beamline kicker components

2009 LHC (dipole) Bunch-by-Bunch Feedback commissioning

SPS E-Cloud and Instability Control

Studies by Arduini, et al and simulations by Rumolo, et al identify key accelerator physics parameters of SPS Ecloud dynamics (many contributors in these areas)

- Horizontal - coupled-bunch behavior
- Vertical - single bunch-like instability, evidence of 700 MHz structure in bunch
- time scales - consistent with several machine revolutions

PSR proof of principle instability feedback experiment by Macek et al

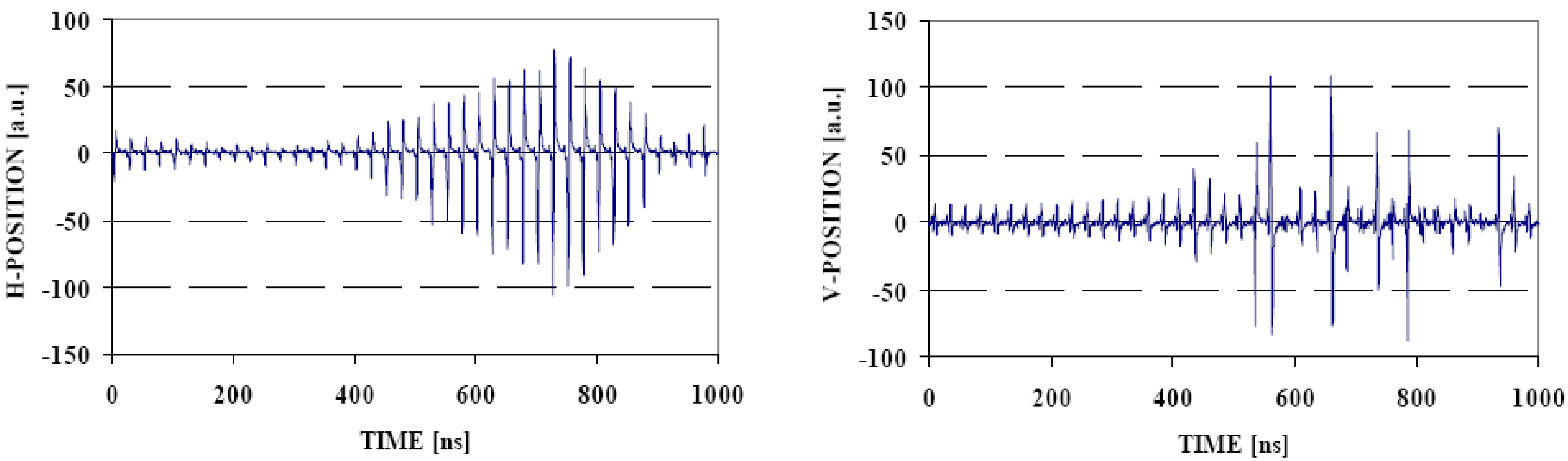


Figure 6. Snapshot of the horizontal (left) and vertical (right) position of the first 48 bunches of the LHC bunch train. $N_b = 0.8\times10^{11} > N_{th} \sim 0.2\text{-}0.3\times10^{11}$.

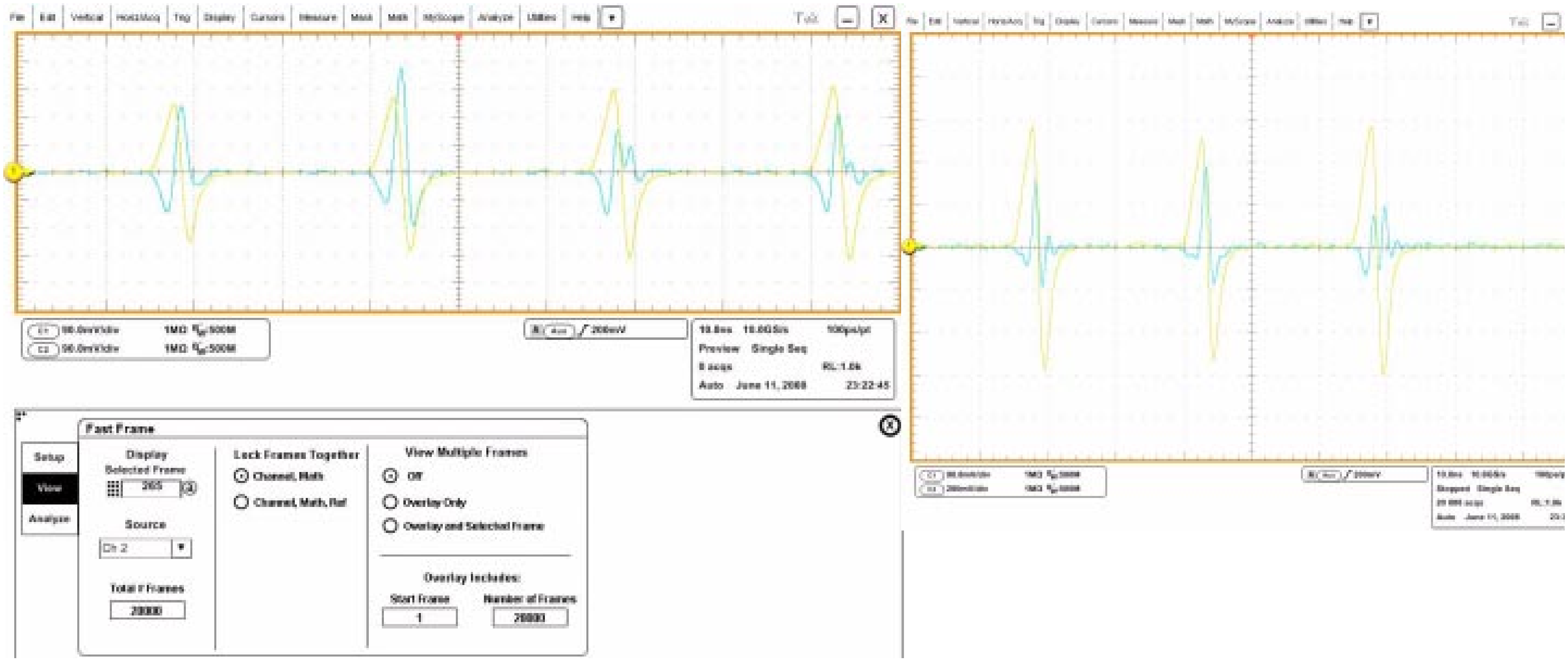
(Figure from Arduini, et al Ecloud 2004 proceedings)

Results from the June 6 MD

W.Hoefle, G. Rumolo, G. Arduini, R. De Maria, J. Byrd et al -

- Dedicated MD in SPS during machine scrubbing
- intensity 1E11 P/bunch, 25 ns separation, 72 bunches/batch, 5 batch injection (4 nominal LHC)
- lowered chromaticity to reduce damping - transverse signal seen after 5th batch injection

Transverse signals from exponential stripline couplers, hybrids (yellow sum, blue vertical)



Results from the August 12 MD

Follow-on from June MD

J. Fox, W. Hoefle, R. De Maria, G. Arduini, G. Rumolo, J. Thompson et al

Tunnel Access to SPS - measure exponential coupler matching, find/fix lousy connections

Move difference hybrids from tunnel to control room, match lengths of long Heliax

Sort out issues with hybrids, measure best 3, build simple receiver

Prepared data recorder, software, use wideband 2 GHz bandwidth, 50 ohm input Z, etc.

MD rescheduled twice from 8/11, finally get 2 AM to 10AM Aug13

Results

4 batches 1E11 P/bunch, 25 ns spacing, 72 bunches batch- better vacuum than June?

lowered chromaticity per June but 4 not 5 batches

NO 700 Mhz Transverse signal at high frequency observed (time or frequency domain)

lots of high-frequency signals > 1700 MHz observed - propagating modes in 10 CM vacuum chamber

added RF voltage modulation to try to excite quadrupole oscillation (increase density)

NO Ecloud-like signal observed

Progress Report - Ecloud/Feedback Modeling

J. Thompson (Cornell Undergrad) was supported by J. Byrd for 6 weeks at CERN July/Aug.

Project - adapt Ecloud model code from G. Rumolo (thanks to G. Rumolo/G. Arduini/W. Hofle)

Goal - examine dynamics with simple transverse feedback in model - explore

- Growth rates
- Modal patterns
- Bandwidth implications - explore dynamics with limited bandwidth feedback

Project summary

A very impressive start for an undergrad

Issues - “feedback model” has no noise, time delay, frequency response, imperfections

(correction is applied on same turn as transverse offset is sensed - no errors or delay*bandwidth limit)

Ecloud code uses 72 slices/bunch, but bunch length varies over time, so effective sampling rate of bunch structure changes. can’t directly transfer data to frequency domain to understand motion in frequency domain

Ecloud code had no coupled-bunch (dipole) impedances or instabilities

Initial suggestions- with this sort of “imaginary feedback” and 4 samples/bunch motion is suppressed

Goals -FY2008/2009 LARP Ecloud effort

2008/2009 -Better understand Ecloud dynamics via simulations and machine measurements

- Participation in E-Cloud studies at the SPS (June, August 2008)
- Analysis of SPS and LHC beam dynamics studies, comparisons with Ecloud models
- Participation in LHC transverse feedback system commissioning
- Adaptation of SLAC's transient analysis codes to SPS and LHC data structures

2009 -Develop reduced beam dynamics model to use in combined beam/feedback system model

Evaluate feasibility of feedforward/feedback techniques to control unstable beam motion, change dynamics

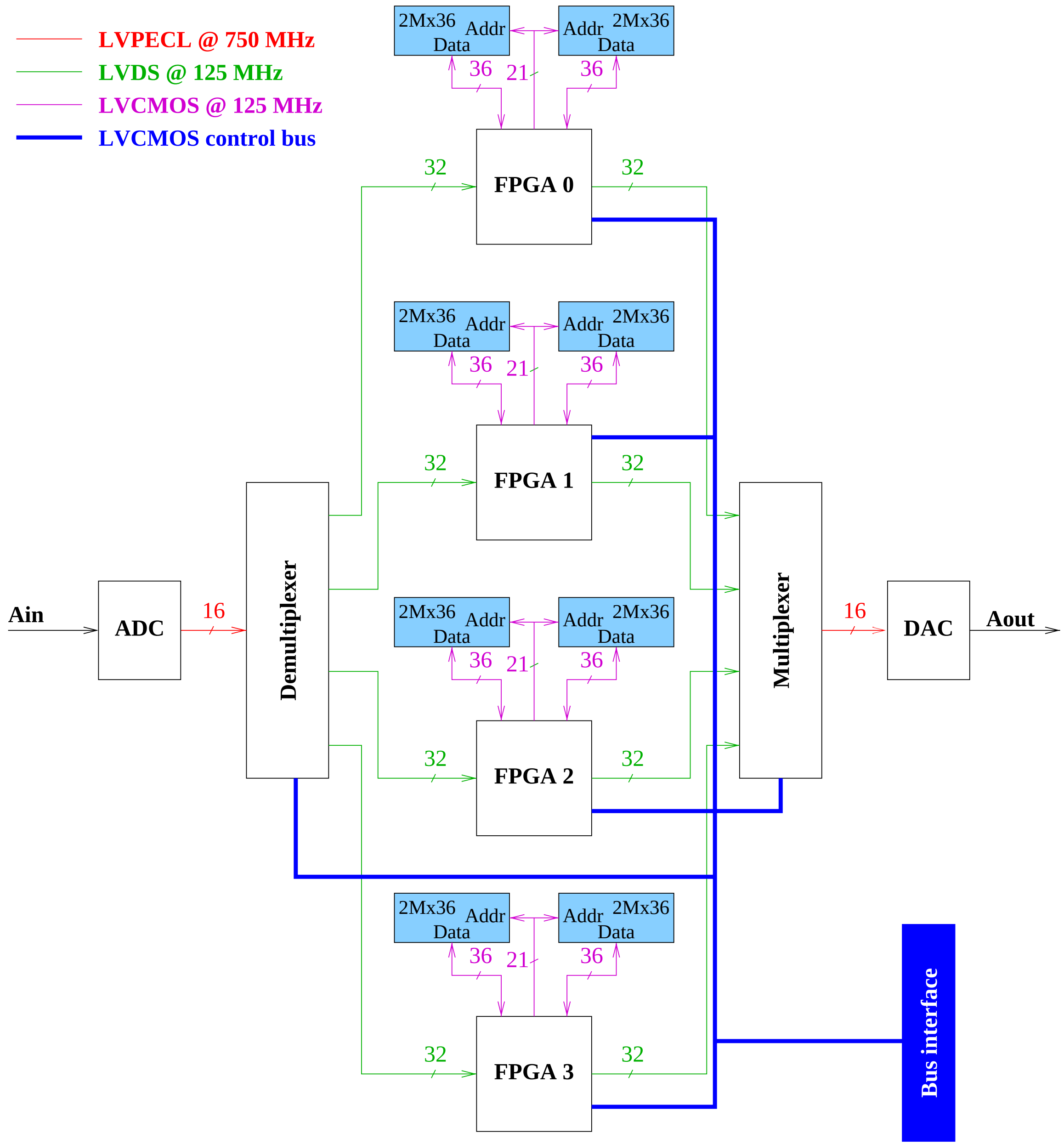
Identify critical technology options, evaluate difficulty of technical implementation

Technical analysis of options

- Bunch-by-bunch dipole control (existing systems, possible enhancements or upgrades)
- Single bunch control (wideband, within bunch Vertical plane)
- Fundamental technology R&D in support of requirements

System Design Proposal and technical implementation/construction project plan

SLAC/KEK/LNF 1.5 GS/sec. Baseband processing architecture



Gboard - joint SLAC/KEK/LNF study

Baseband architecture with 1.5 GHz maximum processing rate implemented as a single VME64X module. Data Flow Processing is implemented in 4 Xilinx Virtex-II FPGA devices.

Each chip handles 4 data samples in parallel. With uneven stepping parallel stream alternates between 16 and 14 samples (94-107 MHz clock rates at 1.5 GSPS).

A 20-tap FIR channel was designed, compiled, placed and simulated for the FPGA implementation.

- 8 bit ADC data, 8 bit DAC output
- 16 bit coefficients
- Full width accumulators (24-29 bits)
- Shift gain of 0-7 bits
- Output saturation to 8 bits
- FPGA resource usage - 52%
- Compiled implementation has 6.3 ns cycle time - for 1.5 GHz we need 9.3 ns.