LHC Power Converter Controls

Radiation Working Group Day 2003

AB-PO-CC Rad Test History

1999	TCC2	WorldFIP components
2000	TCC2	EDAC memory system
2001	TCC2	Analogue Components FGC with 60A converter
2002	TCC2	FGC without converter
2003	Cyclotron TCC2	FGC without peripheral cards FGC without peripheral cards

The Radiation Problem in LHC

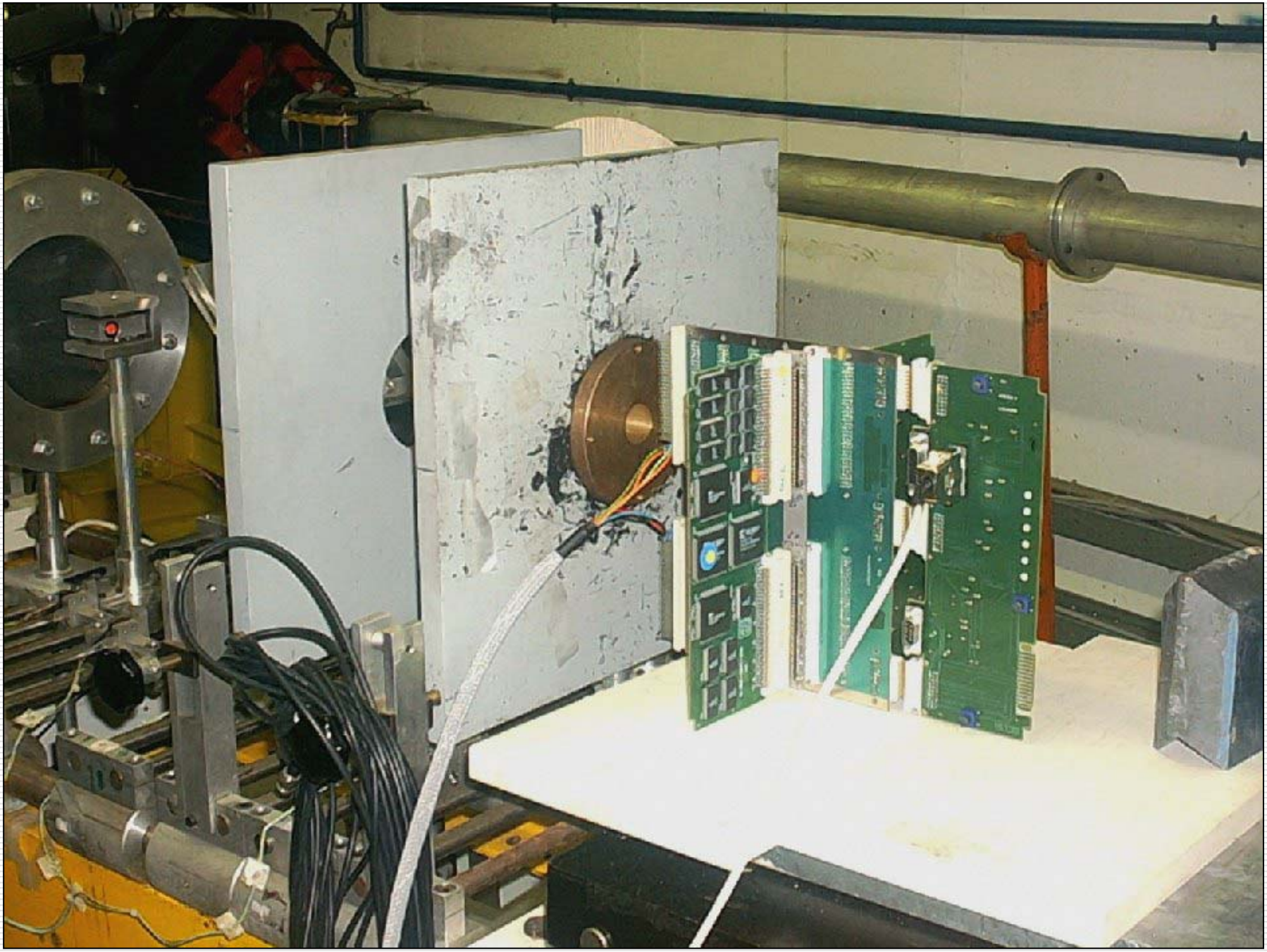
Area	Number of FGCs	Estimated Flux of hadrons > 20MeV	Estimated Dose Rate
Under Arc cryostats	752	$< 10^{10}$ /cm^2/year	2-10 Grays/year
RRs	262	$< 10^{8}$ /cm^2/year	0.1 Grays/year
UAs & SRs	705	~ 0 /cm^2/year	~ 0 Grays/year

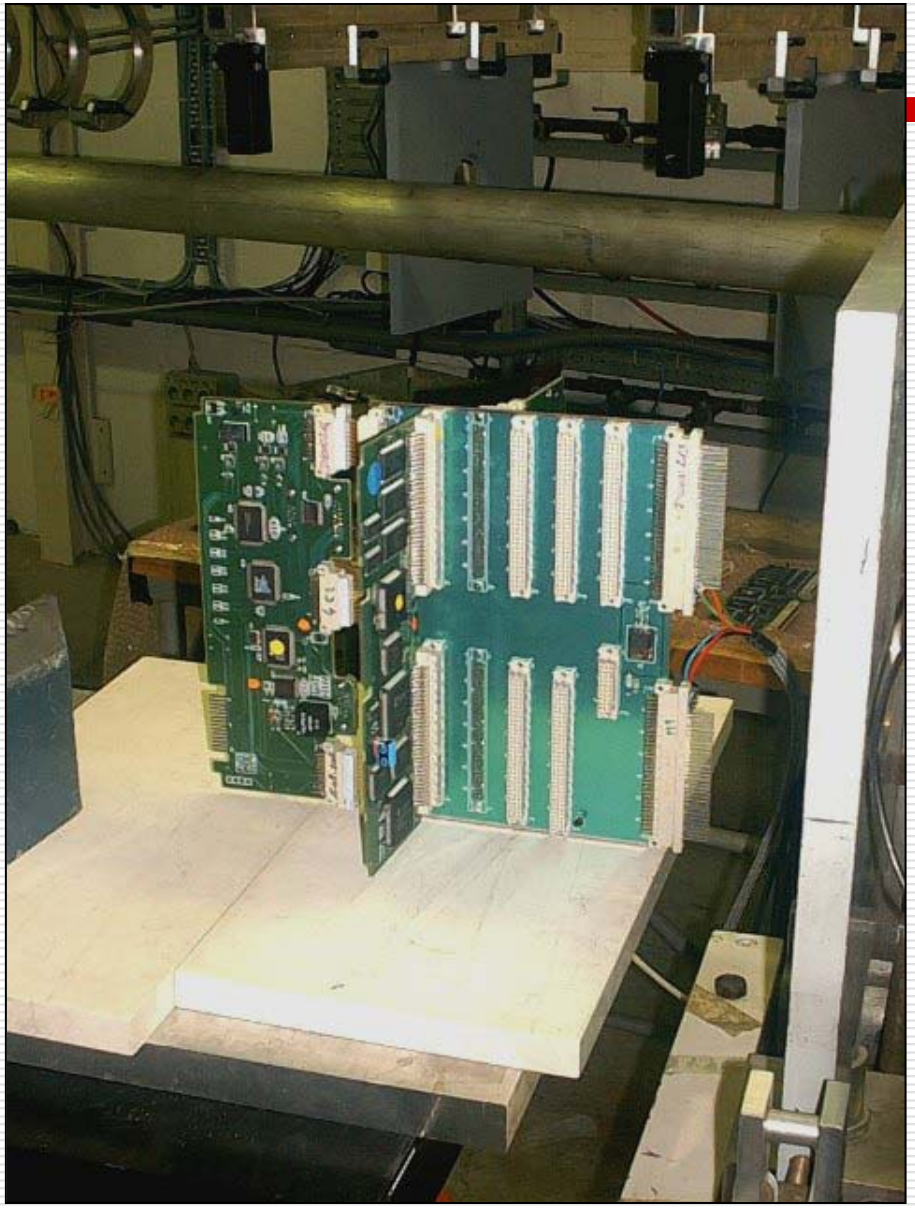
Objectives of Radiation Test at UCL

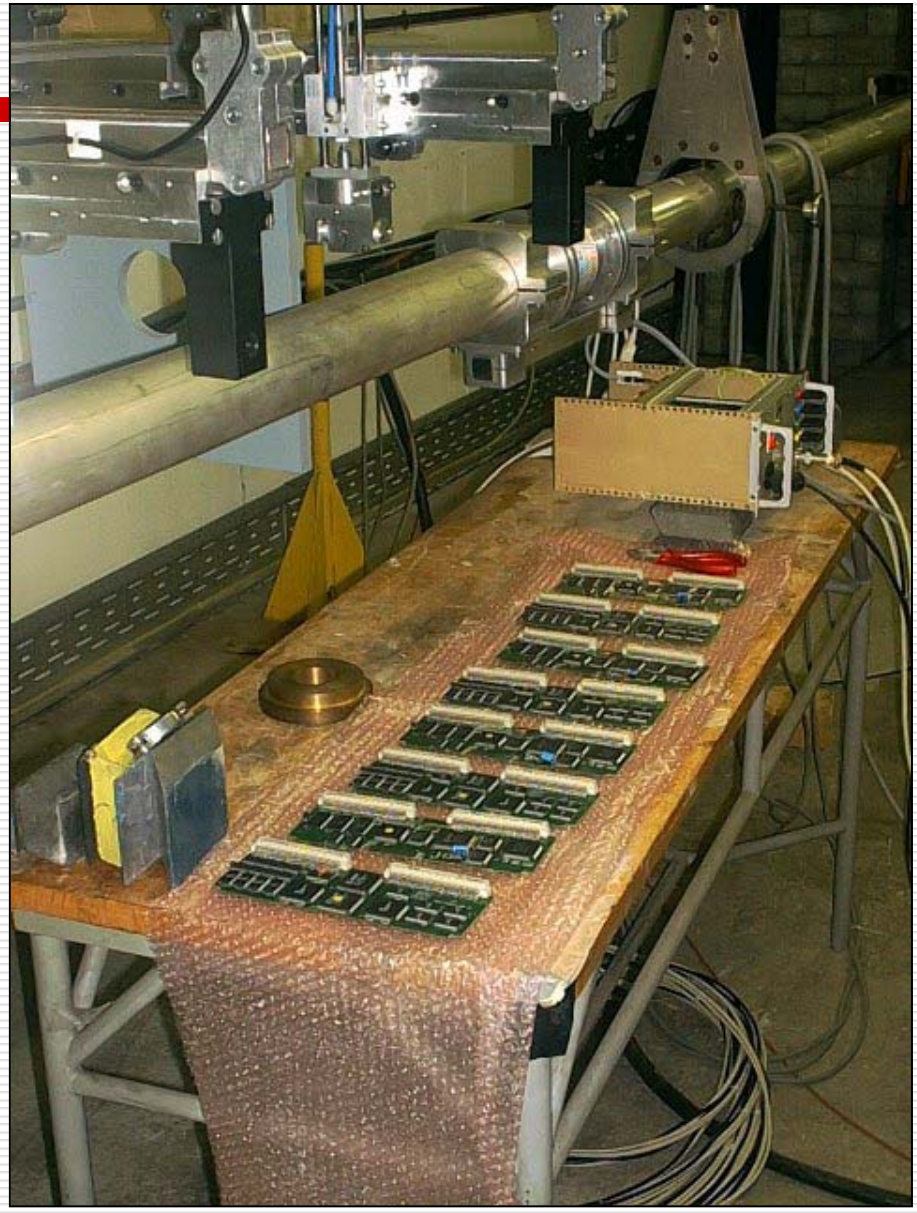
- Calculate the MTBF for the control electronics based the expected radiation levels for LHC
- Use the results to decide if the design is suitable for use in LHC

Test Method

- Critical components identified (all on CPU and Memory boards)
- Five sets of cards taken to UCL with a special backplane
- Each component or group of components was aligned with beam (using a laser)
- Required Flux (particles per cm^2 per second) and Fluence (total particles per cm^2) were requested
- Current consumption and test program reports were recorded on portable PCs during exposure



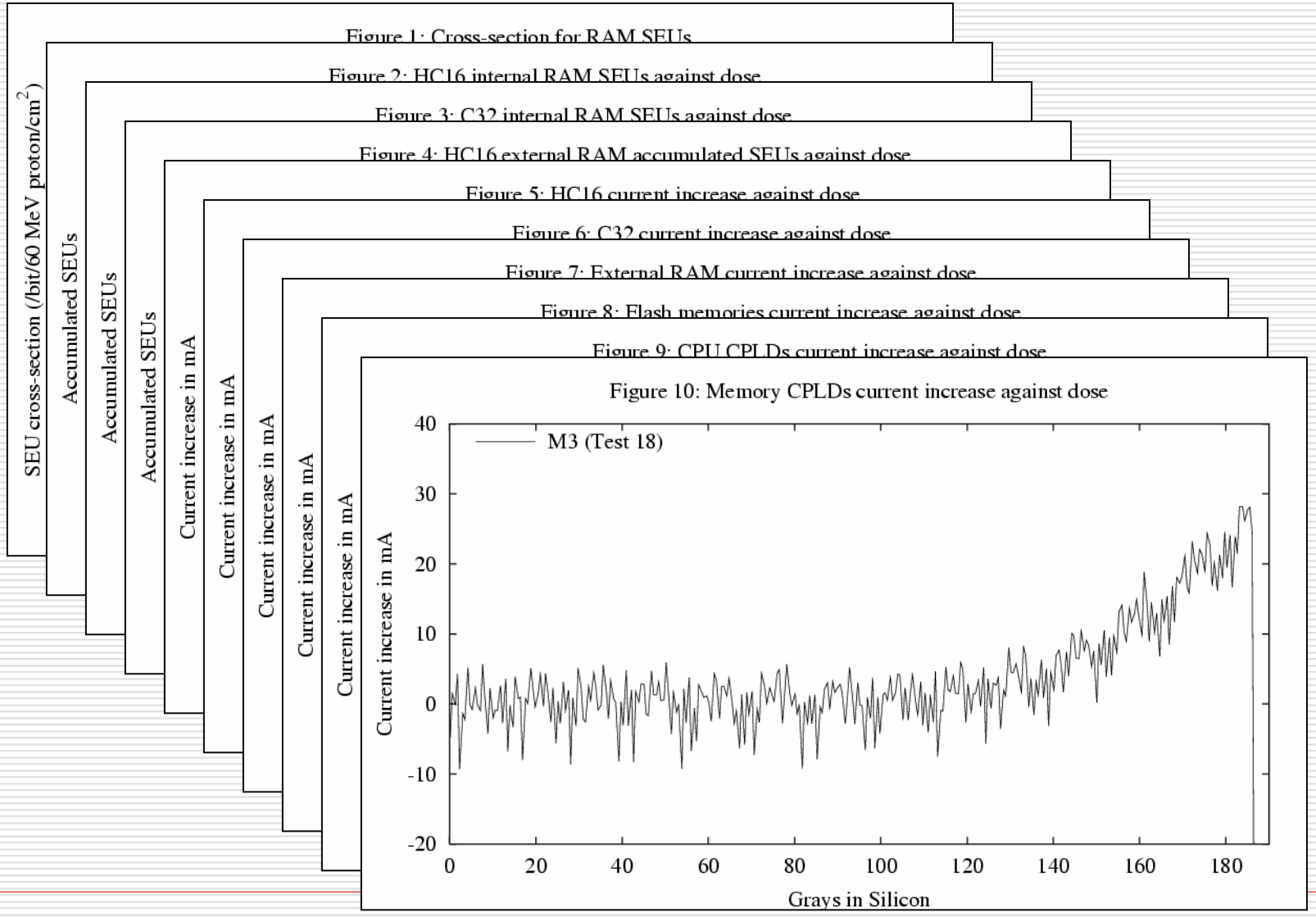




Tests Conducted

Test	Board	Components exposed	Flux	Fluence	State
1	P1	C32	1.00E+08	1.0E+11	Alive
2	P1	HC16	1.00E+08	1.0E+11	Alive
3	M1	HC16 EDAC	1.00E+08	1.0E+11	Alive
4	M1	HC16 memory CPLD	1.00E+08	1.0E+11	Alive
5	P2	CPU CPLDs	3.00E+08	9.0E+10	Dead
6	P3	C32	3.00E+08	2.0E+11	Alive
7	P3	HC16	3.60E+08	1.7E+11	Dead
8	M3	C32 EDAC & RAM	3.00E+08	1.3E+11	Alive
9	M3	HC16 EDAC & RAM & drivers	3.00E+08	2.0E+11	Alive
10	P4	C32	4.60E+08	2.0E+11	Alive
11	P4	HC16	4.50E+08	1.2E+11	Alive
12	P4	CPU CPLDs	4.50E+08	1.8E+11	Dead
13	M4	C32 EDAC & RAM	4.50E+08	2.0E+11	Alive
14	M4	HC16 EDAC & RAM & drivers	4.50E+08	2.7E+11	Dead
15	P1	Flash memories	4.50E+08	3.0E+11	Alive
16	P1	Flash memories	4.50E+08	1.6E+11	Dead
17	M1	Memory CPLDs	4.50E+08	4.0E+10	Dead
18	M3	Memory CPLDs	4.50E+08	1.5E+11	Dead
19	M2	All (edge on)	4.50E+08	1.2E+11	Dead
20	P5	All (shadowed)	4.50E+08	8.1E+10	Alive
21	P5	All (small angle)	4.50E+08	8.8E+10	Alive
22	M5	All (small angle)	4.50E+08	1.0E+11	Alive
23	P5	All (small angle)	4.50E+08	2.0E+10	Dead

Test Results



Results – Total Dose Effects

Component(s)	Current Threshold Grays	Failure level Grays
HC16	100	~240
C32	180	>280
EDAC	>200	>300
RAM	200	>300
Flash Memory	200	>600
Xilinx CPLD	120	~200

Effects of a given dose depend upon the dose rate in a way that is not well understood. Some effects will be less severe whiles others may be worse.

Results – System crashes

- Memory error correction works well – probability of failure due to memory corruption is ~ 0
- Processor register corruptions will cause crashes
  - Estimated MTBF for 750 tunnel based correctors:

    1 – 4 weeks – but some should reset transparently
  - By comparison, MTBF due to other causes is expected to be < 1 week (100,000 hours MTBF for one system means 5.5 days MTBF for 750 systems).

Results – Latch ups

- No latch ups were seen at UCL *except* just before complete component failure
- Probability of latch ups is dependent upon particle energy, so 60 MeV at UCL is NOT representative of LHC
- There may still be a latch up problem, and further tests in TTC2 will investigate the risk

Full Report

- Radiation Tests on the LHC Power Converter Control Electronics, Université Catholique de Louvain-la-Neuve (UCL)
- AB-Note-2003-041
- http://cdsweb.cern.ch/search.py?recid=620638

TCC2 Test (Aug 27-Sept 10)

- We wanted to test two systems for one week each
- No access in the middle so only one system was exposed for two weeks
- It survived for 1.5 weeks
- Preliminary analysis appears to be inline with the Cyclotron data – no time so far for an in depth analysis
- One design change was made based on the results

TCC2 Test – Design change

- The DSP sometimes crashed and could not always be reset by the microcontroller
- This indicates that the DSP is susceptible to latch ups
- A power cycle can be triggered via the WorldFIP even if the microcontroller is dead, but it may require all FGCs on a WorldFIP segment to be power-cycled at the same time
- So the after the change, the microcontroller will be able to initiate a power cycle on request from the control room

Next year…

- We have enough hardware to test up to ten systems in TCC2 in 2004
- This will improve our statistics and should allow more accurate MTBF predictions for LHC

Any Questions?