SL/PO/CC Radiation Tests for 2002

- History – Rad tests from 1999 to 2002
- Scope of 2002 tests and Analysis
- Test 1A – Base controller cards only
- Test 2 – Digital/Analogue I/O included
- Test 1B – System 1 again with I/O
- Summary

History: Rad tests 1999 - 2000

- 1999 – MicroFIP validation
  - ☺ Five standalone MicroFIPs
- 2000 – SRAM EDAC proof of concept
  - ☺ SRAM EDAC test
  - ☺ Flash Memory test
  - 😐 HC16 microcontroller test – Internal registers very occasionally get corrupted which can crash the system.

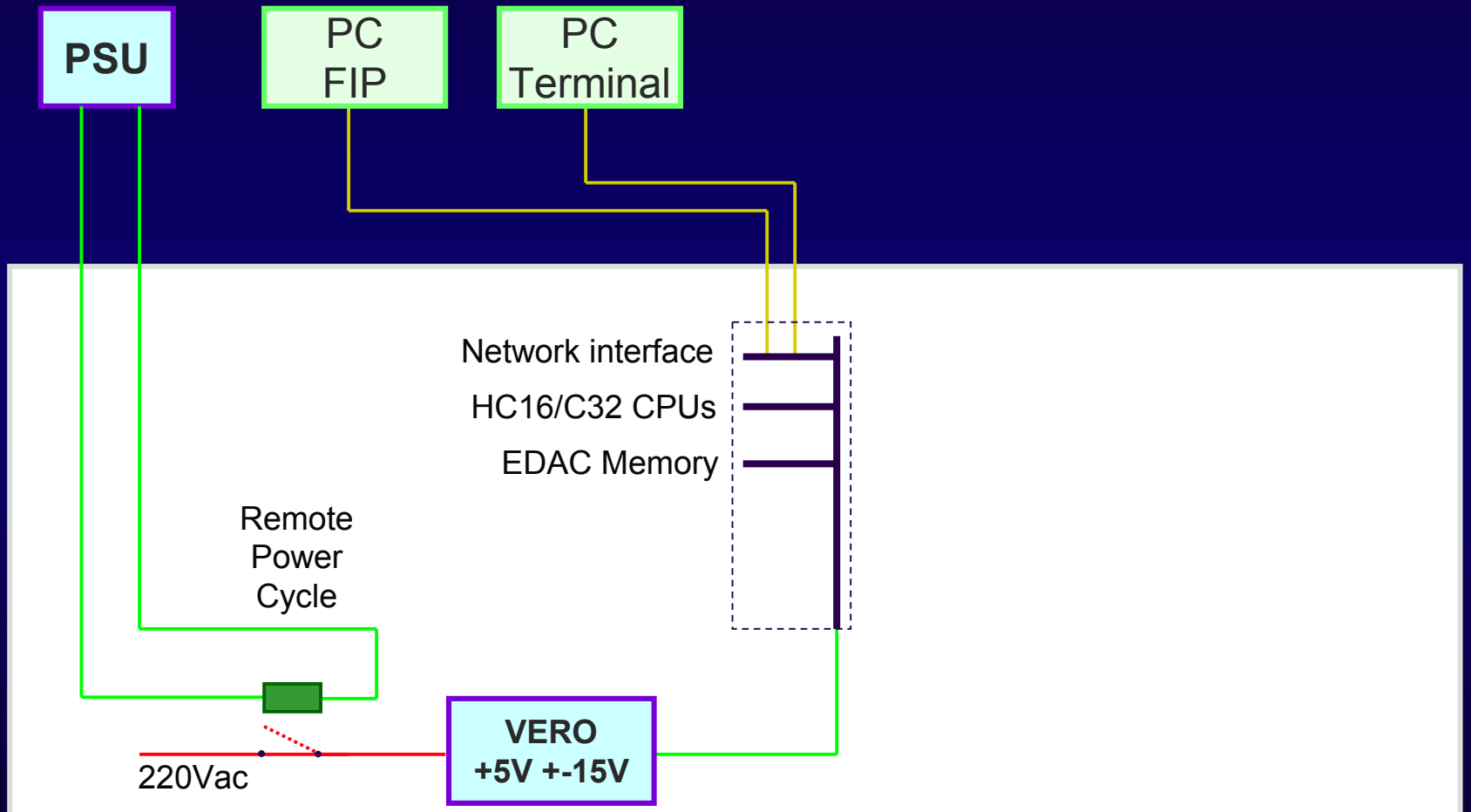
History: Rad tests 2001

- 2001 – HC16/C32, EDAC SRAM, Analogue components & Dallas 1-wire identification bus components
  - ☺ Analogue component tests: Voltage references, ADCs, DAC, MPX
  - ☺ Dallas 1-Wire bus components
  - 😐 Combined HC16/C32 controller test with 60A converter – inconclusive due to thermal problems caused by poor ventilation

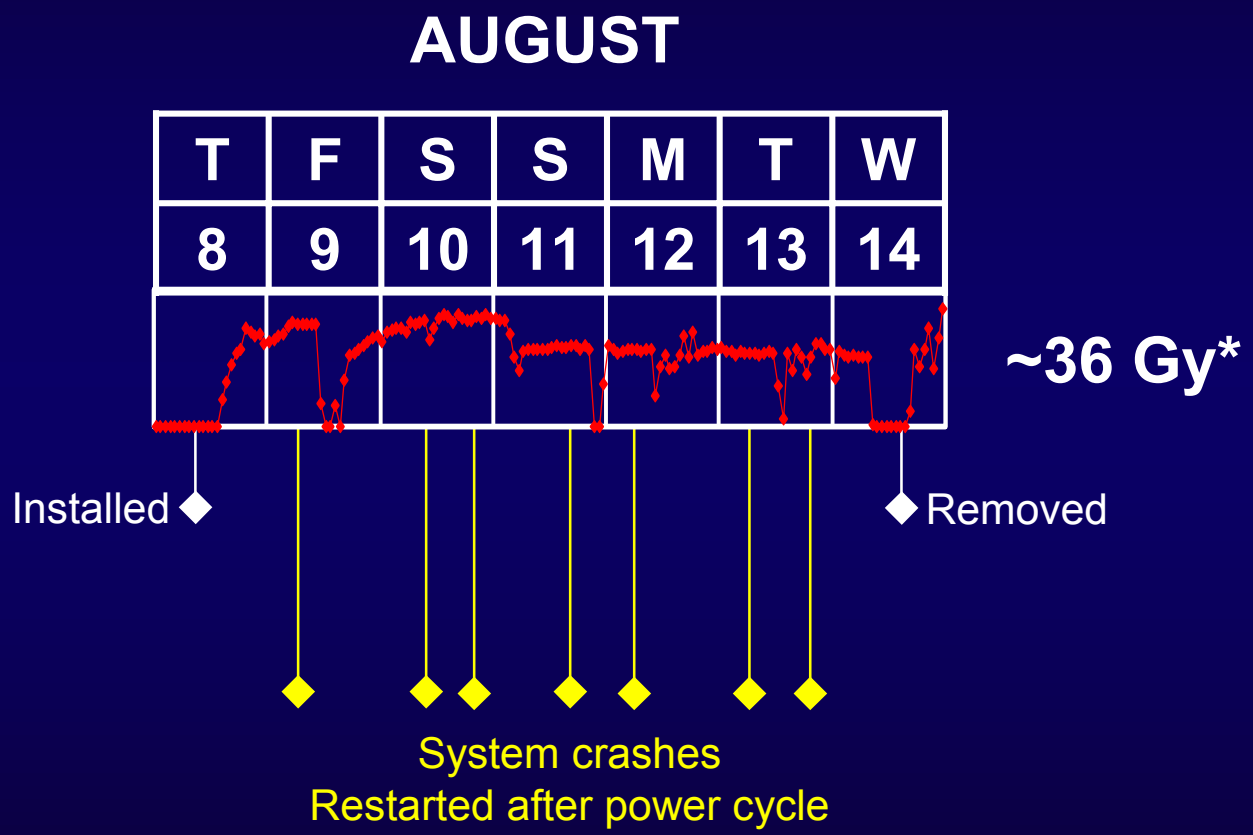
Scope of 2002 Rad tests

- Test of final configuration for processors, memory and Analogue and Digital I/O
- Test of two new components
  - ACT digital driver chip (used on memory board)
  - Mitsubishi C62 microcontroller (manages Dallas 1-Wire Identification bus)
- No test done with a voltage source
  - 60A voltage source validated in 2001
- Simple digital test – outputs looped back to inputs
- Simple analogue test – DAC and on board voltage reference read back via multiplexers using the ADCs.
  - Individual components were validated quantitatively last year.

Test 1A: August 8 - 14



Test 1A : Results

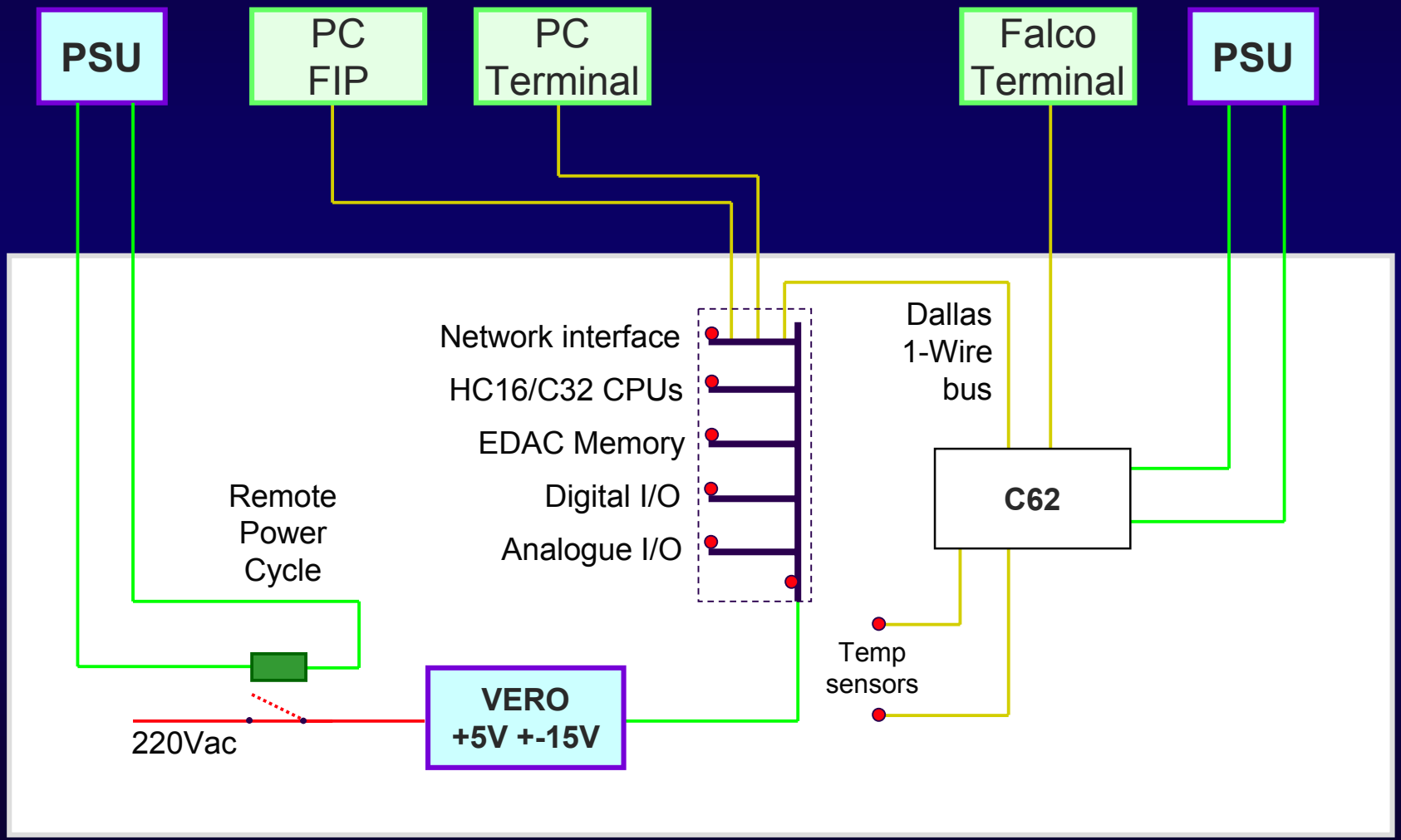


* Average of integrated dose from PMITC07 and PMITC08

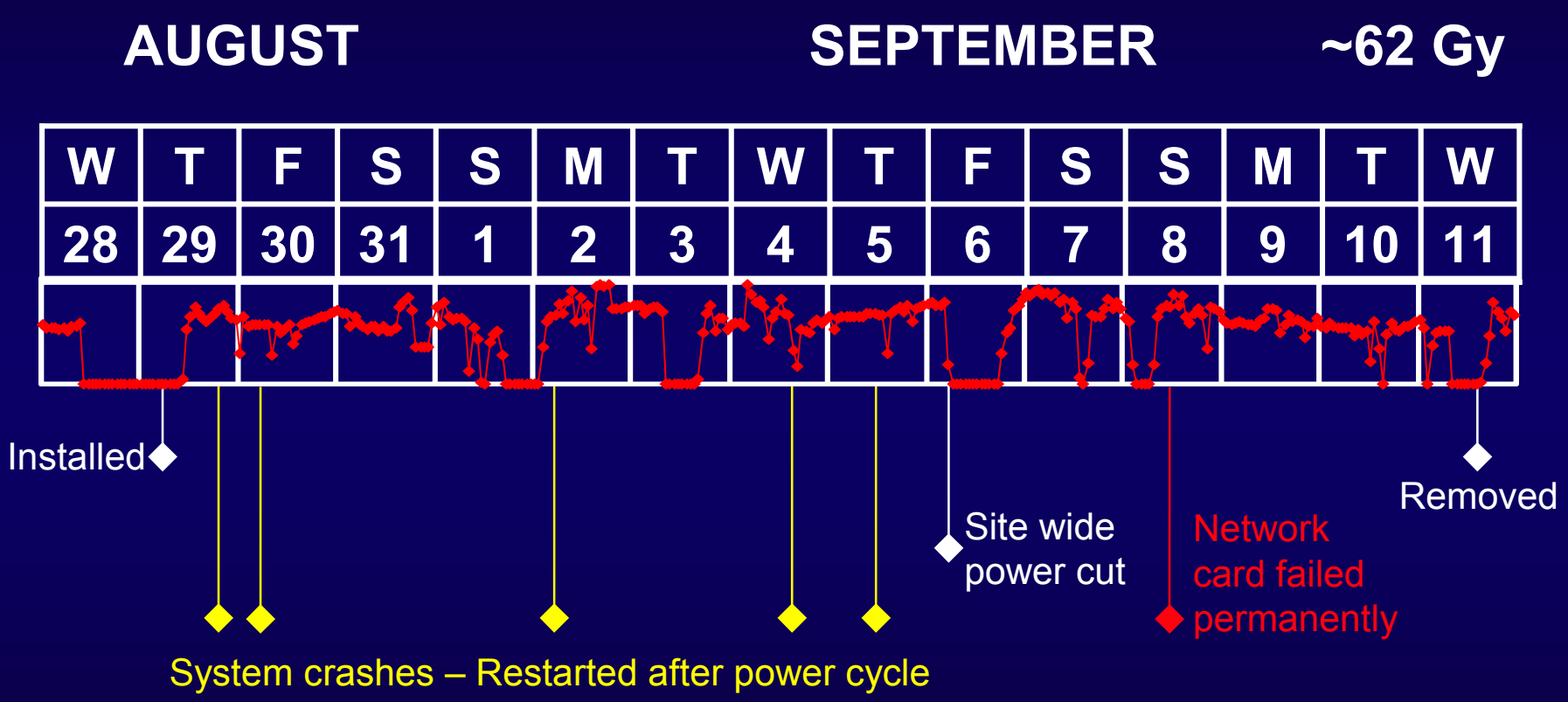
Test 1A : Comments

- Race condition identified in memory logic, so some crashes will have been due to this, and not radiation.
- No component failures during six days of exposure
- ACT drivers used in memory apparently worked well

Test 2: August 28 – September 11



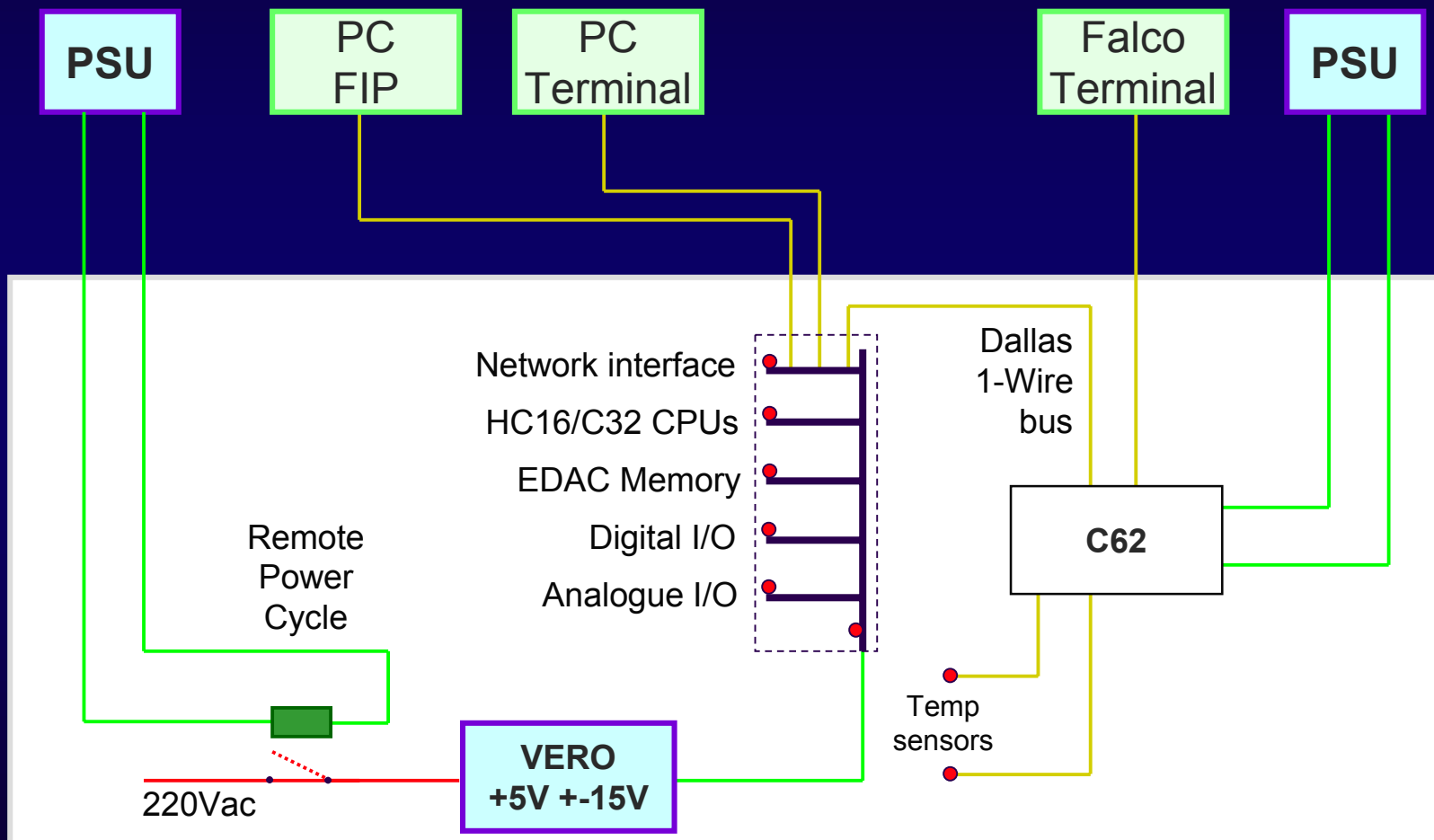
Test 2 : Results



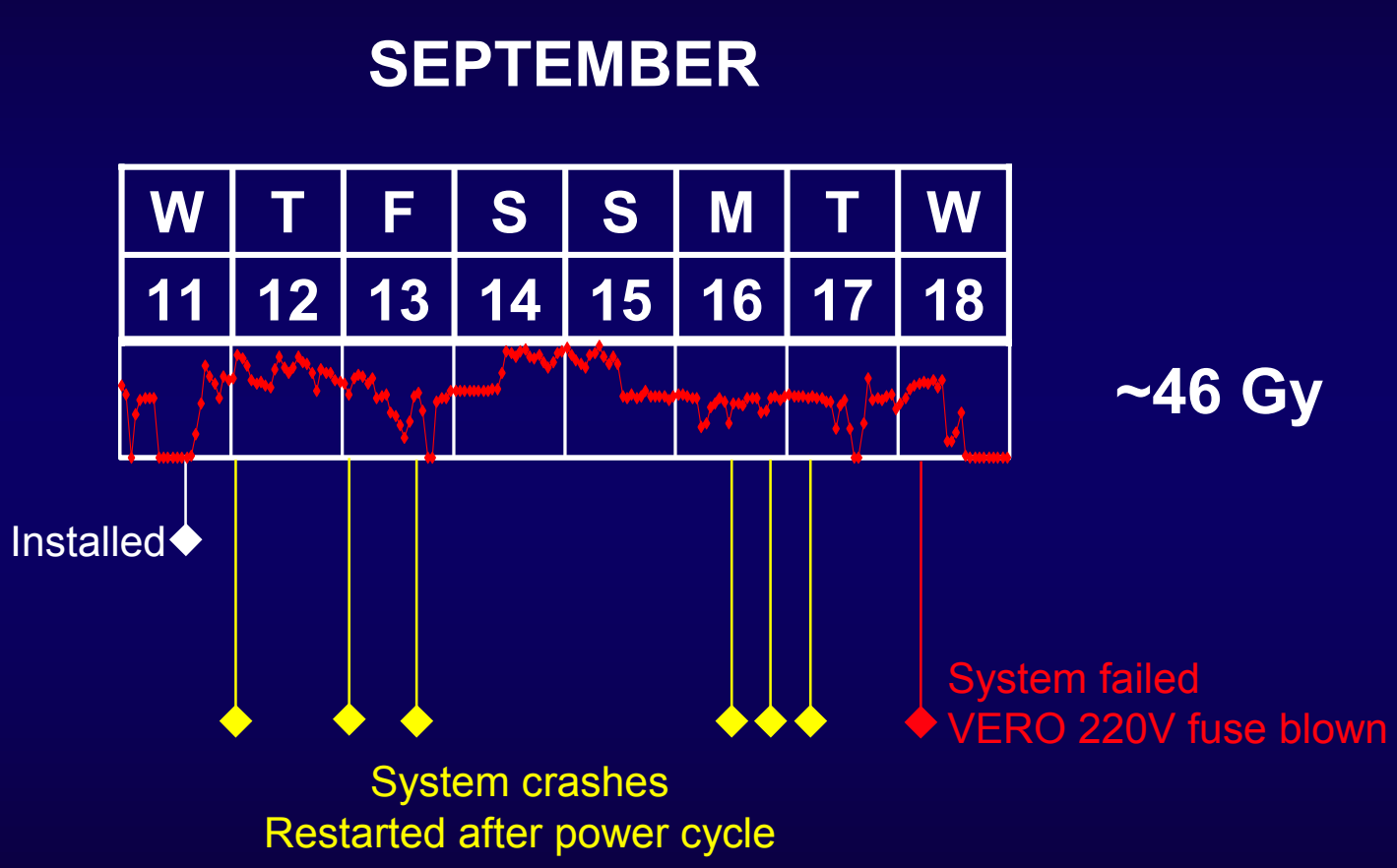
Test 2 : Comments

- Network interface failed after 10 days – reason unknown
- Analogue and Digital I/O components worked well
- C62/Dallas system worked well without permanent failures and with acceptable rate of crashes

Test 1B: September 11 - 18



Test 1B : Results



Test 1B : Comments

- System failed after 7 days (13 days including Test 1A)
- Shortly after communication was lost, the system went cold because the Vero input fuse had blown
- The Vero still works now in the lab, so the failure was transitory but the reason unknown

Summary 1

- 😐 Rad 2002 results for the FGC are somewhat inconclusive
- ☺ EDAC memory works and prevents SEUs in the SRAM from crashing the system
- ☹ Small number of registers exist in the HC16, C32 and uFIP which cannot be protected
- ☺ Mitsubishi C62 and Dallas components survived
  - non-destructive latch-up of the C62/Dallas seen so they will be powered only on request by the HC16
  - C62 will probably run for 20 seconds every five minutes (to read system temperatures)

Summary 2

- ☺ Even pessimistic dose estimate (20 Gray per week) suggests that the system will survive an LHC lifetime.
- ☹ Two permanent failures, but impossible to say if radiation was the reason
- ☹ Mix of particles makes it hard to draw conclusions

- Too late and no budget to change design – we are confident it will work for some time and will enable LHC to start up
- Further tests in 2003 are recommended using PSI source to estimate time to failure in LHC