RADWG DAY
Power Converters
Control Part

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Rad. Test Team SL/PO/CC

- **DIGITAL parts and programs**
  - Ch. Martin , Ph. Semanaz, P. Martinod & T. Valzer
- **FALL BACK system & programs**
  - Q. King & P. A. Masson (cooperant)
- **Tunnel NETWORKING & programs**
  - I. Barnett & T. Valzer
- **TRACABILITY system & programs**
  - A. Dinius , N. David & P. Martinod
- **ANALOG ACQUISITION & analysis programs**
  - T. Valzer
- **ANALOG parts**
  - J. Pett & G. Ramseier (Rad.Test Coordinator)

Outline

- Introduction
- Previous test periods
- Test program 2001
- Digital components
- Analog components
- Design strategy
- Combined tests
- Overall conclusions
- Tests for 2002

Introduction

- 750 Dipole corrector power converters in the LHC tunnel (mid-arc under the cryostat)
- Both control (DICO) and power part must be radiation tolerant to about 20 Gy. with acceptable reliability
- For the control part a single design using COTS components will be used for all LHC power converters
- Rad tests have been on-going for 3 years

Previous test periods

- 1999 - tests of stand-alone WorldFIP
  - OK to >300 Gy. This provided the basic communication mechanism to facilitate future testing
- 2000 - tests of microcontroller HC16 + EDAC memory via uFIP (stand-alone)
  - OK all memory SEUs 'repaired' but some other areas affected

Test program 2001

- Verification of EDAC protected DICO
- Tests of a fall-back control interface
- Tests of auxiliary digital components
- Test of critical analog components
- Combined tests with power parts

Digital components

- **DICO - HC16 + 320C32 (DSP) + memories + uFIP in micro-controlled mode**
  - **SRAM (256 kBytes), fully protected by EDAC system**
  - **FLASH (256 kBytes), no errors, no protection**
  - **HC16 Internal RAM, errors seen, can not be protected**
    - not used
  - **HC16 Internal Registers, can not be seen, can not be protected**
    - vital for system integrity, watchdog restart..
  - **320C32 DSP**
- OK up to 100 Gy.

Digital components

- **Double uFIP** [Fall back solution]
  - **As expected, no problems for fast R/W operations**
- OK up to >>100 Gy.
- **DALLAS / MAXIM** [Card identification system]
  - **DS2430A (256 bits 1 wire EEPROM)**
  - **DS18B20 (1 wire digital thermometer)**
- OK up to >>100 Gy.
- **WorldFIP repeater** (RP131 IR178-2CC1)
  - **Industrial product, DC-DC converter removed**
- broken after 20 Gy. Needs redesign & retest! URGENT!

Analog components

- ADC
  - **For latch-ups, restart after cutting the power supply and re-powering the component**
  - **ADS7852BB (12 bits / 4 inputs)**
    - For QSPI monitoring / diagnostic
    - Rapid test : OK up to 40 Gy.
  - **ADS7807UB (16 bits SAR)**
    - RAD drift @10V is ~ +10 uV/Gy. (see Vref)
    - OK up to 80 Gy. (1 latch-up)
  - **LTC1605ACN (16 bits SAR)**
    - RAD drift @10 V is ~ -15 uV/Gy. (see Vref)
    - OK up to 80 Gy. (1 latch-up)

Analog components

- DAC
  - **drift is inside the loop (ADC is used as reference)**
  - **AD1862N (20 bits audio)**
    - RAD drift @ 10 V is ~ -45 uV/Gy.
    - OK up to 80 Gy.
  - **MAX542ACPD (16 bits)**
    - Some bits are affected, thus the linearity is not acceptable : component rejected.
    - RAD drift @ 10 V is ~ -70 uV/Gy. (see Vref)
  - **AD5542AR (16 bits)**
    - RAD drift is ~ -100 uV/Gy. (see Vref), (1 latch-up)

Analog components

- **V reference**
  - **TCC2 tunnel temp. stability : ~2 deg.C/month**
  - **MAX6325CSA (2,5 V, max. 1ppm/deg.C)**
    - RAD drift @ 2,5 V is ~ -20 uV/Gy.
    - OK up to 80 Gy.
  - **MAX6350CPA (5,0 V,max. 1ppm/deg.C)**
    - RAD drift @ 10 V is ~ -120uV/Gy.
    - OK up to 10 Gy. (tests not continued)
  - **LT1236ACS8-10 (10 V typ. 2ppm/deg.C)**
    - used as 10 V ref. for calibration purposes
    - RAD drift @ 10 V is ~ -40 uV/Gy.
    - OK up to 80 Gy.

Analog components

- Multiplexer
  - MAX337CWI (Dual 8 inputs)
- Regulator
  - LM317LZ (used as 5V reg for ADCs & DACs)
- Resistor network (TaN)
  - DP1603-1002A (ratio stability vital, used for signal conditioning)
- Operational amplifier
  - OPA2227PA
- All the above are OK up to 80 Gy.

Design strategy

- **RAD Tolerant**
  - **Not all errors can be detected / repaired**
    - Minimize by design choices
  - **Digital (critical) registers**
    - rewrite, triple-up: - physically and in software
  - **Latch-ups**
    - Power down, selective restart
  - **Analog redundancies**
    - Hi-reliability PSU, two ADC, swap-over(s)
  - **Selective restarts, fast reboot, hold DAC value**
  - **More frequent calibrations due to drift**

Complete test

(Converter & DICO)

- 1st try - DICO operated up to 9 Gy.
- 2nd try - DICO operated up to 40 Gy.
- Failure reasons
  - FPGA (DICO) destruction, due to excessive temperature inside power converter case
  - Some material already irradiated (converter)
  - DCCT broken ..open loop operation
- Other results in the next presentation

Overall Conclusions

- No major problems for all sensitive parts up to 20 Gy.
- MTBF will not be substantially affected by operating in the tunnel - mid arc
- Over the converter lifetime, a few (<1/year) automatic restarts of the DICO must be expected due to radiation effects and should have minimal impact on operation

Tests for 2002

- Final pre-production DICO version to be assembled and a series of five complete power converters must be fully tested for overall performance and radiation tolerance
- This will enable better statistics for in-service ‘restarts’ to be estimated
- More ‘real-time’ monitoring of the radiation level at the exact test location would be most useful