Progress on p-type isolation technology

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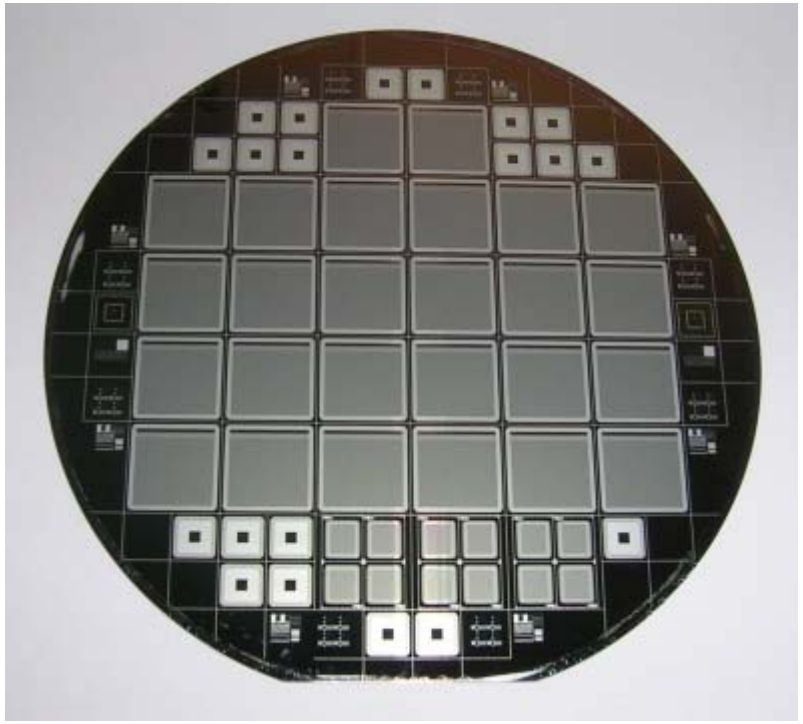
The story so far...

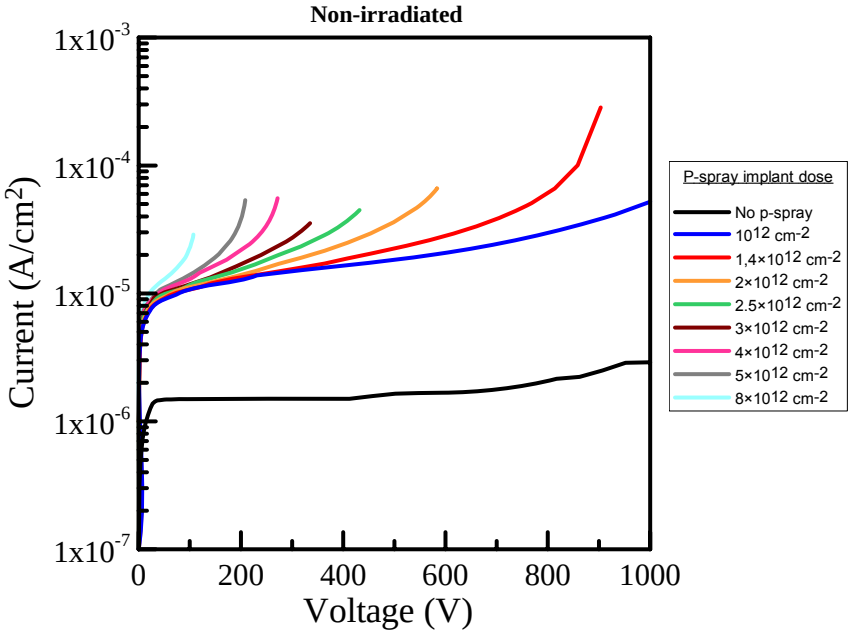


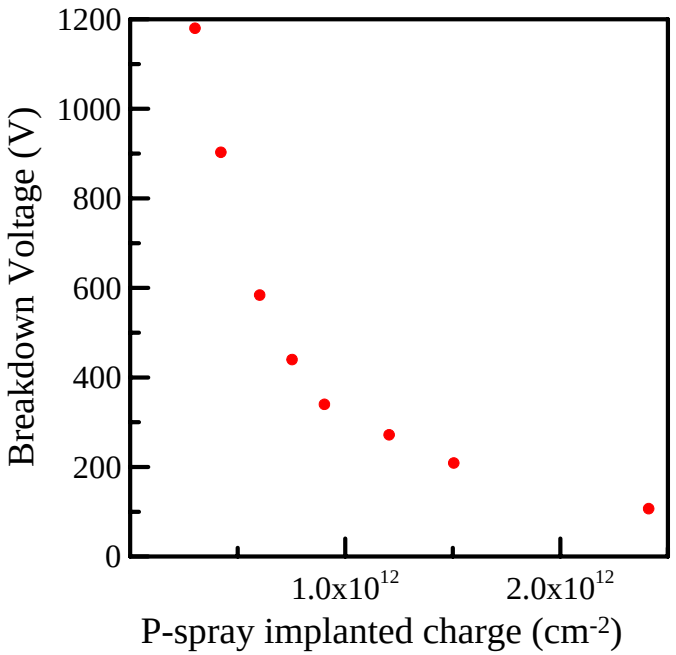
- IMB-CNM is developing different detector technologies
- We are to process wafers for the Collaboration
- P-in-N and N-in-P
- Mask set designed by RD50
- Surface insulation provided only by p-spray (no layer for p-stops)

- Optimize the p-spray parameters before processing the RD50 wafers
  - Complete simulation process (ISE-TCAD)
  - Test runs to check simulation results and adjust p-spray implant parameters (dose, energy, SiO_2 layer thickness)

Simulation results

- V_{BD} decreases and leakage current increases as the p-spray implanted charge increases
- Need high p-spray doses to avoid inversion in the silicon surface in irradiated devices
- Compromise solution between reasonable V_{BD} and good strip insulation. Can be critical in devices fabricated on Cz silicon
- See presentation at the 6th RD50 workshop for details





Test runs 1 and 2

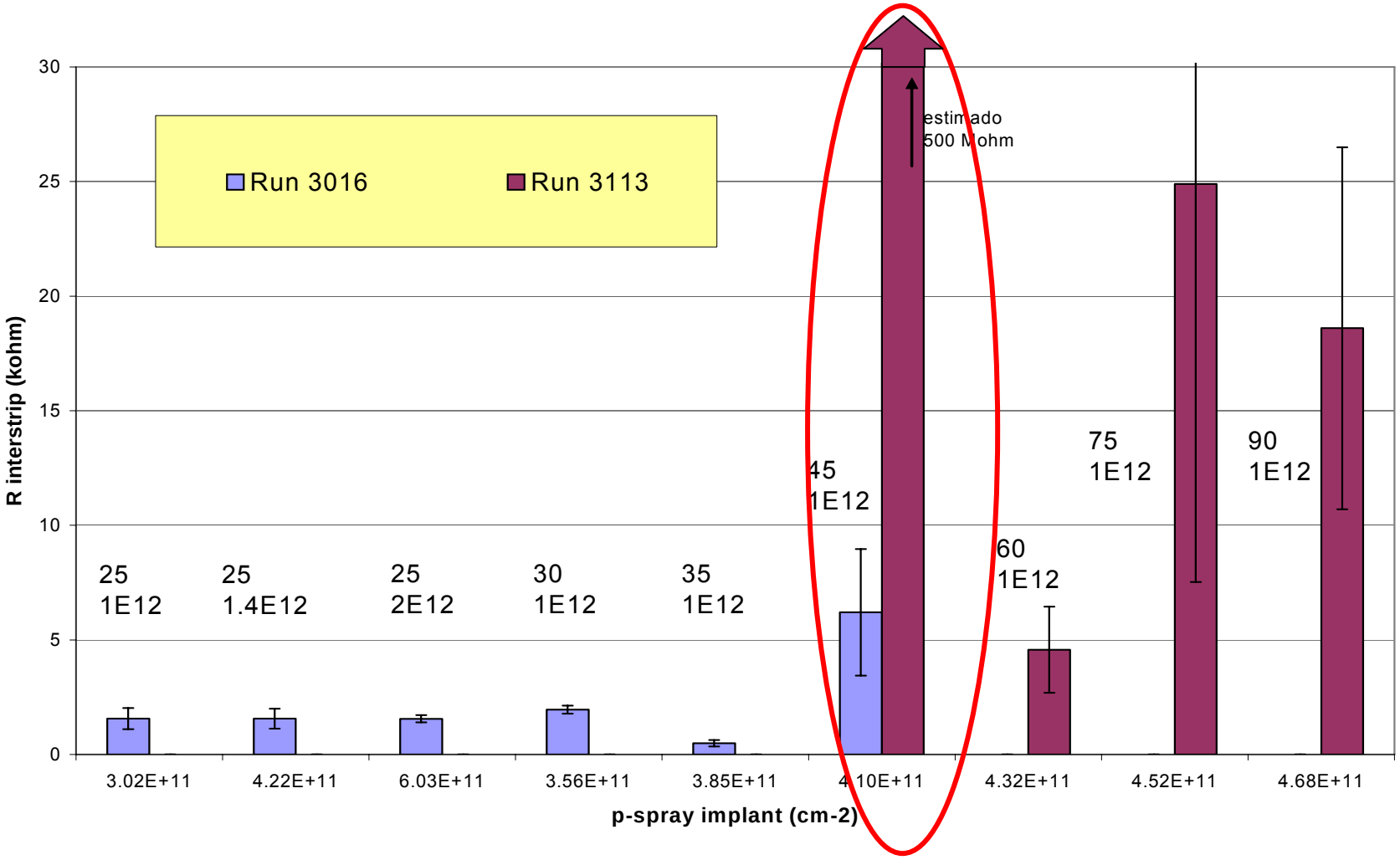
- New wafers from Siltronix
- <100>, p-type, 300 ± 15 mm
- ρ (nominal)= 30 kΩ·cm, ρ (measured)= 20 kΩ·cm
- Low p-spray implant doses, but all guarantee strip isolation, according to the simulations

	Run 1		Run 2	
Wafer	**E (keV)**	**Dose (cm^{-2})**	**E (keV)**	**Dose (cm^{-2})**
1	**25**	**10^{12}**	**45**	**10^{12}**
2	**25**	**1.4×10^{12}**	**60**	**10^{12}**
3	**25**	**2×10^{12}**	**75**	**10^{12}**
4	**30**	**10^{12}**	**90**	**10^{12}**
5	**35**	**10^{12}**		
6	**45**	**10^{12}**		

Test runs 1 and 2: results

- Bad results:
  - all devices in most wafers shorted
  - No correlation between results and process parameters
  - No agreement with expected values from simulation
  - Only two wafers with working detectors
- Siltronix wafers
  - Bad visual aspect of wafers
  - After investigating we discovered crystallographic defects
  - Wafers replaced by the company
- We believe bad results were due to the quality of the wafers

Run 1 and 2 inter-strip resistance



~250 MΩ for n-in-p with P-stops → still some hope

Test run 3

- We decided to repeat the only good wafer from run 2
- Six wafers processed with identical parameters to study the repeatability of the technology
- 3 Siltronix wafers from a different batch than previous two runs
- 3 Topsil wafers

- 2 more Siltronix wafers with corner parameters

Test run 3

Wafer	Vendor	Type	ρ (kΩ·cm)	p-spray E (keV)	p-spray dose (cm^{-2})
1	Topsil	DOFZ	1-5	45	10^{12}
2	Topsil	DOFZ	1-5	45	10^{12}
3	Topsil	DOFZ	1-5	45	10^{12}
4	Siltronix	FZ	30	45	10^{12}
5	Siltronix	FZ	30	45	10^{12}
6	Siltronix	FZ	30	45	10^{12}
7	Siltronix	FZ	30	45	5×10^{12}
8	Siltronix	FZ	30	150	10^{12}

- **Initial results from characterization: ALL wafers OK!!**

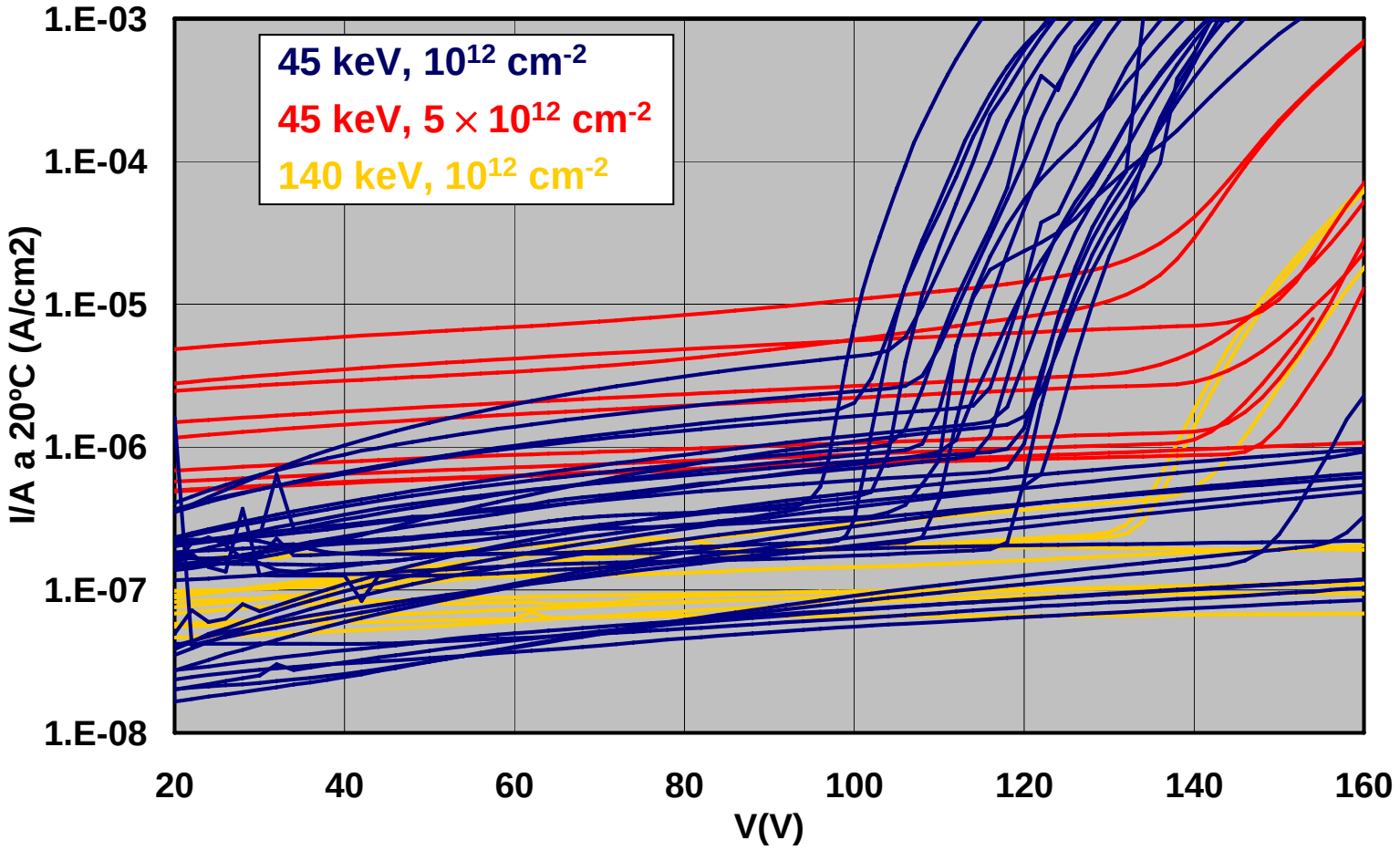
Pad detectors: Breakdown voltage

	V_{BD} (V)	
p-spray	**simulated**	**measured**
45 keV 10^{12} cm^{-2}	900	> 700 V
150 kev 10^{12} cm^{-2}	710	~ 700 V
45 kev 5×10^{12} cm^{-2}	210	~ 250 V

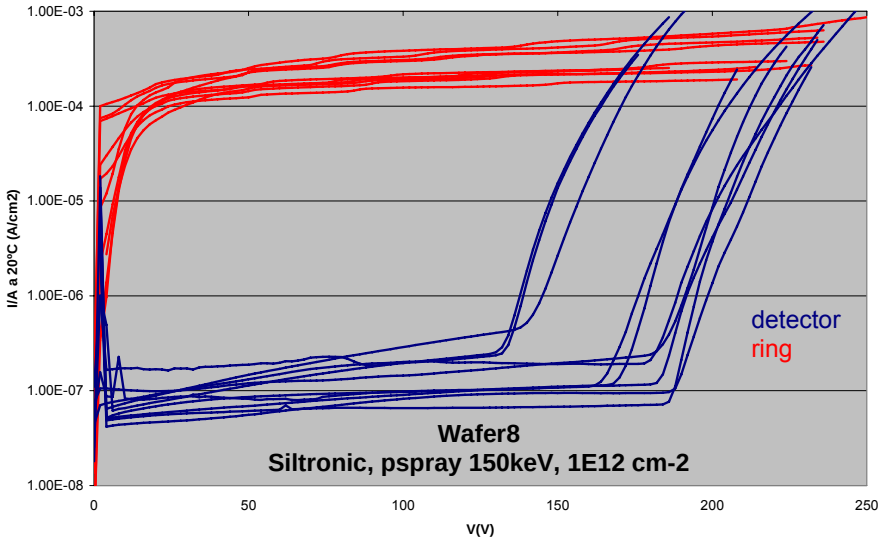
6 wafers

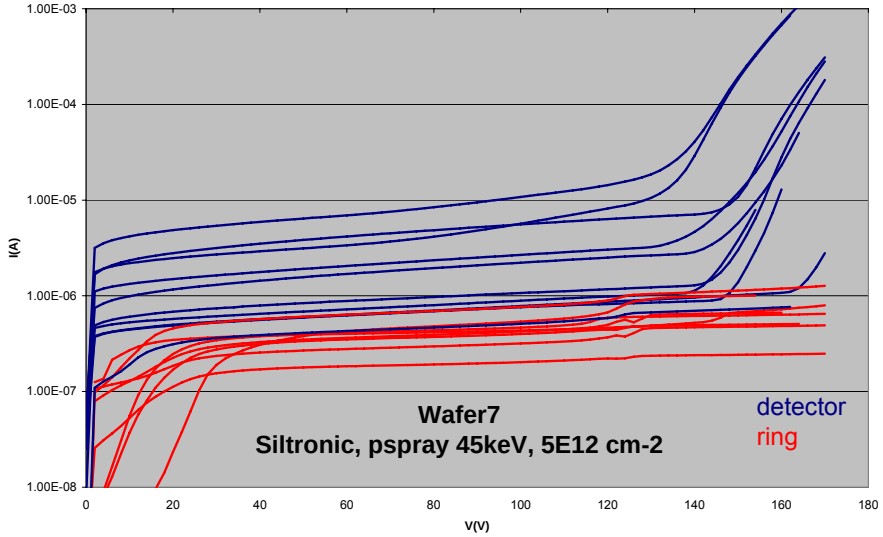
Microstrip detectors: Breakdown voltage

- V_{BD} between 100 and 200 V <u>for all wafers</u>



Microstrip detectors: Leakage current





- Microstrips with a p-spray dose of 10^{12} cm^{-2} are not fully isolated
- Large leakage currents in guard ring
- Should improve with wafer cutting

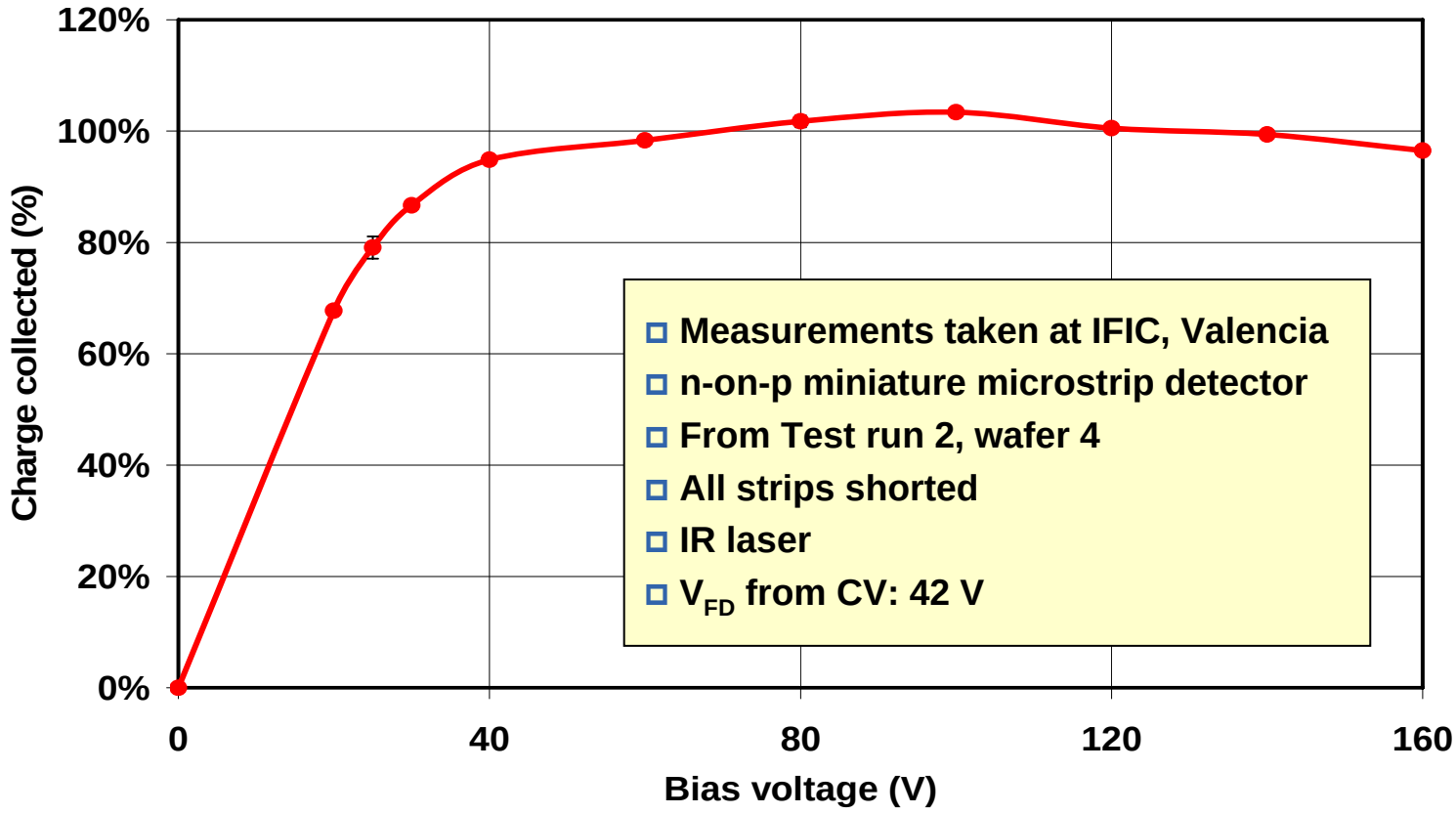
Microstrip detectors: Leakage current

	Manufacturer	I(diode)	I(ring)
45 keV 10^{12} cm^{-2}	Siltronix (3 wafers) Topsil (3 wafers)	70 ± 40 nA 500 ± 200 nA	2.8 ± 0.8 mA 1.3 ± 0.2 mA
150 kev 10^{12} cm^{-2}	Siltronix (1 wafer)	120 ± 50 nA	200 ± 50 µA
45 kev 5×10^{12} cm^{-2}	Siltronix (1 wafer)	2 ± 1 µA	400 ± 30 nA

- Measured at VFD + 20V (62 & 86 V), corrected at 20ºC
- Detector area ~ 1 cm^2

Charge Collection Efficiency results

- IFIC setup finished and operative with IR laser
- CNM setup in progress, finished by next month



Conclusions

- Good results
- Working devices
- Simulation agreement for pad detectors
- Strip detector breakdown voltage not much dependent on p-spray dose, limited by geometry
- We are ready to start RD50 process
  - We have to check epitaxial backside rim incompatibilities

- We propose to increase both energy and dose, i.e.:
  - Energy: 100 - 120 keV
  - Dose: 2 - 3 $\times$ 10^{12} cm^{-2}

Reminder of RD50 process

Technology	Wafers	Growing method	Type	Wafer origin	Comments
P-in-N	4	MCZ	N	RD50	>500 Ω·cm, 300 µm
	2	EPI	N	RD50	thickness ~ 150 µm
N-in-P	4	MCZ	P	RD50	>2 kΩ·cm, 300 µm
	4	FZ	P	CNM	
	4	FZ	P	CNM	Oxygen enriched DOFZ
	2	EPI	P	RD50	thickness ~ 150 µm
N-in-N	2	FZ	N	CNM	Single side processing
TOTAL	22				