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(On-line) Data Processing for the EU-DET, MAPS based Beam Telescope Demonstrator

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Outline

- The goal for the DAQ in 2006 (my personal point of view)
- Minimum data processing during acquisition
- DAQ example based on existing acquisition cards
- Conclusions

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DAQ Requirements for the Beam Telescope Demonstrator: to be discussed and agreed on

Some proposition

- Continuous data taking: no dead time
- Real-time (in-flight) zero suppression
- Acquisition cards: ADC + FPGA + two-frames data memory + buffer (hit) memory
- Common interface for the PC
- Sensitive area selection based on internal data?
- On-line track reconstruction?

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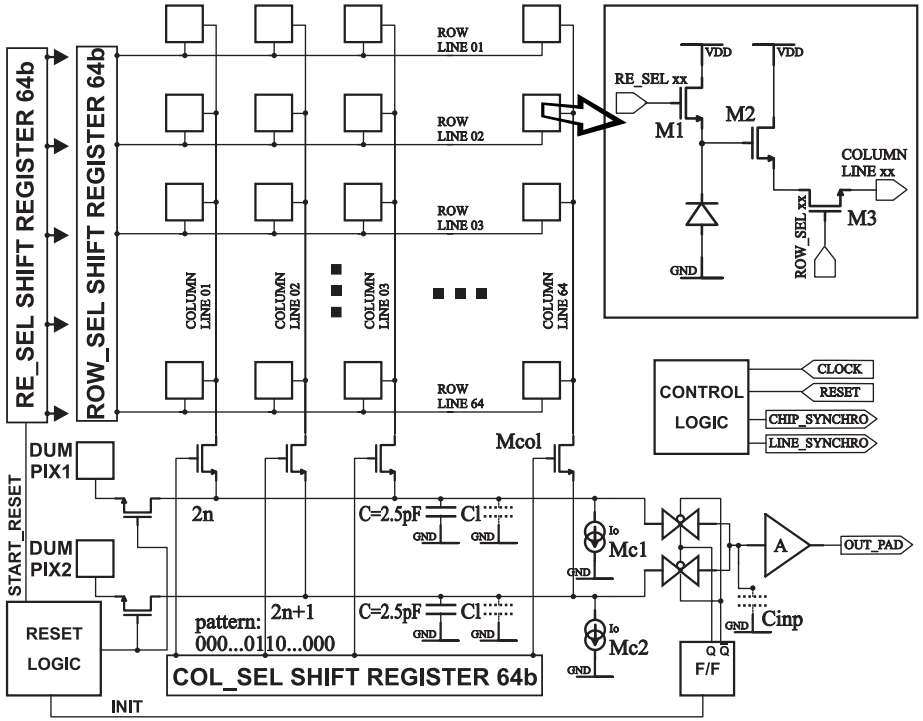
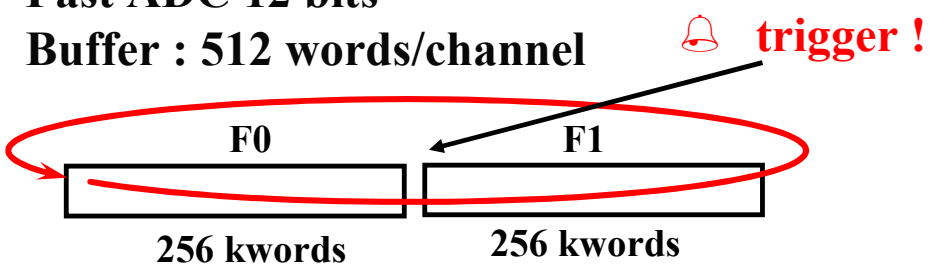
The simplest readout electronics (Mimosa5): diode + 3 transistors/pixel



1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time)), simple data processing in order to recognise hits

Fast ADC 12 bits

Buffer : 512 words/channel



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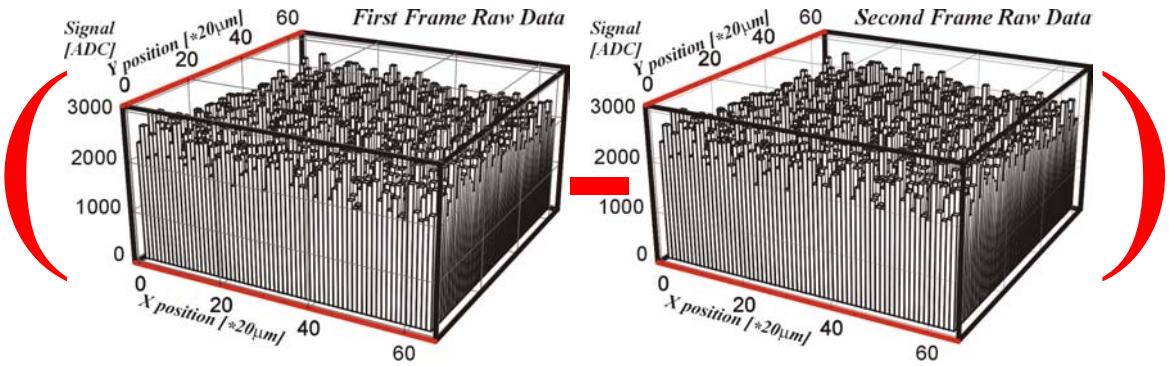
Data processing: (Digital) Correlated Double Sampling (CDS)



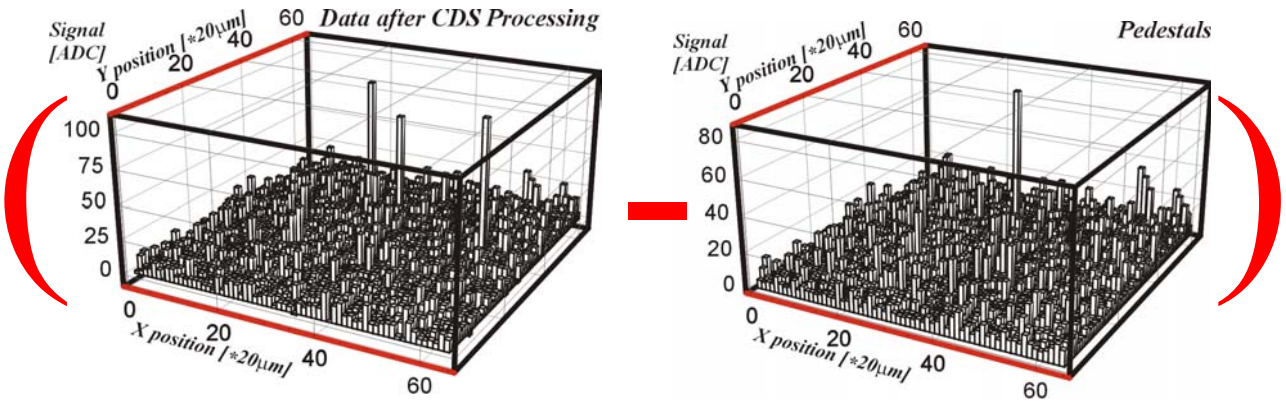
frame 1) frame2)

(frame2 - frame1) subtraction

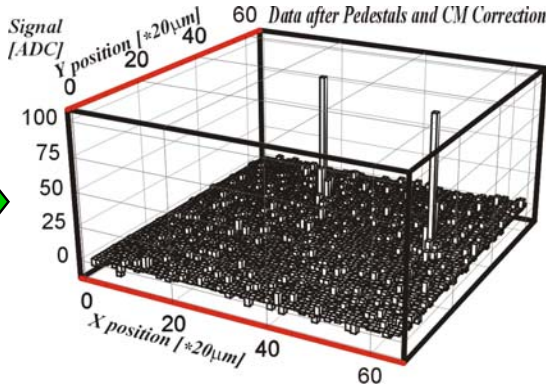
Useful signal on top of Fixed Pattern DC level

Fixed Pattern dispersion: ~100 mV

Typical signal amplitude: ~1mV



frame2 – frame1) **Pedestal (dark current) subtraction**



Hit candidates!

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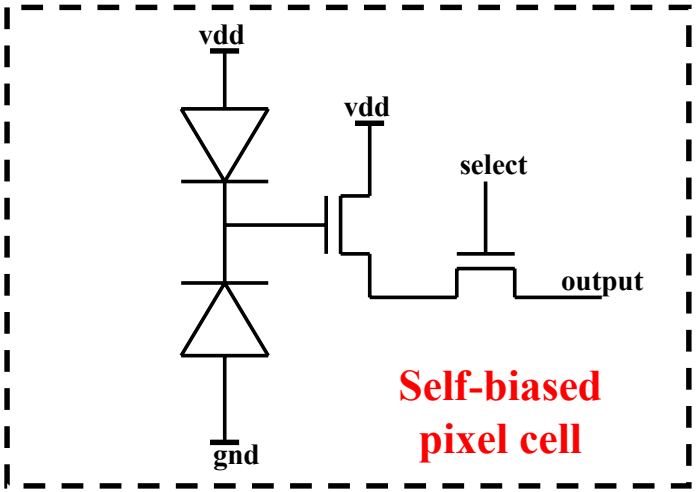
MimoSTAR case: self-biasing



- NO Reset (only synchronisation pulse at the beginning)
- NO pedestal (dark current) correction
- NO Common Mode correction???

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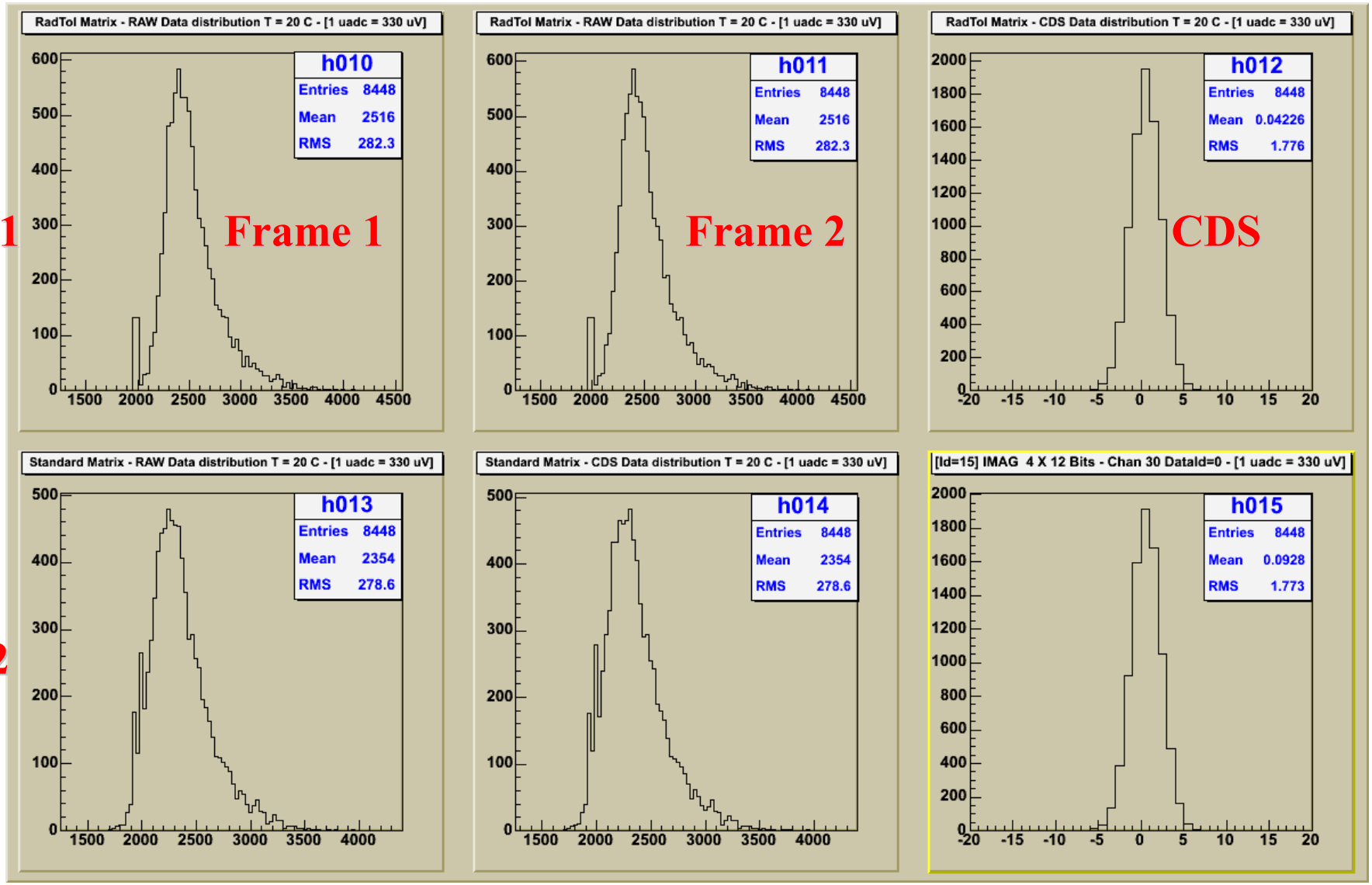
Raw data examples from MimoSTAR 2 (ADC counts)

Ch. #1

Ch. #2



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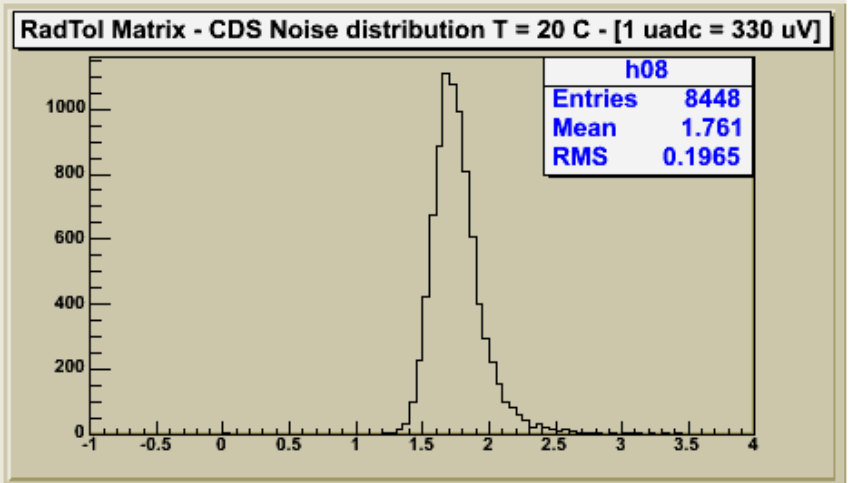
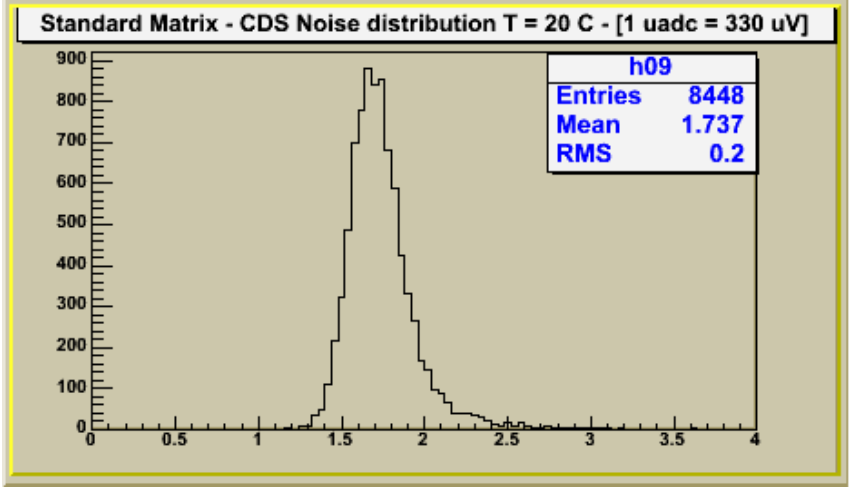
Raw noise distribution

Ch. #1



Ch. #2



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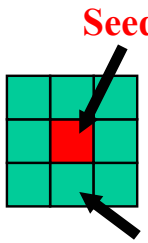
Mimosa9 beam tests: efficiency, noise hit rejection



Hit selection: $\{S/N_{seed} > n\}$ AND $\{S/N_{crown} > k\}$; $Noise_{crown} = \sqrt{8} \times Noise_{pixel}$

For n = 4 and k = 2 → noise hit rejection should be $> 10^6$

that's about what we measure…

Measured MIP detection efficiency > 99.5%
for n = 6 (5) and k = 4 (2)

Noise safety factor of 2 ÷ 2.5, before efficiency drops…

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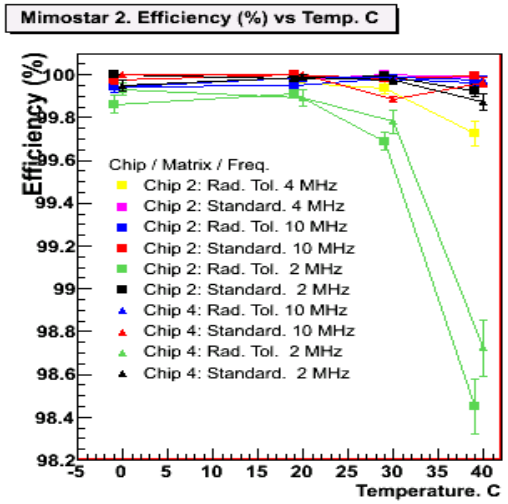
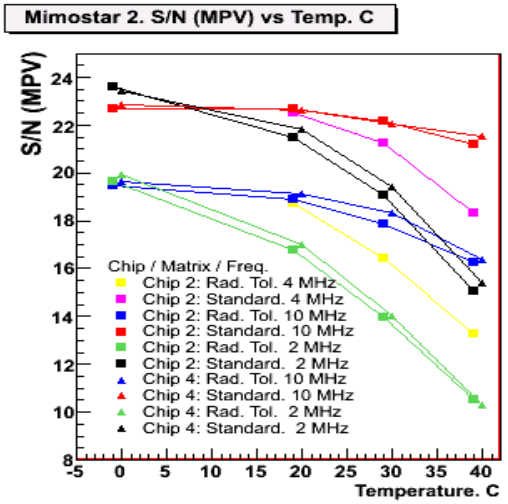
MimoSTAR2 beam tests summery

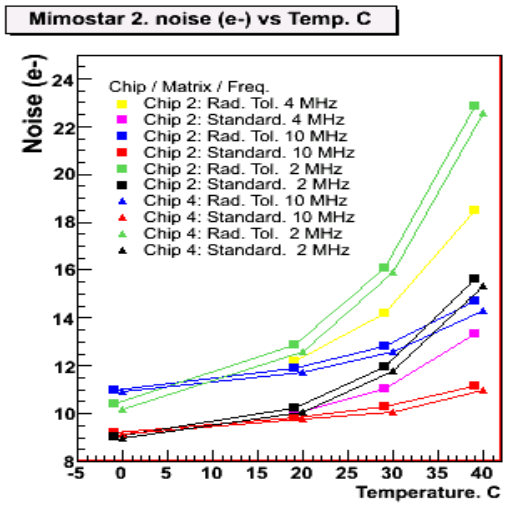
10 MHz = 800 µs integration

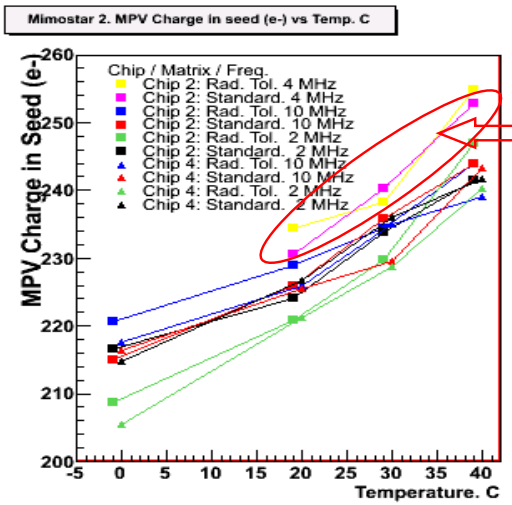
4 MHz = 2 ms integration

2 MHz = 4 ms integration









Estimated/preliminary calibration @4MHz

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Minimum on-line data processing: data flow estimation

No data reduction:

10^5 pixels × 4 ref. planes × 2 bytes × 1 kframes/s = 0.8 Gbytes/s

Quite a lot!!!

Zero suppression:

4 clusters × 10 pixels × 4 ref. planes × 4 bytes (address and CDS) × 1 kframes/s = 640 kbytes/s

Much better! (three orders of magnitude less)

Sparsification:

4 clusters × 4 ref. planes × 8 bytes (x and y position, amplitude) × 1 kframes/s = 128 kbytes/s

Factor five less

Full track reconstruction:

2 tracks × 12 bytes (x, y, θ, ϕ, χ^2) × 1 kframes/s = 24 kbytes/s

Another factor five less

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Minimum amount of calculation for zero-suppression in FPGA, supposing pipelining (one operation per 50 ns clock cycle)

1. Read from ADC (frame n)
2. Read from memory (frame n-1), write to memory (frame 2)
3. CDS: frame (n) – frame (n-1)
4. CDS – threshold
5. Decision
6. Neighbors selection
7. Address and amplitude coding
8. Transmission to the buffer memory (FIFO?)

What with the common mode correction? Really needed?
Possible on the basis of data from one row?

Expert needed in order to estimate the minimum FPGA resources!

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The DAQ system: examples from existing (@IReS) device

- Present system based on VME boards: 4-channel, 12 bit, 40 MHz ADC, FPGA XC4000, 4Mby RAM for digital conversion, zero- suppression implemented and tested @10 MHz several years ago (by Pawel Jaloha) but never used in practice

- Soon replaced by USB boards: 4-channel, 12 bit, 50 MHz ADC, FPGA Virtex2, 4Mby RAM for digital conversion AND sparsification (to be implemented)

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DAQ USB 2.0

Analog

· 4 ADC 12 bits – 40 Mhz

· 10^6 pixels **shared** 1-4 Inputs

Digital

· **Pattern** generator **& Trigger**

· 12 **Digital I/O: 8 LVDS and 4 NIM (2 In, 2 Out)**

Daq

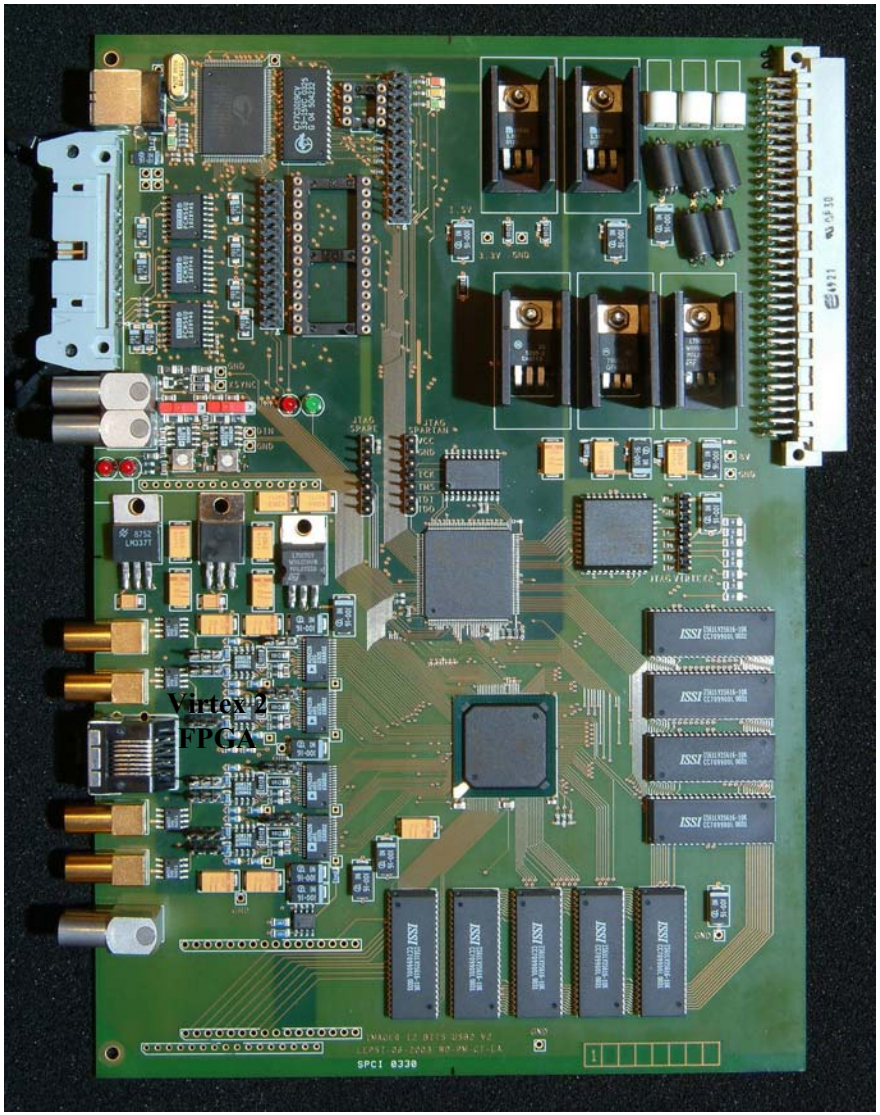
· Transfer **15 MB/ s USB 2.0**

Firmware (To Be Done)

· CDS Calculation (Done)

· Pedestal subtraction

· Data sparsification



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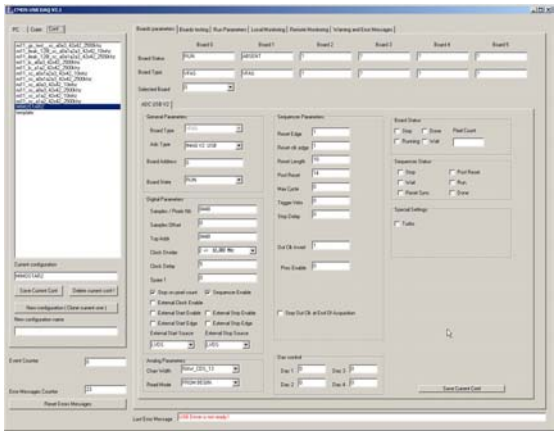
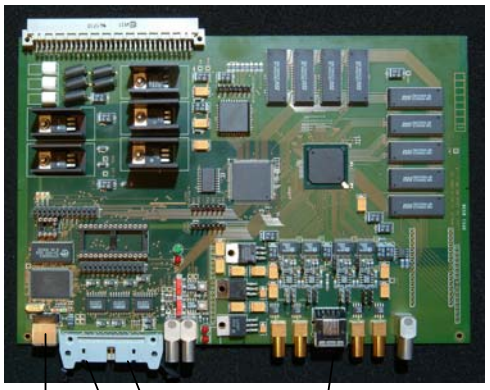
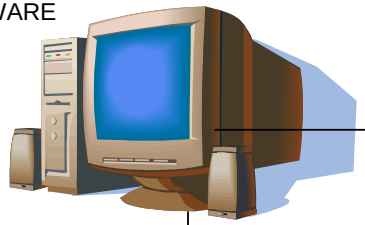
Minimum set-up to run MimoSTAR sensor



GUI FOR DAQ SOFTWARE

IMAGER USB 2.0 BOARD





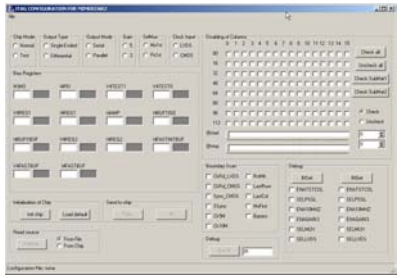
USB 2.0 CONNECTION FOR DAQ

ANALOG DATA FROM
MIMOSTAR2 TEST BOARD

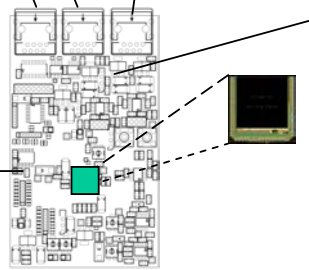
CLOCK/ SYNCRONIZATION
SIGNALS
STATUS SIGNALS

LV POWER SUPPLY

GUI FOR JTAG SOFTWARE



PARALLEL PORT CONNECTION FOR JTAG



MIMOSTAR2 CHIP

MIMOSTAR2 TEST BOARD

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Conclusions and prospects

If the DAQ specification agreed on, the development may start soon!

Should it be based on existing boards? If not, what will be effect on the schedule?

We must also soon discuss and agree on the Sensor/DAQ Interface (mechanics, electric standards, protocol)

The final DAQ for digitally readout sensors should be the logical evolution of the Demonstrator DAQ!