

Prog. Report & Plans on Demonstrator & Ultimate Sensors

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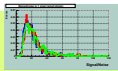
OUTLINE

- MIMOSA-14 (alias MIMO★-2) beam test results
- Plans for MIMO★-3 \mapsto demonstrator
- Progress and Plans for the final sensors: 1) fast col.. // with ADC, 2) high precision array
- Summary



- ▶ **AMS 0.35 μm OPTO techno. (... may still be available for 10 yrs ...):**
 - ◇ **2 matrices of 64 x 128 pixels (30 μm pitch) \mapsto active area of 4 x 4 mm²**
 - \hookrightarrow 1 matrix with rad. hard pixels (already tested with MIMO-11)
 - ◇ **JTAG architecture for steering**
 - ◇ **frame r.o. time: 0.8, 1.6, 4.0 ms (pixel r.o. frequency: 10, 4, 2 MHz)**

- ▶ **Developed for STAR vertex detector upgrade:**
 - ◇ **operated at $T \lesssim 40^\circ C$**
 - ◇ **required rad. tolerance: $\lesssim 3 \cdot 10^{11} n_{eq}/cm^2$ – O(10) kRad/yr**
 - \hookrightarrow installation of **Large** version inside apparatus in 2007/2008

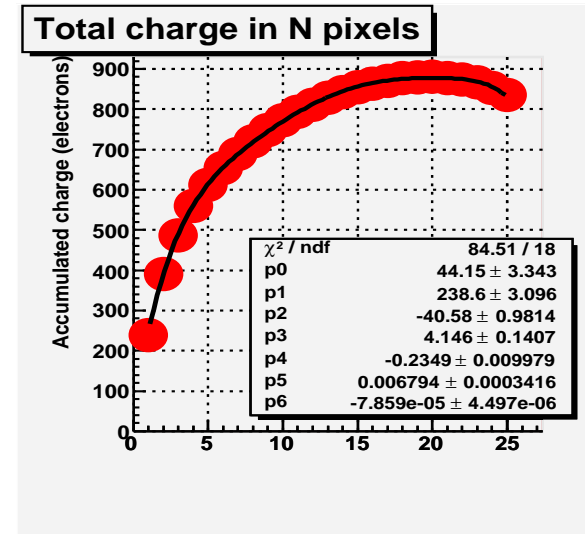
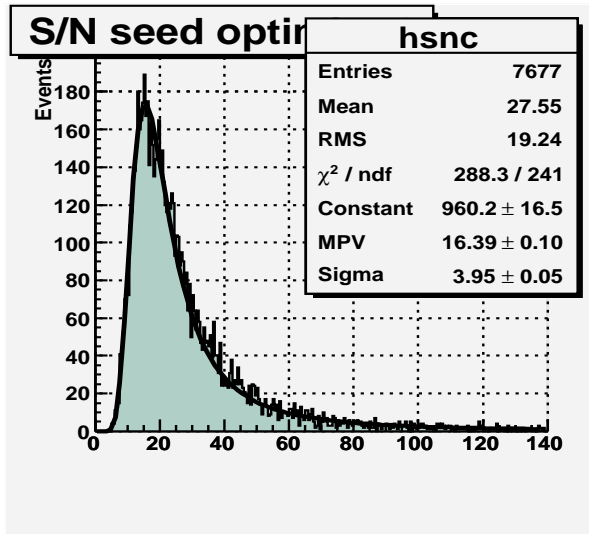
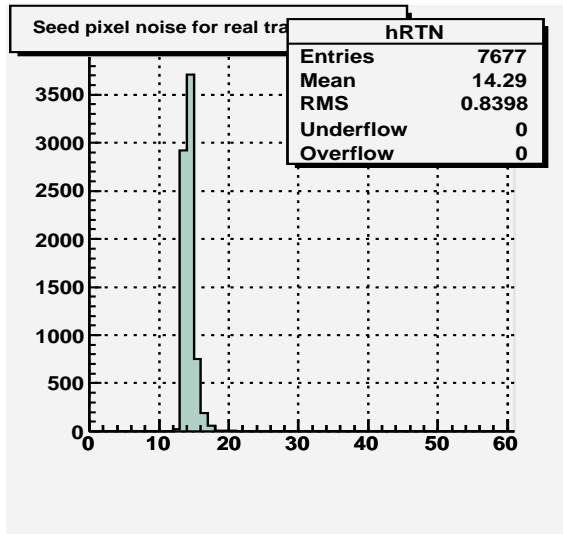
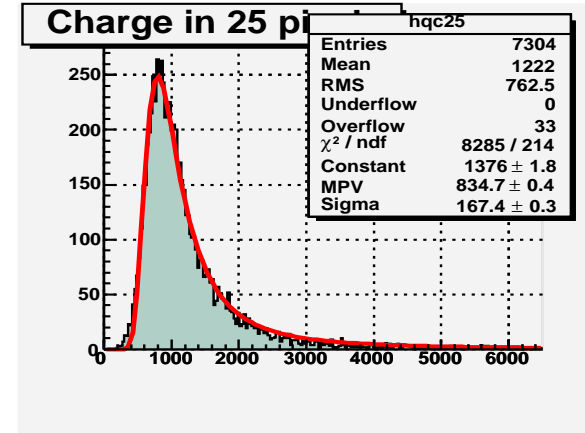
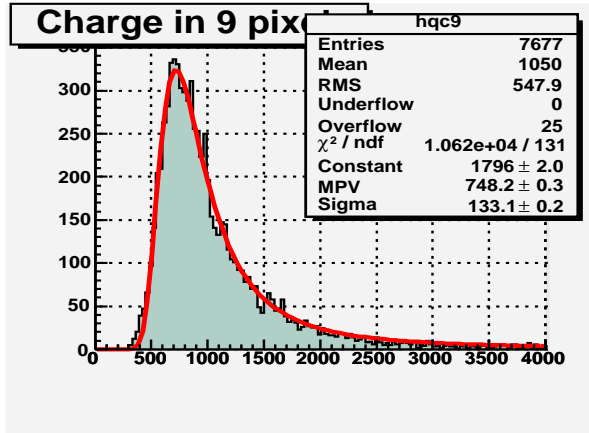
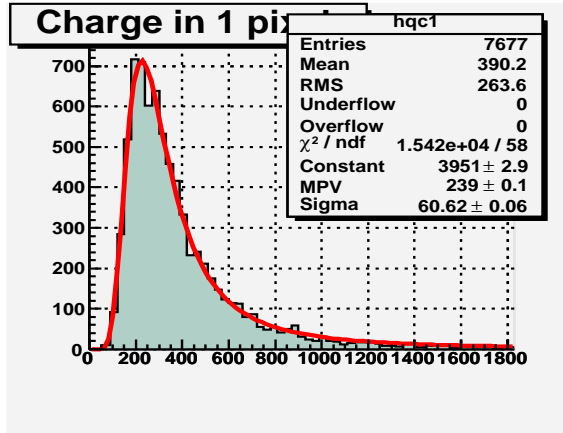


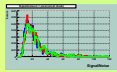
MIMO★-2 beam test results

DESY: 5 GeV/c Electrons in November 2005

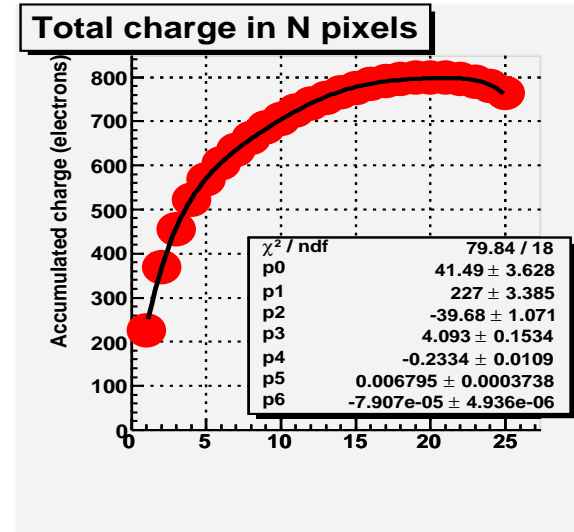
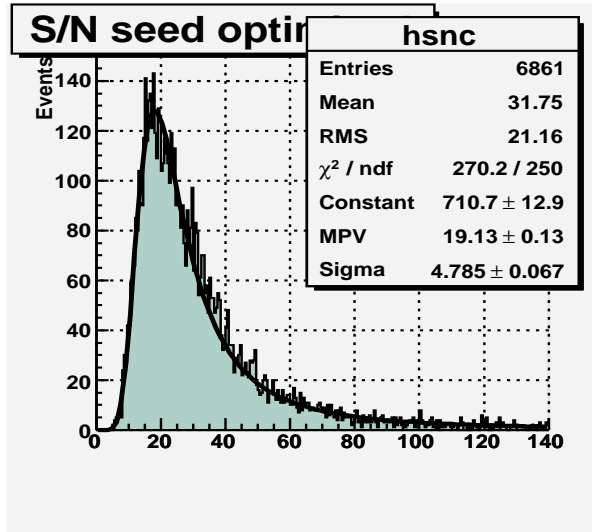
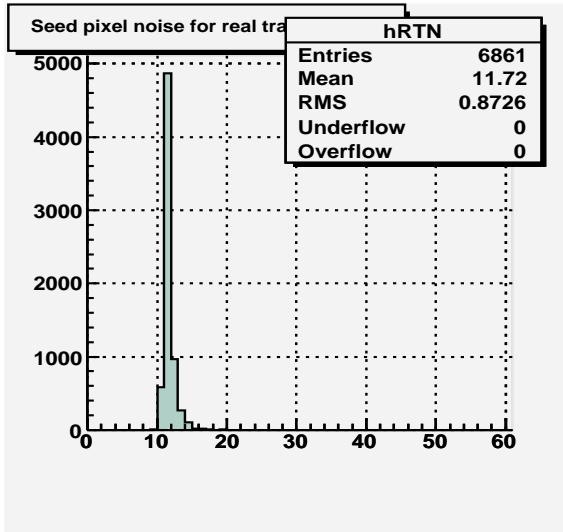
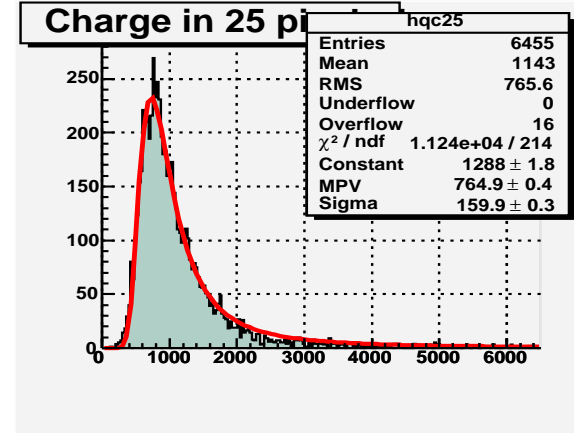
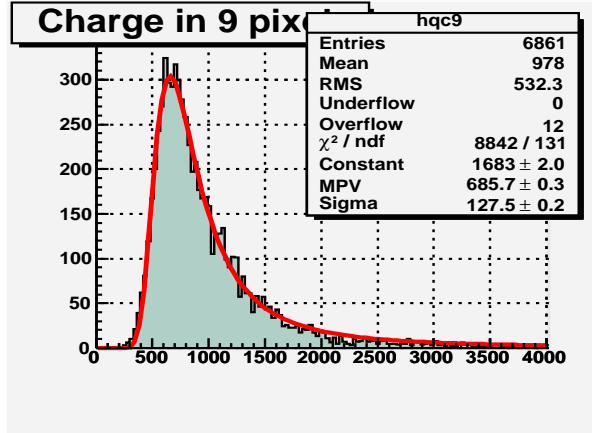
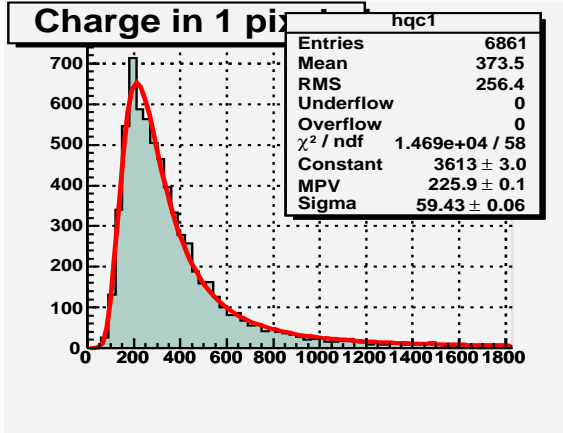


M14 ; run 14508; PI 9, sub 1, dist 150; Gain 8.24; eff 99.974 +- 0.018; Seed 5.0; Neigh 2.0



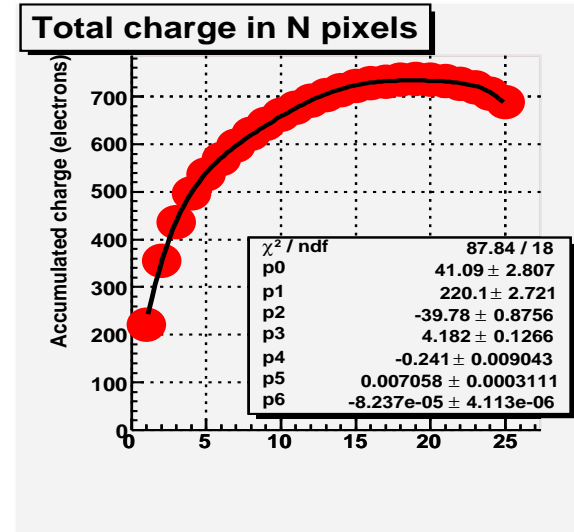
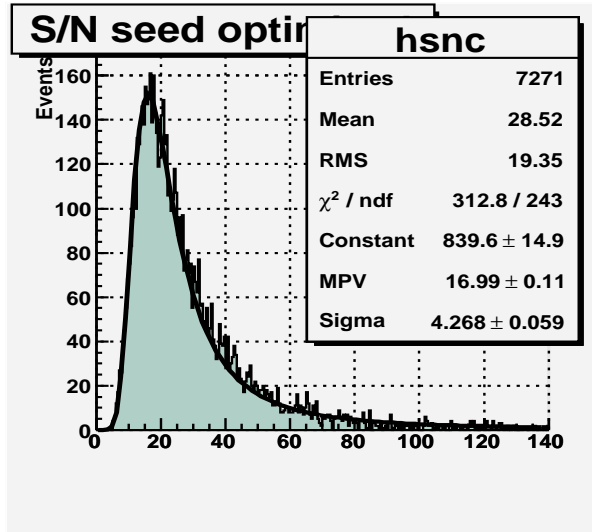
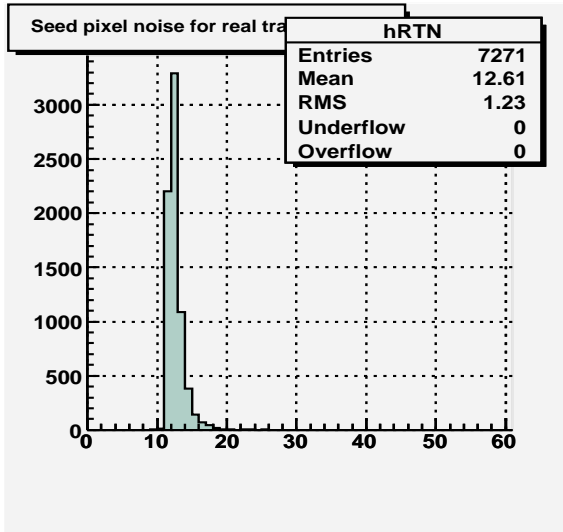
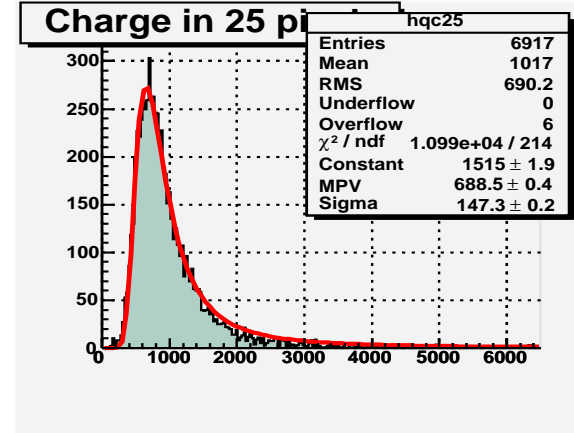
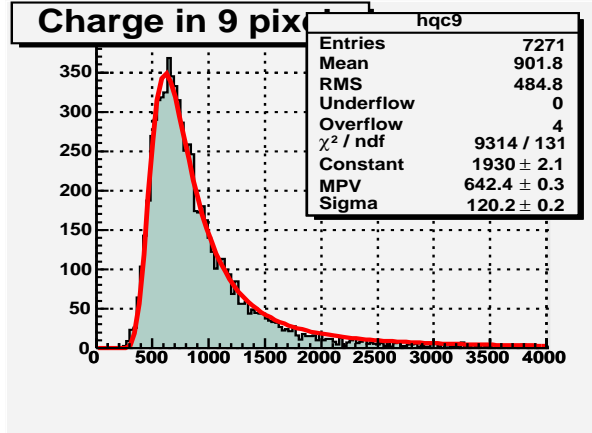
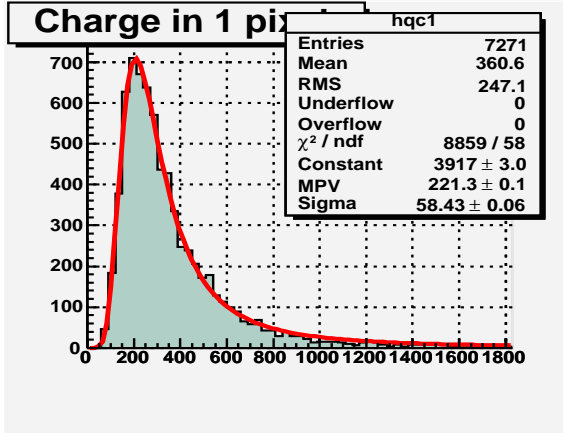


M14 ; run 14512; PI 9, sub 1, dist 150; Gain 8.00; eff 99.985 +- 0.015; Seed 5.0; Neigh 2.0





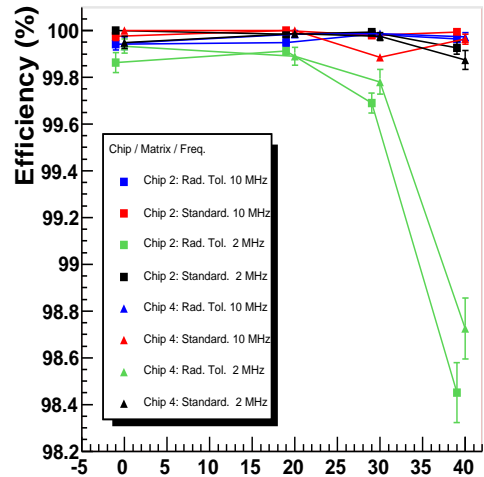
M14 ; run 14513; PI 9, sub 1, dist 150; Gain 6.92; eff 99.890 +/- 0.039; Seed 5.0; Neigh 2.0





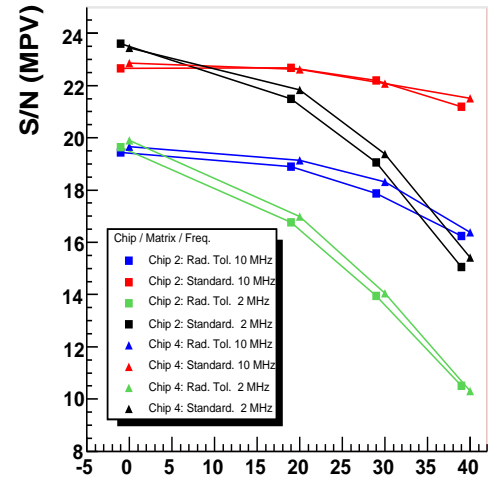
- ▶ JTAG design fully proved
- ▶ Main results at $T = 25^\circ$ and $t_{r.o.} = 0.8$ & 4 ms:
 - ∴ $N \sim 11 - 14 e^- ENC$
 - ∴ $S/N \sim 15 - 21$ (MPV)
 - ∴ $\epsilon_{det} \gtrsim 99.8\%$
 - ∴ $\sigma_{sp} \sim 3 \mu m$ (MIMOSA-9)

Mimostar 2. Efficiency (%) vs Temp. C



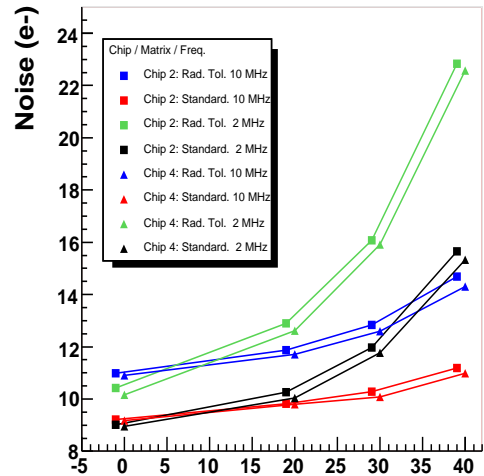
Temperature. C

Mimostar 2. S/N (MPV) vs Temp. C



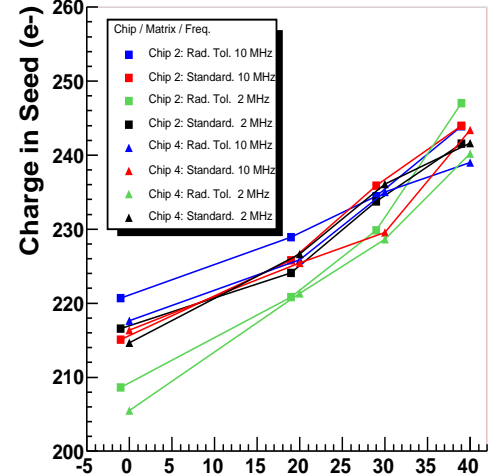
Temperature. C

Mimostar 2. noise (e-) vs Temp. C



Temperature. C

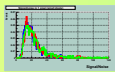
Mimostar 2. Charge in seed (e-) vs Temp. C



Temperature. C

▶ CONCLUSION:

- ◇ Architecture of sensor for telescope demonstrator running at room temperature validated
 - ↳ few sensors available early '06 for EUDET
- ◇ Design of final sensor for demonstrator can start
 - ↳ ∴ fabrication \gtrsim Summer '06
 - ∴ chips available for mounting \sim end '06



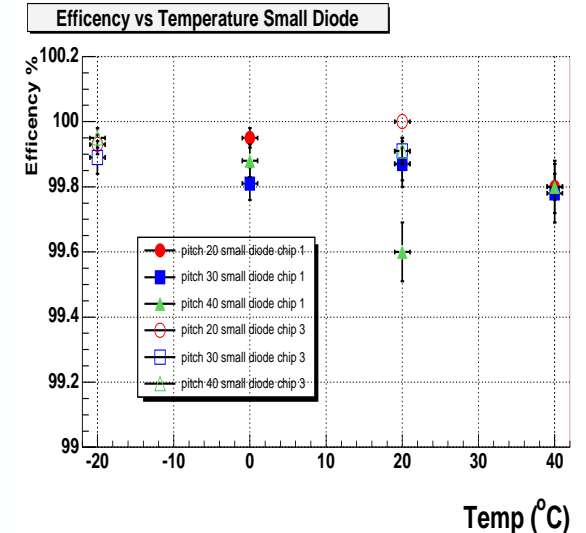
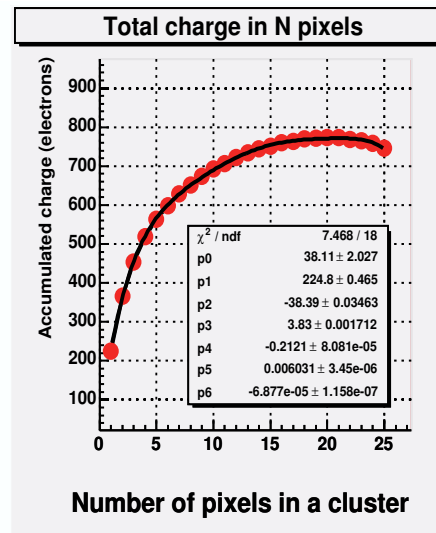
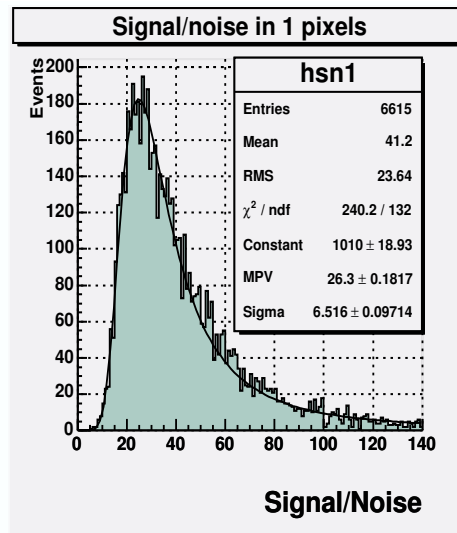
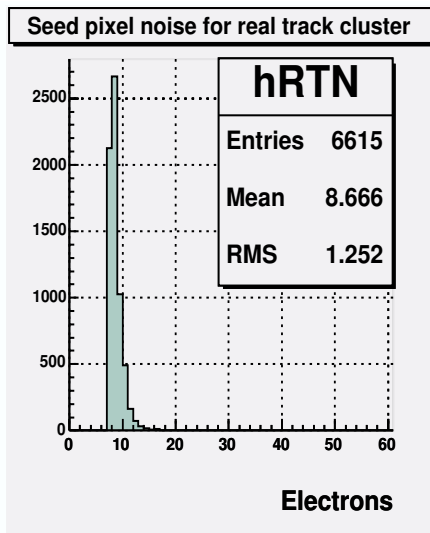
► Fabrication process explored with MIMOSA-9, -11, -14, -15

↳ assessed in terms of epi. thickness, noise & S/N (T), rad. tolerance, ...

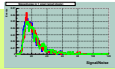
► Excellent m.i.p. detection performances (observed with 120 GeV/c π^- at CERN-SPS):

◇ S/N \sim 20-30 (MPV) \rightarrow $\epsilon_{det} \sim$ 99–99.9 %

◇ $\sigma_{sp} = 1.5 \mu m$ (20 μm pitch) – 3 μm (30 μm pitch)



■ **AMS-0.35 μm OPTO:** most attractive process tested up to now \mapsto baseline for further sensor R&D
(seems available for long ...)



NEXT STEPS

SENSORS EQUIPPING THE TELESCOPE DEMONSTRATOR

**■ MIMO★-3L (for Large) :**

- Technology: AMS 0.35 OPTO
- ◇ STAR upgrade for physics run ≤ 2009 (AuAu coll.)
- 640 x 256 pixels (30 μm pitch) = 10 sub-arrays of 64 x 256 pixels
- ◇ Active surface $\sim 19.2 \times 7.7 \text{ mm}^2$ (10 x MIMO★-2)
- 2 // outputs (50 MHz) $\mapsto t_{r.o.} = 1.6 \text{ ns}$
- ◇ Same JTAG design as MIMO★-2
- Fabrication planned for late Summer 2006 via engineering run
 - \hookrightarrow to be mounted on 20 cm ladders at LBNL in 2007 \mapsto physics ≥ 2008
- ◇ Reticle (engineering run) will host several other chips



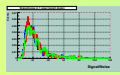
■ MIMO★-3M (for Medium) = 40 % of MIMO★-3L surface

- 256 x 256 pixels (30 μm pitch) = 4 sub-arrays of 64 x 256 pixels
- ◇ Active surface $\sim 7.7 \times 7.7 \text{ mm}^2$ (4 x MIMO★-2)
- 4 // outputs (10 MHz) $\mapsto t_{r.o.} = 1.6 \text{ ms}$ (baseline)
- ◇ Same JTAG design as MIMO★-2
- To be fabricated planned in same engineering run as MIMO★-3L
- ◇ Some (rather minor) details may still vary w.r.t. the above (e.g. sub-arrays of 64 x 320 pixels)

■ Time -Line: chip fabricated and tested \leq end 2006



PROGRESS AND PLANS FOR FINAL SENSORS EQUIPPING THE TELESCOPE

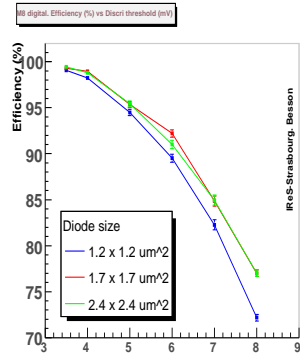


► MIMOSA-8 tests with 5 GeV/c e^- beam at DESY in September 2005

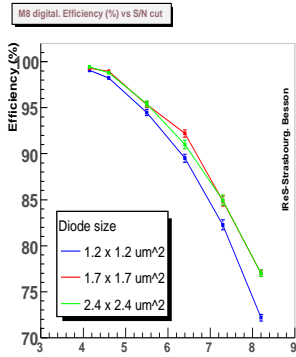
► Excellent m.i.p. detection performances despite modest thickness of epitaxial layer

◇ det. eff. \sim 99.3 % for fake rate of \sim 0.1 %

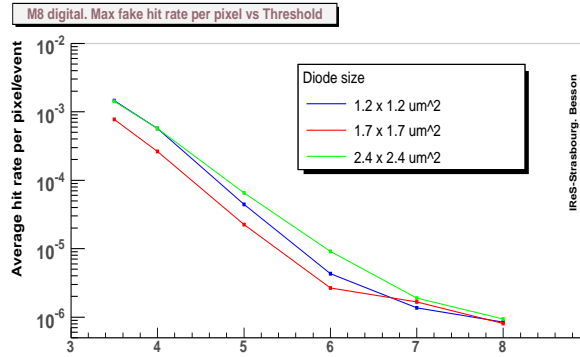
◇ discriminated cluster multiplicity \sim 3–4



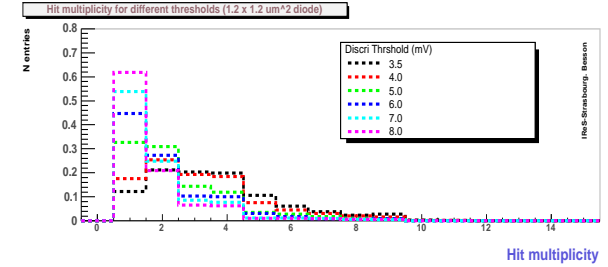
Discr. Threshold (mV)



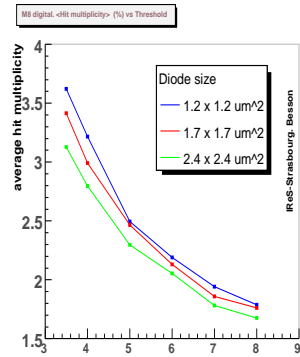
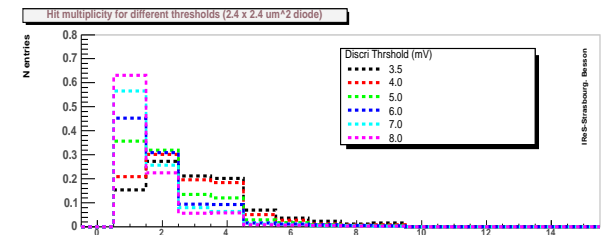
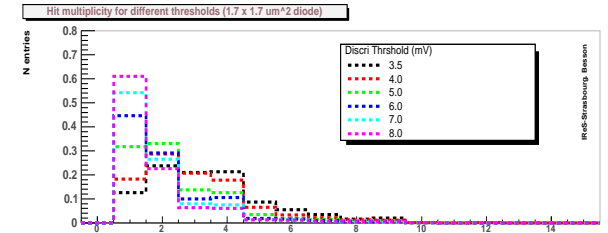
Discr. S/N cut



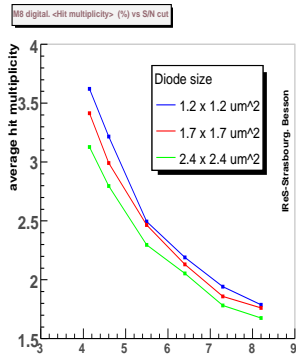
Discr Threshold (mV)



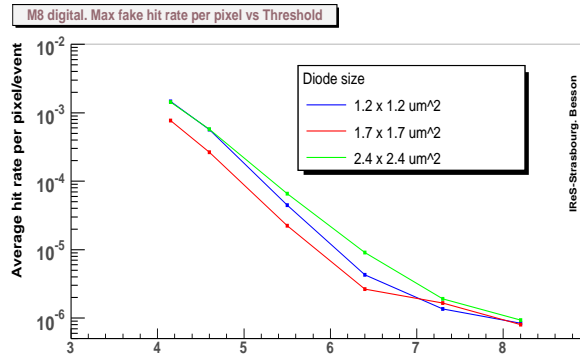
Hit multiplicity



Discr Threshold (mV)



Discr S/N cut



Discr. S/N cut

■ Archi. validated for next steps: techno., rad. tol. pixel at T_{room} , ADC, zero supp., etc. \rightarrow EUDET (2008)



- MIMO★-3L and MIMO★-3M manufactured via engineering run hosting several other devices: ILC VD, CBM VD, other GSI expts, generic functionalities, ...

- ▶ Several devices are relevant for EUDET:
 - new version of MIMOSA-8 (rad. tol. pixe, col. // r.o., digital output with 2xCDS & discri.)
 - ◇ various 4-5 bits ADC architectures to (ultimately) replace discri. of MIMOSA-8
 - imager prototype (512 x 512 pixels ?) for high precision hit position det. (13-15 μm pitch)
 - ◇ several other test structures

- First studies of zero suppression architecture behind ADC have started

- High precision sensor design implemented in MIMOSA-15 will be tested early 2006

- Thinning investigations $\lesssim 50 \mu m$ continue



■ Chip architecture for telescope demonstrator works very well

↳ few sensors will be available early 2006 for EUDET

■ Design of final sensor for demonstrator can start:

↳ ∴ fabrication \lesssim end Summer 2006 \mapsto chips available for mounting \sim end 2006

∴ more details on output signals and chip steering in Wojciech's talk

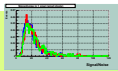
■ Engineering run will also include:

○ prototype (extension of MIMOSA-8) for final chip

◇ various ADC alternatives for final chip

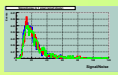
○ imager prototype for high precision hit position determination

■ Zero suppression study for final sensor has started



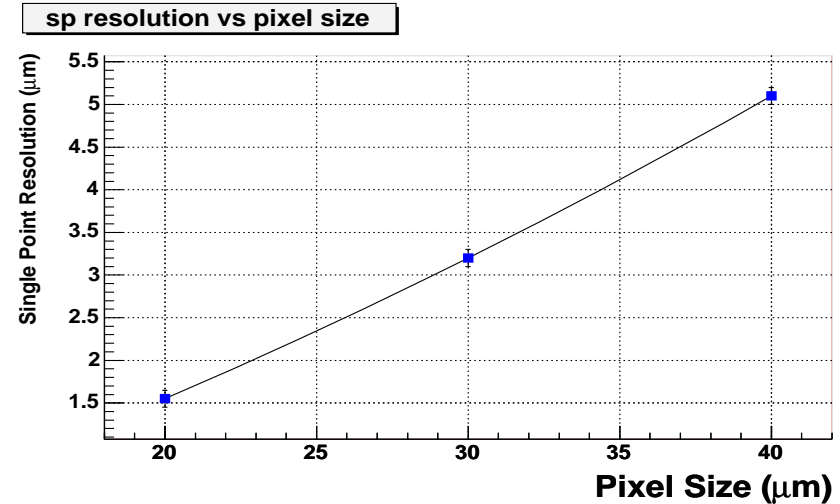
BACKUP SLIDES

SPATIAL RESOLUTION, RAD. TOLERANCE, MIMOSA-8



► Single point resolution versus pixel pitch:

- ◇ chips mounted on Si-strip telescope (8 planes)
installed on a 120 GeV/c π^- beam at CERN-SPS
- ◇ clusters reconstructed with eta-function,
exploiting charge shared between pixels
- ◇ $\sigma_{sp} \sim 1.5 \mu\text{m}$ (20 μm pitch)
↳ $\sigma_{sp} \sim 5 \mu\text{m}$ (40 μm pitch)

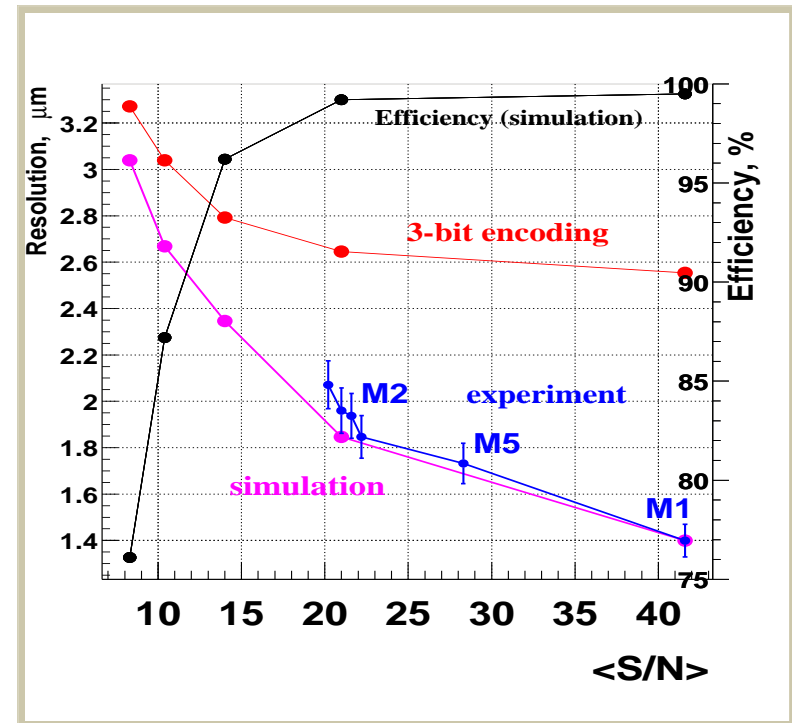


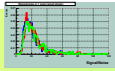
► σ_{sp} dependence on S/N and on ADC granularity:

- ◇ results found with "simple" pixels are excellent
(but no integrated signal processing ...)
- ◇ noise of FAST pixels will be \sim twice higher ($\sim 20 e^-$ ENC)
- ◇ effect simulated on real MIMOSA data (120 GeV/c π^-)
(simulation consistency cross-checked with data)

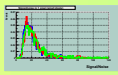
► $\epsilon_{det} \gtrsim 96\%$ if $\langle S/N \rangle \gtrsim 14$

$\sigma_{sp} \lesssim 3 \mu\text{m}$ even if $\langle S/N \rangle \sim 10$ and only 3-bit encoding

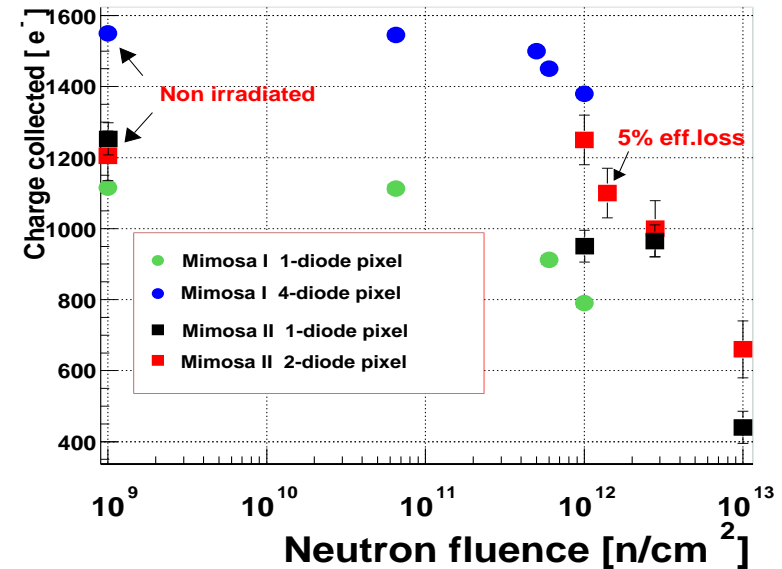




RADIATION TOLERANCE



- ▶ Neutrons of O(1 MeV) at JINR (Dubna):
irradiation of up to $10^{13} n_{eq}/cm^2$
 - ▶ Tests with 2 sensors from diff. fabrication processes:
 - ◇ AMS-0.6 ($\lesssim 14 \mu m$ epitaxy)
 - ◇ AMI-0.35 ($\sim 4 \mu m$ epitaxy)
- ↪ charge loss for $\lesssim 10^{12} n_{eq}/cm^2$
modest increase of I_{leak} & noise ($\lesssim 10\%$)



- ▶ AMS-0.35 OPTO ($\gtrsim 10 \mu m$ epitaxy)
↪ S/N(MPV) vs fluence and T:
- ↪ fluences of $\lesssim 10^{12} n_{eq}/cm^2$ acceptable,
better performances with $T < 0^\circ C$
($\epsilon_{det} \gtrsim 99.5 \pm 0.1\%$)

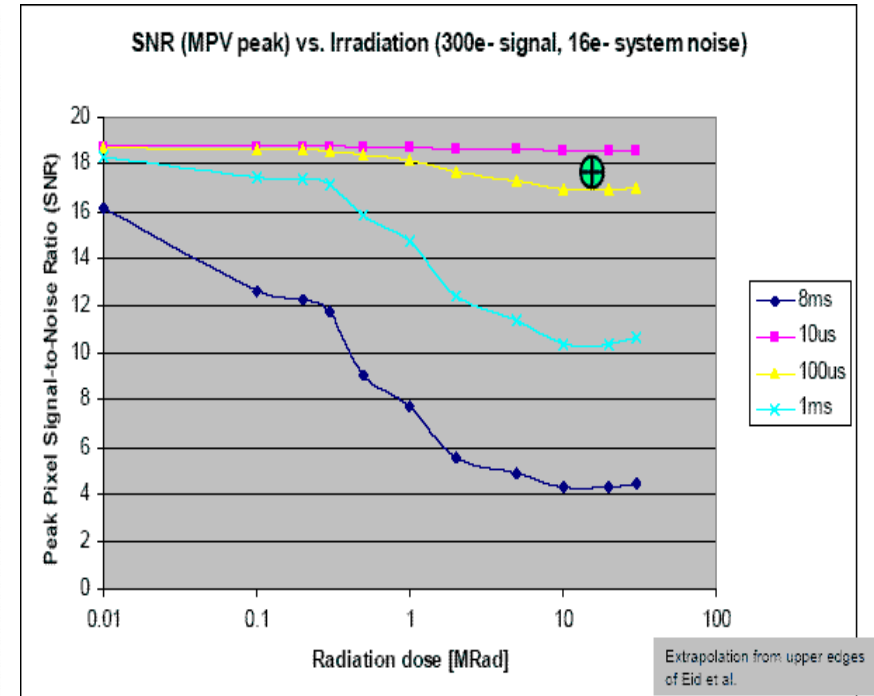
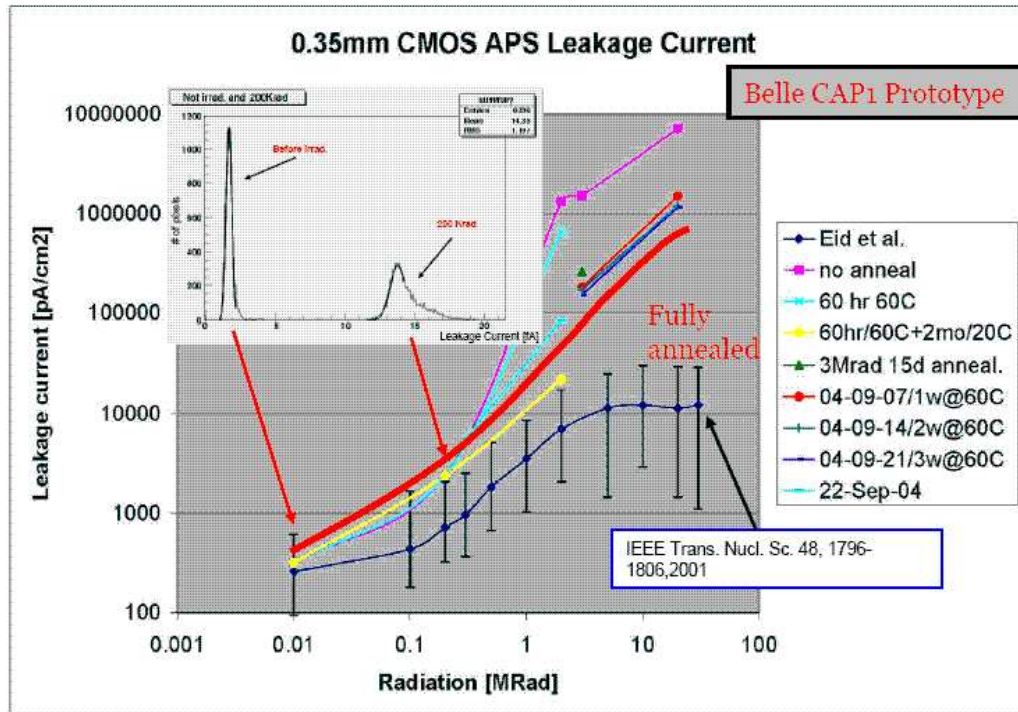
Fluence	T = -20°C	T = 0°C
0	28.4 ± 0.2	26.3 ± 0.2
$10^{11} n_{eq}/cm^2$	25.3 ± 0.2	24.5 ± 0.4
$10^{12} n_{eq}/cm^2$	18.7 ± 0.2	—

- Rad. tolerance is fabrication process dependent ↪ need more measurements
- Room for improvement ? → explore recovering procedures (vs t, T)



▶ 3 major effects expected from ionising radiation:

- ◇ Shift of threshold voltages: \propto Nb(holes) created & trapped in gate oxide \propto oxide thickness
 ↪ aim for \lesssim 10 nm thick oxide (\sim the case for \leq 0.35 μ m technologies)
- ◇ Leakage current in NMOS transistors
- ◇ Leakage current in N-channel intertransistors

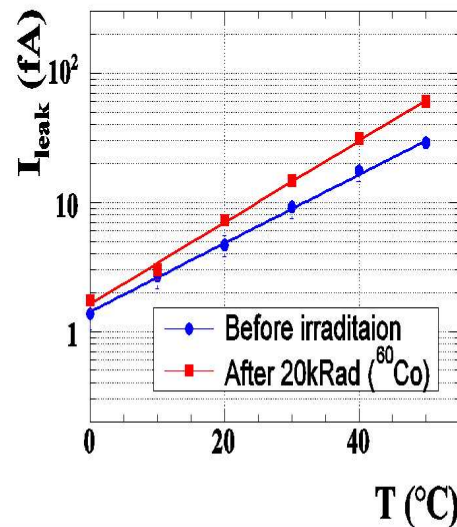
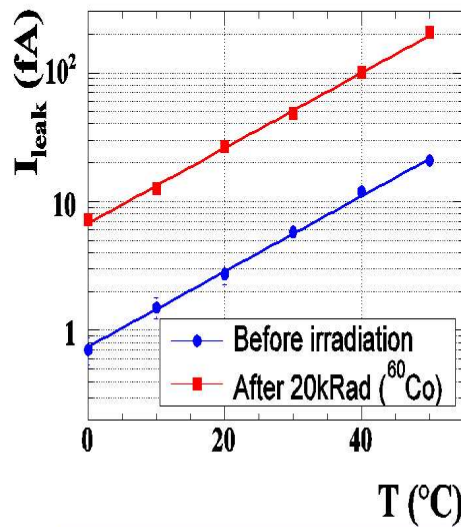
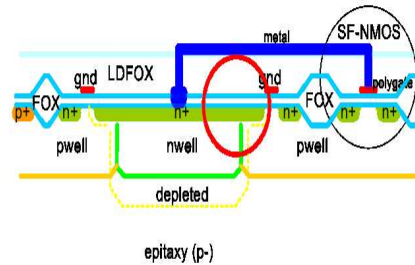
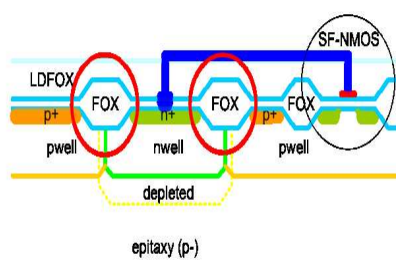


▶ Aim for short integration time and for $T \lesssim 0^\circ\text{C}$



Pixel designs avoiding thick oxide around N-well and including guard-ring

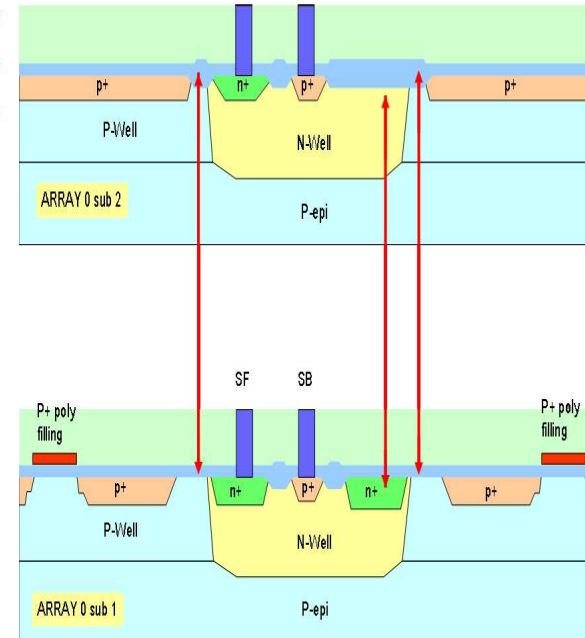
Studies on radiation hardness (ionising): MIMOSA9



Increase of leakage current depends on the diode layout.
 Probable reason: Presence of thick oxide (FOX) near the diode.

Beamtest on MIMOSA11

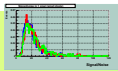
Running conditions: +40°C, 700µs readout time



	New	After 20kRad
Standard pixel (A0 Sub 2)		
S/N (MPV):	23.9	10.3
Det Eff [%]:	99.9	97.7
Noise [e ⁻]:	10.7	23.5

Hardened pixel (A0 Sub 1)		
S/N (MPV):	14.9	15.1
Det Eff [%]:	99.5	99.6
Noise [e ⁻]:	16.1	16.1

Radiation hardened pixel remains stable after irradiation.
 Obvious reason: Leakage current increases after irradiation slower than for the standard pixel.
 S/N of the radiation hard pixel is not yet optimized (See MIMOSA15).



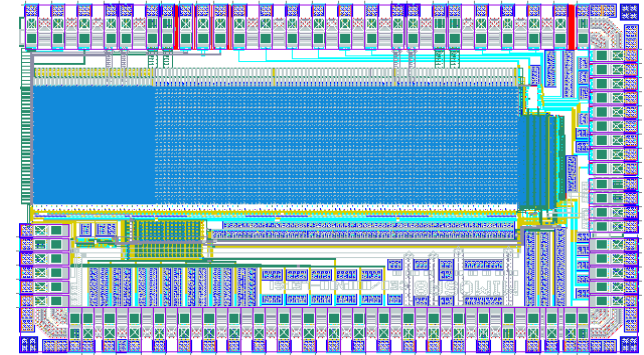
MIMOSA-8 (FAST COL. // WITH DISCRIMINATED OUTPUT)

CHARACTERISTICS AND LAB TEST RESULTS



► **MIMOSA-8:**

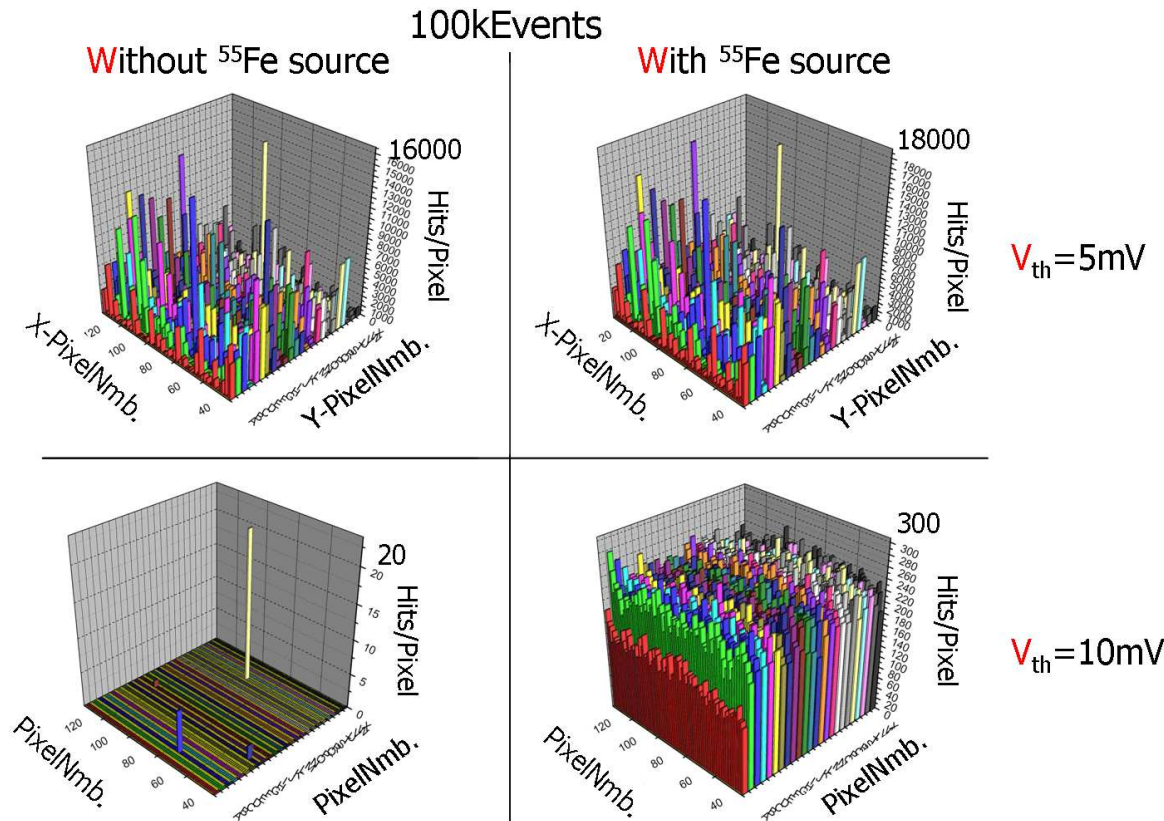
- TSMC 0.25 μm digital fab. process (8 μm epitaxy)
- 32 // columns of 128 pixels (pitch: 25 μm)
- 4 sub-arrays featuring AC and DC coupled on-pixel voltage amplif.
- on-pixel CDS
- discriminator at end of each column



► tests with ^{55}Fe source:

- ◇ conversion factor: 50 – 110 $\mu\text{V}/e^-$,
- ◇ pixel noise (including CDS): $\sim 13 - 18 e^- \text{ ENC}$!
- ◇ little pixel-to-pixel dispersion ($< 10 e^- \text{ ENC}$)!
- ◇ discriminator operational:
- ↳ discriminated ^{55}Fe X-Ray clusters observed !

■ Architecture seems worth extending with integ. ADC \mapsto EUDET E.U. project

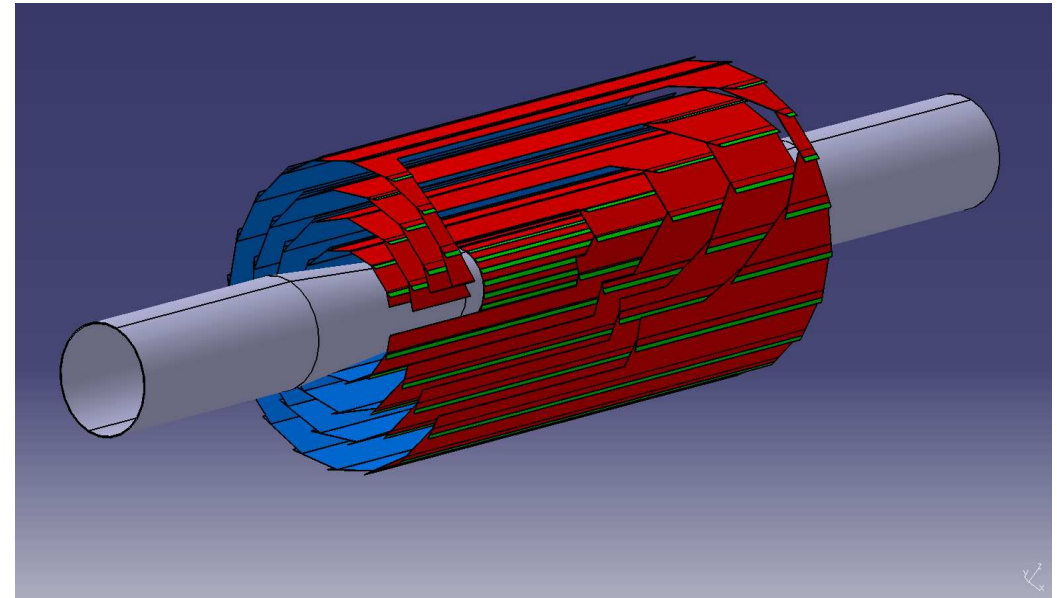




- Application to the ILC Vertex Detector

- ▶ **Geometry:** 5 cylindrical layers (R=15 – 60 mm), $\| \cos\theta \| \leq 0.90 - 0.96$
- ▶ $\sigma_{IP} = a \oplus b/p \cdot \sin^{3/2}\theta$, with $a < 5 \mu m$ and $b < 10 \mu m$
- ▶ **Read-out time:** \uparrow 25 μs in L0 \uparrow 50 μs in L1 $\therefore \lesssim 200 \mu s$ in L2, L3, L4

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	<100	<5
L1	25	25	50	26	65	<130	<7
L2	37	30	<200	24	75	<100	<5
L3	48	35	<200	32	70	<110	<6
L4	60	40	<200	40	70	<125	<6
Total				142	305	<565	<29



- ▶ **Ultra thin layers:** $\sim 0.1 \% X_0/\text{layer}$ (?) ▶ **Very low P_{diss}^{mean} :** $\ll 100 \text{ W}$ (\mapsto minimise cooling)
- ▶ **Rad. tolerance (3 yrs):** $\lesssim 3 \cdot 10^{10} n_{eq}/\text{cm}^2$ – $\lesssim 6 \cdot 10^{12} e_{10MeV}/\text{cm}^2$ (150 kRad, $2 \cdot 10^{11} n_{eq}/\text{cm}^2$)



▷ Fast col. // architecture (like MIMOSA-8), allowing to process signal (CDS, ADC, sparsification) during BX:
 ↪ complex, close to technology limits ↪ much design & test effort needed (but quite universal output)

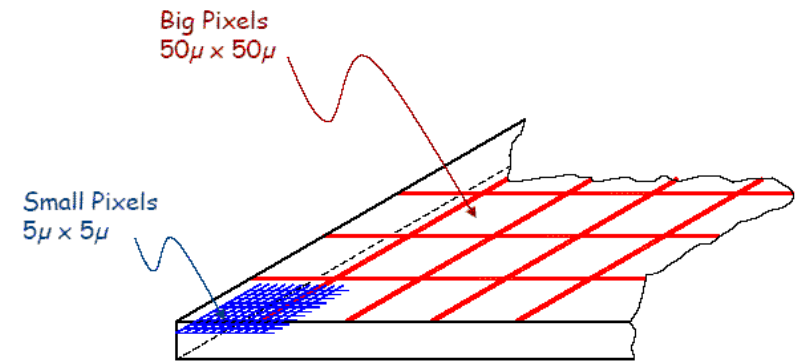
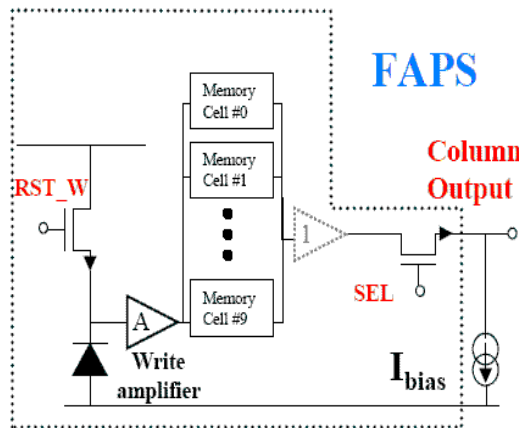
▶ Alternative ↪ 2 phase μ circuit architecture exploiting beam time structure, reducing data flux:

- 1) charge stored (eventually sampled) inside pixel during train crossing: $O(1)$ ms
- 2) signal transfered and processed inbetween trains: $O(100)$ ms

▶ Different strategies of storage during train crossings:

\therefore 20 – 25 μm large pixels with $\gtrsim 20$ capacitors
 ↪ $\lesssim 50 \mu s$ long snapshots/capacitor

\therefore $\lesssim 5 \mu m$ large pixels with 1 capa.(hit position)
 and 50 μm large pixels for hit zone selection



▷ Difficulty: are small capacitors precise enough ?

▷ Difficulty: can cluster size be $\lesssim 3$ pixels ?