L0/L1 Trigger Electronics for the ALICE PHOS Detector

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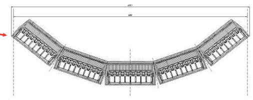
Introduction

The Photon Spectrometer (PHOS) of the ALICE experiment [1] at the LHC measures electromagnetic showers of up to 100 GeV via a large matrix of PWO crystals. L0 triggers for p-p collisions and the L1 triggers for Pb-Pb collisions are generated. Front End Cards (FEC) sum over 4 APDs which transform the collected light signal into an electric signal, and feed the analogue sum into the Trigger Region Unit (TRU), which contains 112 digitizer channels of 12 bits and covers 28x16 crystals. L0 trigger is generated in TRU, L1 trigger is generated in Trigger OR (TOR), which receives L0 trigger and data from TRU and sends the trigger to the Central Trigger Processor (CTP).

PHOS detector:
5 modules cover 5*20 degrees
- 18.000 PWO crystals
- 36.000 readout channels
- Level-0, Level-1 Trigger



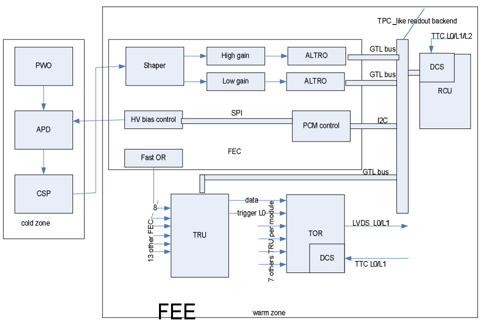
Each Module:56*64 crystals

L0/L1 requirements

In order to reduce overall data flow, ALICE trigger have three trigger levels. For PHOS, L0 is mainly used as a minimum bias trigger in p-p collisions. L1 is optimized to provide more information for particles produced in Pb-Pb collisions. The latency for L0 and L1 are 1.2 us and 6.5 us respectively, 400 ns is needed for the trigger signals to be processed in CTP (Central Trigger Processor) and travel from the CTP to the Front End Electronic (FEE). L0 must arrive at CTP within 800 ns after interactions, L1 must arrive within 6.1us. PHOS will generate one L0 and three L1 signals.

The embedded electronics

The PHOS FEE is embedded in the warm zone below the crystals [2]. Each group of 2x16 crystals generate 32 analog channels, which are passed into the warm zone. The FEC [3] in the warm zone shapes, digitizes and buffers these signal and also sums 2x2 analog channels. 14 FEE cards are interconnected to one TRU, which covers 28x16 crystals, as seen in the figure below. Each FEE card has 8 analog sums, so each TRU [4] has overall 112 channels which are handled by 14 ADCs with 8 channels. 8 TRUs per module are connected to TOR [5] which get the L0 trigger and data and then transmit L0 and generate L1. Following a valid trigger, the data stored in ALTRO are read out by RCU via GTL bus.



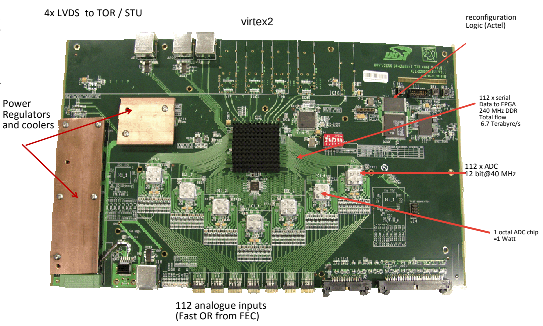
FEE

The FEC

The FEC has three important modules: Shaper, ALTRO and Fast OR. Fast OR combines 2x2 analog pulses from Charge Sensitive Pre-Amplifier and sends the results to TRU via differential lines. The card also contains a PCM controller, which is a firmware state machine that responds as slave device to the DCS subsystem of Readout Control Unit. The FEC HV bias controller sets the APD bias voltages individually.

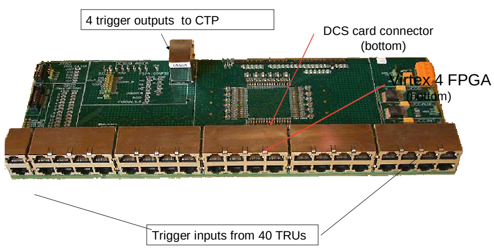
TRU and L0 trigger

PHOS has 5 modules, each module has 8 TRUs, each of which deals with 28x16 crystal signals, corresponding to 14x8 analog channels converted by 14 ADCs. The FPGA in TRU performs deseralization, comparison and buffering. Simulations prove that 2x2 sliding windows, which collects most of deposit energy for one photon, yields high trigger efficiency of > 95% at tolerable fake trigger levels.



TOR and L0/L1

The TOR card with DCS sitting on it connects up to 40 TRU inouts via differential cables. It combines L0s from the TRUs and sends it out. If the L0 is validated, TOR generates L1 trigger and sends it out.



Challenge:

2x2 sum data has to be collected from a large number of analog channels. During data collection, and after data concentration in the TOR unit, new overall sums have to be calculated in order to generate the final trigger signals. Everything has to be finished within 6.1 us. This sets very strict demands to the processing power and the data links. Each link has to transfer 200 Mbps, pushing the limits of the FPGAs and causing problems with cross-talk between the channels.

Conclusion:

The firmware for generation of L0 has been used at P2. Work is ongoing to generate L1,which concerns the data transmission between TRU and TOR and max finding. The link speed is at the limit for the FPGAs. . The finding of isolated photon and high pt + π0 and total Et is to be done in the future.

References

1. K.Aamodt et al.(The ALICE-PHOS collaboration) The ALICE experiment at the CERN LHC, JINST 3(2008) S08002.
2. H. Muller et al. (The ALICE-PHOS collaboration), Trigger electronics for the ALICE PHOS detector, Nucl. Instrum. Meth. A158 (2004) 525-528
3. H. Muller et al. (The ALICE-PHOS collaboration) Front-end electronics for PWO-based PHOS calorimeter of ALICE, Nucl. Instrum. Meth. A567 (2006) 264-267.
4. H. Muller et al. Trigger Region Unit for the ALICE PHOS calorimeter, 11th workshop on electronics for LHC and future experiments, Heidelberg Germany Sept 2005.
5. J. Alme et al. Radiation-tolerant SRAM-FPGA Based Trigger and Readout Electronics for the ALICE experiment, IEEE Trans. Nucl. Sci. 55(2008) 76-83.